Instruction Specifier	Mnemonic	Instruction	Addressing Modes	Status Bits
0000 0000	CTOD			
0000 0000	STOP	Stop execution	U	
0000 0001	RETTR	Return from trap	U	
0000 0010	MOVSPA	Move SP to A	U	
0000 0011	MOVFLGA	Move NZVC flags to A	U	
0000 010a	BR	Branch unconditional	i, x	
0000 011a	BRLE	Branch if less than or equal to	i, x	
0000 100a	BRLT	Branch if less than	i, x	
0000 101a	BREQ	Branch if equal to	i, x	
0000 110a	BRNE	Branch if not equal to	i, x	
0000 111a	BRGE	Branch if greater than or equal to	i, x	
0001 000a	BRGT	Branch if greater than	i, x	
0001 001a	BRV	Branch if V	i, x	
0001 010a	BRC	Branch if C	i, x	
0001 011a	CALL	Call subroutine	i, x	
0001 100	NOT :-	Div. i. i.	**	NZ
0001 100r	NOTr	Bitwise invert r	U	NZV
0001 101r	NEGr	Negate r	U	NZVC
0001 110r	ASLr	Arithmetic shift left r	U	NZC
0001 111r	ASRr	Arithmetic shift right r	U	C
0010 000r	ROLr	Rotate left r	U	C
0010 001r	RORr	Rotate right r	U	C
0010 01nn	NOPn	Unary no operation trap	U	
0010 1aaa	NOP	Nonunary no operation trap	i	
0011 0aaa	DECI	Decimal input trap	d, n, s, sf, x, sx, sxf	NZV
0011 0aaa 0011 1aaa	DECO	Decimal output trap	i, d, n, s, sf, x, sx, sxf	
0100 0aaa	STR0	String output trap	d, n, sf	
0100 0aaa 0100 1aaa	CHARI	Character input	d, n, s, sf, x, sx, sxf	
0100 Taaa 0101 Oaaa	CHARO	Character output	i, d, n, s, sf, x, sx, sxf	
0101 Oaaa	CHARO	Character output	1, u, 11, 5, 51, A, 5A, 5A1	
0101 1nnn	RETn	Return from call with n local bytes	U	
0110 0aaa	ADDSP	Add to stack pointer (SP)	i, d, n, s, sf, x, sx, sxf	NZVC
0110 1aaa	SUBSP	Subtract from stack pointer (SP)	i, d, n, s, sf, x, sx, sxf	NZVC
0111 raaa	ADDr	Add to r	i, d, n, s, sf, x, sx, sxf	NZVC
1000 raaa	SUBr	Subtract from r	i, d, n, s, sf, x, sx, sxf	NZVC
1001 raaa	ANDr	Bitwise AND to r	i, d, n, s, sf, x, sx, sxf	NZ
1010 raaa	ORr	Bitwise OR to r	i, d, n, s, sf, x, sx, sxf	NZ
1011 raaa	CPr	Compare r	i, d, n, s, sf, x, sx, sxf	NZVC
1100 raaa	LDr	Load r from memory	i, d, n, s, sf, x, sx, sxf	NZ
1101 raaa	LDBYTEr	Load byte from memory	i, d, n, s, sf, x, sx, sxf	NZ
1110 raaa	STr	Store r to memory	d, n, s, sf, x, sx, sxf	
1110 taaa 1111 raaa	STBYTEr	Store byte r to memory	d, n, s, sf, x, sx, sxf	
111111111111111111111111111111111111111	JIDIILI	Store by to I to inclinory	G, 11, 5, 51, A, 5A, 5A1	

aaa	Addressing mode
000 001 010 011 100 101 110 111	Immediate Direct Indirect Stack-relative Stack-relative deferred Indexed Stack-indexed Stack-indexed

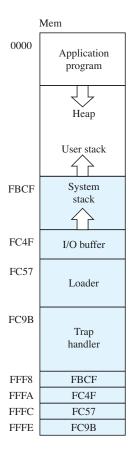
a	Addressing mode
0 1	Immediate Indexed

r	Register
0	Accumulator, A
1	Index register, X

- **(b)** The addressing-a field.
- (c) The register-r field.

(a) The addressing-aaa field.

Addressing Mode	aaa	Letters	Operand
Immediate Direct Indirect Stack-relative	000 001 010 011	i d n s	OprndSpec Mem [OprndSpec] Mem [Mem [OprndSpec]] Mem [SP + OprndSpec]
Stack-relative deferred Indexed Stack-indexed Stack-indexed deferred	100 101 110 111	sf x sx sxf	Mem [Mem [SP + OprndSpec]] Mem [OprndSpec + X] Mem [SP + OprndSpec + X] Mem [Mem [SP + OprndSpec] + X]



```
Mnemonic
                       Register transfer language specification
ST0P
                       Stop execution
                       NZVC \leftarrow Mem[SP] \langle 4...7 \rangle; A \leftarrow Mem[SP + 1]; X \leftarrow Mem[SP + 3];
RETTR
                       PC \leftarrow Mem[SP + 5] ; SP \leftarrow Mem[SP + 7]
MOVSPA
                       A \leftarrow SP
                       A \langle 0..11 \rangle \leftarrow 0, A \langle 12..15 \rangle \leftarrow NZVC
MOVFLAGA
                       PC \leftarrow Oprnd
\mathsf{BR}
                       N = 1 \lor Z = 1 \Rightarrow PC \leftarrow Oprnd
BRLE
                       N = 1 \Rightarrow PC \leftarrow Oprnd
BRLT
                       Z = 1 \Rightarrow PC \leftarrow Oprnd
BREQ
                       Z = 0 \Rightarrow PC \leftarrow Oprnd
BRNE
                       N = 0 \Rightarrow PC \leftarrow Oprnd
BRGE
                       N = 0 \land Z = 0 \Rightarrow PC \leftarrow Oprnd
BRGT
                       V = 1 \Rightarrow PC \leftarrow Oprnd
BRV
BRC
                       C = 1 \Rightarrow PC \leftarrow Oprnd
                       SP \leftarrow SP - 2; Mem[SP] \leftarrow PC; PC \leftarrow Oprnd
CALL
                       r \leftarrow \neg r; N \leftarrow r < 0, Z \leftarrow r = 0
NOTr
                       r \leftarrow -r; N \leftarrow r < 0, Z \leftarrow r = 0, V \leftarrow \{overflow\}
NEGr
                       C \leftarrow r\langle 0 \rangle, r\langle 0...14 \rangle \leftarrow r\langle 1...15 \rangle, r\langle 15 \rangle \leftarrow 0; N \leftarrow r < 0, Z \leftarrow r = 0, V \leftarrow \{overflow\}
ASLr
                       C \leftarrow r\langle 15 \rangle, r\langle 1...15 \rangle \leftarrow r\langle 0...14 \rangle; N \leftarrow r < 0, Z \leftarrow r = 0
ASRr
                       C \leftarrow r\langle 0 \rangle, r\langle 0..14 \rangle \leftarrow r\langle 1..15 \rangle, r\langle 15 \rangle \leftarrow C
R0Lr
                       C \leftarrow r\langle 15 \rangle, r\langle 1..15 \rangle \leftarrow r\langle 0..14 \rangle, r\langle 0 \rangle \leftarrow C
RORr
N<sub>O</sub>P<sub>n</sub>
                       Trap: Unary no operation
                       Trap: Nonunary no operation
NOP
                       Trap: Oprnd \leftarrow \{decimal\ input\}
DECI
                       Trap: \{decimal\ output\} \leftarrow Oprnd
DEC0
                       Trap: \{string\ output\} \leftarrow Oprnd
STR0
                       byte Oprnd \leftarrow \{character\ input\}
CHARI
                        \{character\ output\} \leftarrow byte\ Oprnd
CHARO
                       SP \leftarrow SP + n ; PC \leftarrow Mem[SP] ; SP \leftarrow SP + 2
RETn
                       SP \leftarrow SP + Oprnd; N \leftarrow SP < 0, Z \leftarrow SP = 0, V \leftarrow \{overflow\}, C \leftarrow \{carry\}
ADDSP
                       SP \leftarrow SP - Oprnd; N \leftarrow SP < 0, Z \leftarrow SP = 0, V \leftarrow \{overflow\}, C \leftarrow \{carry\}
SUBSP
ADDr
                       r \leftarrow r + Oprnd; N \leftarrow r < 0, Z \leftarrow r = 0, V \leftarrow \{overflow\}, C \leftarrow \{carry\}
SUBr
                       r \leftarrow r - Oprnd; N \leftarrow r < 0, Z \leftarrow r = 0, V \leftarrow \{overflow\}, C \leftarrow \{carry\}
                       r \leftarrow r \land Oprnd; N \leftarrow r < 0, Z \leftarrow r = 0
ANDr
                       r \leftarrow r \lor Oprnd; N \leftarrow r < 0, Z \leftarrow r = 0
0Rr
                       T \leftarrow r - Oprnd; N \leftarrow T < 0, Z \leftarrow T = 0, V \leftarrow \{overflow\}, C \leftarrow \{carry\}
CPr
LDr
                       r \leftarrow Oprnd; N \leftarrow r < 0, Z \leftarrow r = 0
LDBYTEr
                       r(8..15) \leftarrow \text{byte Oprnd}; N \leftarrow r < 0, Z \leftarrow r = 0
STr
                       Oprnd \leftarrow r
STBYTEr
                       byte Oprnd \leftarrow r\langle 8..15 \rangle
                       T \leftarrow \text{Mem}[FFFA]; \text{Mem}[T-1] \leftarrow IR; \text{Mem}[T-3] \leftarrow SP;
Trap
                       Mem[T-5] \leftarrow PC ; Mem[T-7] \leftarrow X ; Mem[T-9] \leftarrow A ;
                       \text{Mem}[T-10]\langle 4...7 \rangle \leftarrow \text{NZVC}; \text{SP} \leftarrow T-10; \text{PC} \leftarrow \text{Mem}[\text{FFFE}]
```

NUL 000 0000 00 SP 010 0000 20 @ 100 0000 40 \ \cdot \text{110 0000 60} \\ SOH 000 0001 01 \text{!} 010 0001 21 \ A 100 0001 41 \ a 110 0001 61 \\ STX 000 0010 02 \ \cdot \text{!} 010 0010 22 \ B 100 0010 42 \ b 110 0010 62 \\ ETX 000 0011 03 \ \cdot \text{!} 010 0011 23 \ C 100 0011 43 \ c 110 0011 63 \\ EXT 000 0010 04 \ \cdot \cdot \text{!} 010 0011 23 \ C 100 0011 43 \ c 110 0010 64 \\ ENQ 000 0100 04 \ \cdot \cdot \text{!} 010 0010 24 \ D 100 0100 145 \ e 110 010 65 \\ ACK 000 0110 05 \ \cdot \cdot \text{!} 010 0101 25 \ E 100 0110 45 \ e 110 0110 65 \\ ACK 000 0110 06 \ \cdot \cdot \cdot \text{!} 010 011 27 \ G 100 0110 46 \ f 110 0110 66 \\ BEL 000 0111 07 \ \cdot \text{!} 010 0111 27 \ G 100 0111 47 \ g 110 0110 66 \\ HT 000 1001 09 \ \cdot \cdot \cdot \text{!} 010 100 29 \ I 100 1001 44 \ j 110 1001 69 \\ LF 000 1010 0A \ \cdot \cdot \text{!} 010 101 29 \ I 100 1001 44 \ j 110 1010 66 \\ TY 000 1010 0A \ \cdot \cdot \text{!} 010 1010 24 \ J 100 1010 44 \ j 110 1010 66 \\ TY 000 1010 0A \ \cdot \cdot \text{!} 010 1010 29 \ I 100 1001 49 \ i 110 1010 69 \\ LF 000 1010 0A \ \cdot \cdot \text{!} 010 1010 2A \ J 100 1010 4A \ j 110 1010 66 \\ CR 000 1110 0B \ \cdot \cdot \text{!} 010 1100 2C \ L 100 1100 4C \ I 110 1010 6C \\ CR 000 1110 0B \ \cdot \cdot \text{!} 010 1101 2D \ M 100 1101 4D \ m 110 110 6D \\ SO 000 1110 0B \ \cdot \cdot \text{!} 010 1111 2F \ N 100 1110 4B \ m 110 1101 6B \\ SI 000 1111 0F \ \sigma \text{!} 010 1111 2F \ \cdot \text{!} 100 1110 4B \ m 110 1101 6B \\ SI 000 1111 0F \ \sigma \text{!} 011 111 2F \ \cdot \text{!} 100 1110 55 \ \cdot \text{!} 111 0000 70 \\ DC1 001 0000 10 \(10 \text{!} \\ DLE 001 0000 10 12 2 2 011 0010 32 \ R 101 0010 52 \ r 111 0010 72 \\ DC2 001 0010 12 2 2 011 0010 33 \ R 101 0011 55 \ \text{!} 111 0010 75 \\ EXB 001 1100 16 \ A \ \text{!} \text{!} 110 101 35 \ \text{!} 111 101 07 \\ EXB 001 1010 16 \ A \ \text{!} 1110 101 35 \ \text{!} 111 101 70 \\ EXB 001 1	Char	Bin	Hex									
SOH 000 0001 01 ! 010 0001 21 A 100 0001 41 A 110 0001 61	NUL	000 0000	00	SP	010 0000	20	@	100 0000	40	`	110 0000	60
ETX 000 0010 03 # 010 0010 22	SOH	000 0001	01		010 0001	21	Α	100 0001	41	a	110 0001	61
EOT 000 0100 04	STX	000 0010	02	ıı .	010 0010	22	В	100 0010	42	b	110 0010	62
ENQ 000 0101 05	ETX	000 0011	03	#	010 0011	23	С	100 0011	43	С	110 0011	63
ACK 000 0110 06	EOT	000 0100	04	S	010 0100	24		100 0100	44	d	110 0100	64
BEL 000 0111 07 ' 010 0111 27 G 100 0111 47 g 110 0111 67 BS 000 1000 08 (010 1000 28 H 100 1000 48 h 110 1000 68 HT 000 1010 0A * 010 1010 2A J 100 1001 49 i 110 1001 69 LF 000 1010 0A * 010 1010 2A J 100 1010 4A j 110 1010 69 LF 000 1100 0C , 010 1101 2B K 100 1011 4B k 110 1010 60 CR 000 1100 OC , 010 1101 2D M 100 1101 4D m 110 1101 6B FF 000 1101 OD - 010 1101 2D M 100 1101 4D m 110 1110 6B SI 000 1111 OF		000 0101	05	%	010 0101			100 0101	45	е	110 0101	
BSC 000 1000 08 (010 100 28 H 100 1010 48 h 110 1000 68 HT 000 1010 09) 010 1001 29 I 100 1001 49 i 110 1001 69 LF 000 1010 0A * 010 1010 2A J 100 1010 4A j 110 1010 6A VT 000 1011 0B + 010 1011 2B K 100 1011 4B K 110 1011 6B FF 000 1100 0C , 010 1100 2C L 100 1100 4C I 110 1101 6B FF 000 1101 0D - 010 1101 2D M 100 1101 4D m 110 1101 6D SO 000 1110 0E . 010 1110 2E N 100 1110 4E n 110 1101 6E SI 000 1111 0F / 010 1111 2F 0 100 1111 4F 0 110 1111 6F DLE 01 0000 10 0 0 01 10000 30 P 101 0000 50 P 111 0000 70 DC1 001 0001 11 1 01 0000 31 Q 10 10000 51 Q 111 0000 71 DC2 001 001 001 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 001 13 3 01 0011 33 S 101 0011 53 S 111 0011 73 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0110 35 U 101 0100 55 V 111 0100 75 SYN 001 0110 16 6 011 0110 36 V 101 0100 5A T 111 0100 78 EM 001 1001 17 T CAN 001 1000 18 8 011 1000 38 X 101 0011 57 W 111 0110 75 SYN 001 1001 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 78 EM 001 1001 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 78 EM 001 1001 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 78 EM 001 1001 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 78 EM 001 1010 1A : 011 1010 3B [101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1010 5C] 111 1100 7C GS 001 1101 1D = 011 1101 3B [101 1010 5D] 111 1101 7D RS 001 1110 1E > 011 1110 3E ^ 101 1110 5E ^ 111 1110 7D	ACK	000 0110	06	&	010 0110	26	F	100 0110	46	f	110 0110	66
HT 000 1001 09	BEL	000 0111	07	'	010 0111	27	G	100 0111	47	g	110 0111	67
LF 000 1010 0A	BS	000 1000	08	(010 1000	28	Н		48	h	110 1000	68
VT 000 1010 0A	HT	000 1001	09	, ,	010 1001	29	1	100 1001	49	i	110 1001	69
FF 000 1100 0C , 010 1100 2C L 100 1100 4C l 1110 1100 6C CR 000 1101 0D - 010 1101 2D M 100 1101 4D m 110 1101 6D SO 000 1110 0E . 010 1110 2E N 100 1110 4E n 110 1101 6E SI 000 1111 0F / 010 1111 2F 0 100 1111 4F 0 110 1111 6F DLE 001 0000 10 0 011 0000 30 P 101 0000 50 p 111 0000 70 DC1 001 0001 11 1 011 0001 31 Q 101 0000 51 q 111 0001 71 DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0011 13 3 011 0011 33 S 101 0011 53 s 111 0011 73 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 U 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0101 55 U 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0101 55 U 111 0101 75 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0111 77 CAN 001 1000 18 8 011 1000 38 X 101 1001 59 Y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1000 78 EM 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1010 3C \ 101 1100 5C \ 111 1100 5C \ 111 1100 7C GS 001 1101 1D = 011 1101 3D \ 1 101 1100 5C \ 111 1110 7D RS 001 1110 1E > 011 1110 3E ^ 101 1110 5D } 111 1110 7D	LF	000 1010	0A	*	010 1010	2A	J	100 1010	4A	j	110 1010	6A
CR 000 1101 0D - 010 1101 2D M 100 1101 4D m 110 1101 6D SO 000 1110 0E . 010 1110 2E N 100 1110 4E n 110 1110 6E SI 000 1111 0F / 010 1111 2F 0 100 1111 4F 0 110 1111 6F DLE 001 0000 10 0 011 0000 30 P 101 0000 50 p 111 0000 70 DC1 001 0001 11 1 011 0001 31 Q 101 0001 51 Q 111 0001 71 DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0011 13 3 011 0011 33 S 101 0011 53 S 111 0011 73 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 U 111 010 75 SYN 001 0110 16 6 011 0110 36 V 101 0101 55 U 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0101 57 W 111 0111 77 CAN 001 1000 18 8 011 1000 38 X 101 1001 59 Y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1010 5C	VT	000 1011	0B	+	010 1011	2B	K	100 1011	4B	k	110 1011	6B
SO 000 1110 0E . 010 1110 2E N 100 1110 4E n 110 1110 6E SI 000 1111 0F / 010 1111 2F 0 100 1110 4E n 110 1110 6E DLE 001 0000 10 0 011 0000 30 P 101 0000 50 p 111 0000 70 DC1 001 0001 11 1 011 0001 31 Q 101 0001 51 q 111 0001 71 DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0101 13 3 011 0011 33 S 101 0011 53 s 111 0010 72 DC3 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0101 74 NAK 001 0101 15	FF	000 1100	0C	,	010 1100	2C	L	100 1100	4C	1	110 1100	6C
SI 000 1111 OF / 010 1111 2F O 100 1111 4F O 110 1111 6F DLE 001 0000 10 0 011 0000 30 P 101 0000 50 p 111 0000 70 DC1 001 0010 11 1 011 0001 31 Q 101 0001 51 q 111 0001 71 DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0011 13 3 011 0011 33 S 101 0011 53 s 111 0010 72 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 76 ETB 001 0111 17	CR	000 1101	0D	-	010 1101	2D	M	100 1101	4D	m	110 1101	6D
DLE 001 0000 10 0 011 0000 30 P 101 0000 50 p 111 0000 70 DC1 001 0001 11 1 011 0001 31 Q 101 0001 51 q 111 0001 71 DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0011 13 3 011 0011 33 S 101 0011 53 s 111 0010 72 DC3 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 75 SYN 001 0101 16 6 011 0110 36 V 101 0101 56 V 111 0110 76 ETB 001 0100 18	SO	000 1110	0E		010 1110	2E	N	100 1110	4E	n	110 1110	6E
DC1 001 0001 11	SI	000 1111	0F	/	010 1111	2F	0	100 1111	4F	0	110 1111	6F
DC2 001 0010 12 2 011 0010 32 R 101 0010 52 r 111 0010 72 DC3 001 0011 13 3 011 0011 33 S 101 0011 53 S 111 0010 72 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0110 56 V 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0101 76 EM 001 1000 18 8 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A	DLE	001 0000	10	0	011 0000	30		101 0000	50	р	111 0000	70
DC3 001 0011 13 3 011 0011 33 S 101 0011 53 s 111 0011 73 DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0110 56 V 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0101 76 EM 001 1000 18 8 011 1000 38 X 101 1000 58 X 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 5A z 111 1001 7A ESC 001 1011 1B	DC1	001 0001	11		011 0001	31		101 0001		q	111 0001	
DC4 001 0100 14 4 011 0100 34 T 101 0100 54 t 111 0100 74 NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0110 56 V 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0111 77 CAN 001 1000 18 8 011 1000 38 X 101 1000 58 x 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A z 111 1010 7A ESC 001 1011 1B	DC2	001 0010	12	2	011 0010	32		101 0010	52	r	111 0010	72
NAK 001 0101 15 5 011 0101 35 U 101 0101 55 u 111 0101 75 SYN 001 0110 16 6 011 0110 36 V 101 0110 56 V 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0111 77 CAN 001 1000 18 8 011 1000 38 X 101 1000 58 X 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1010 5C 111 1100 7C GS 001 1101 1D	DC3	001 0011	13	3	011 0011	33	S	101 0011	53	S	111 0011	73
SYN 001 0110 16 6 011 0110 36 V 101 0110 56 V 111 0110 76 ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0110 76 CAN 001 1000 18 8 011 1000 38 X 101 1000 58 X 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 101 1B ; 011 101 3B [101 101 5B { 111 1101 7B FS 001 1100 1C <	DC4	001 0100	14	4	011 0100	34	T	101 0100	54	t	111 0100	74
ETB 001 0111 17 7 011 0111 37 W 101 0111 57 W 111 0111 77 CAN 001 1000 18 8 011 1000 38 X 101 1000 58 X 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 59 Y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1011 5B { 111 1011 7B} FS 001 1100 1C < 011 1100 3C \ 101 1100 5C 111 1100 7C GS 001 1101 1D = 011 1101 3D] 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E	NAK	001 0101	15	5	011 0101	35	U	101 0101	55	u	111 0101	75
CAN 001 1000 18 8 011 1000 38 X 101 1000 58 x 111 1000 78 EM 001 1001 19 9 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1011 5B { 111 1011 7B } FS 001 1100 1C < 011 1100 3C \ 101 1100 5C 111 1100 7C GS 001 1101 1D = 011 1101 3D] 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E 101 1110 5E ~ 111 1110 7E	SYN	001 0110	16	6	011 0110	36	V	101 0110	56	V	111 0110	76
EM 001 1001 19 9 011 1001 39 Y 101 1001 59 y 111 1001 79 SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1011 5B { 111 1011 7B FS 001 1100 1C <	ETB	001 0111	17	7	011 0111	37	W	101 0111	57	W	111 0111	77
SUB 001 1010 1A : 011 1010 3A Z 101 1010 5A Z 111 1010 7A ESC 001 1011 1B ; 011 1011 3B [101 1011 5B { 111 1010 7A FS 001 1100 1C 011 1100 3C \ 101 1100 5C 111 1100 7C GS 001 1101 1D = 011 1101 3D] 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E ^ 101 1110 5E ~ 111 1110 7E	CAN	001 1000	18	8	011 1000	38	Χ	101 1000	58	Х	111 1000	78
ESC 001 1011 1B ; 011 1011 3B [101 1011 5B { 111 1011 7B } FS 001 1100 1C < 011 1100 3C \ 101 1100 5C 111 1100 7C GS 001 1101 1D = 011 1101 3D 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E	EM	001 1001	19	9	011 1001	39		101 1001	59	у	111 1001	79
FS 001 1100 1C < 011 1100 3C \ 101 1100 5C 111 1100 7C GS 001 1101 1D = 011 1101 3D 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E	SUB	001 1010	1A	:	011 1010	3A	Z	101 1010	5A	Z	111 1010	7A
GS 001 1101 1D = 011 1101 3D] 101 1101 5D } 111 1101 7D RS 001 1110 1E > 011 1110 3E	ESC	001 1011	1B	;	011 1011	3B	[101 1011	5B	{	111 1011	7B
RS 001 1110 1E > 011 1110 3E 101 1110 5E ~ 111 1110 7E	FS	001 1100	1C	<	011 1100	3C	\	101 1100	5C		111 1100	7C
RS 001 1110 1E > 011 1110 3E	GS	001 1101	1D	=	011 1101	3D]	101 1101	5D	}	111 1101	7D
US 001 1111 1E 2 011 1111 3E 101 1111 5E DEI 111 1111 7E	RS	001 1110	1E	>	011 1110	3E	^	101 1110	5E	~	111 1110	7E
OS COLLIN II : COLLIN SI _ LOCALIN SI DEL III III /I	US	001 1111	1F	?	011 1111	3F	_	101 1111	5F	DEL	111 1111	7F

Abbreviations for Control Characters

SOH STX	null, or all zeros start of heading start of text end of text	FF CR SO SI	form feed carriage return shift out shift in	CAN EM SUB ESC	cancel end of medium substitute escape
ENQ	end of transmission enquiry acknowledge bell	DC1 DC2	data link escape device control 1 device control 2 device control 3	FS GS RS US	file separator group separator record separator unit separator
BS HT LF VT	backspace horizontal tabulation line feed vertical tabulation	NAK SYN	device control 4 negative acknowledge synchronous idle end of transmission block	SP DEL	space delete