CDA 4213/CIS 6930 CMOS VLSI
Fall 2022

Final Project

Today's Date:	12/1/2022
Your Team Name	*Team Tesla*
Team Members	Jaylen Brown (U53294015)
No. of Hours Spent:	50 hours
Exercise Difficulty: (Easy, Average, Hard)	Average

(1) **Proposed Design – Bit slice design**

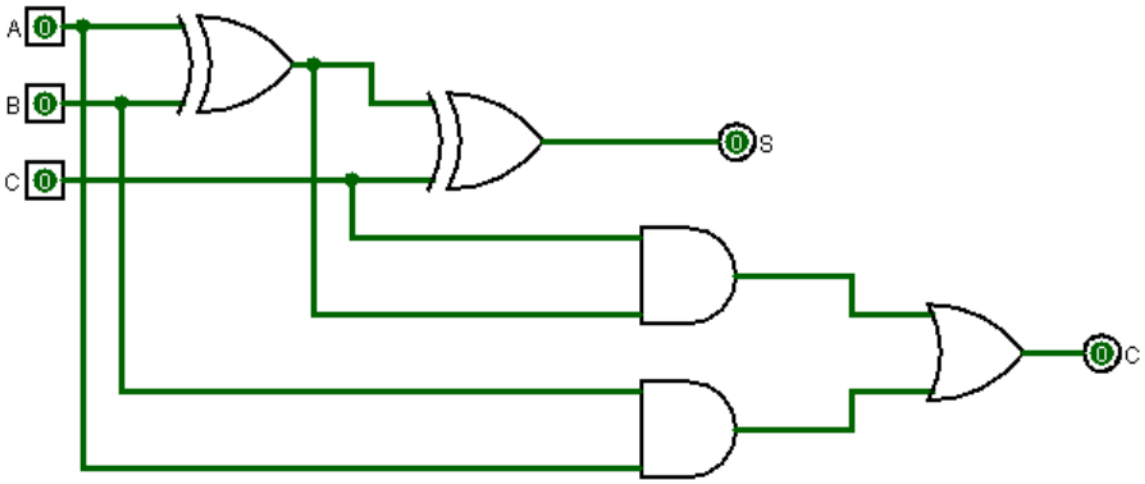
(a) **List all module bit-slices you have used for your design.**

I. Full Adder:
II. Full Adder with AND gate:
III. Serial In Parallel Out Shift Register
IV. Parallel In Series Out Shift Register With MUX
V. MUX

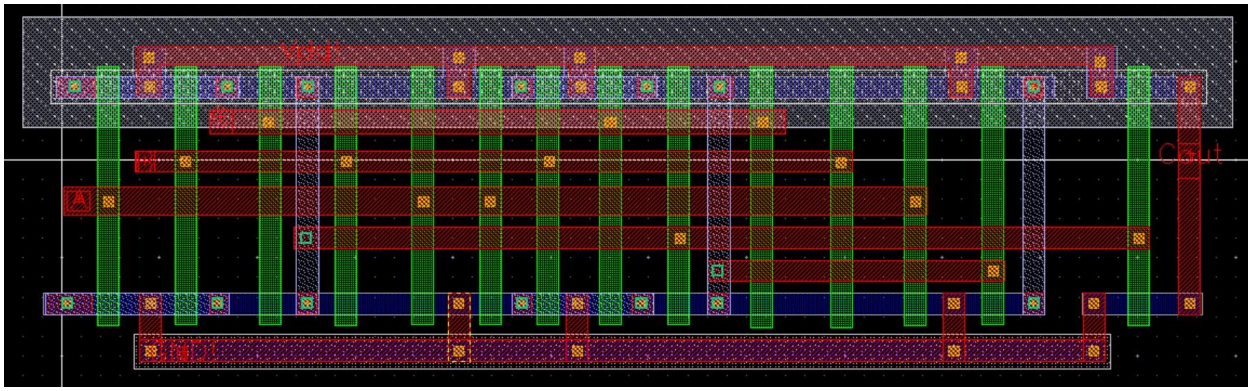
(b) **For each bit slice, show the gate-level design and layout design:**

I. Full Adder:

a. Gate-Level Design

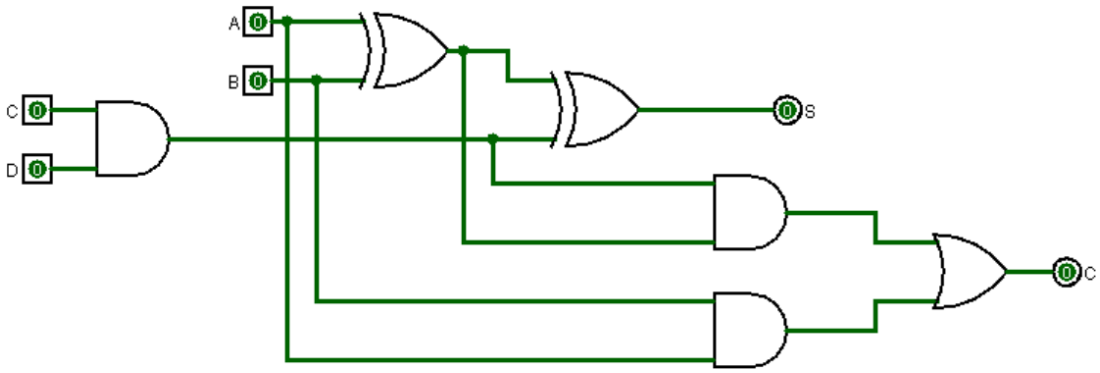


b. Layout Design

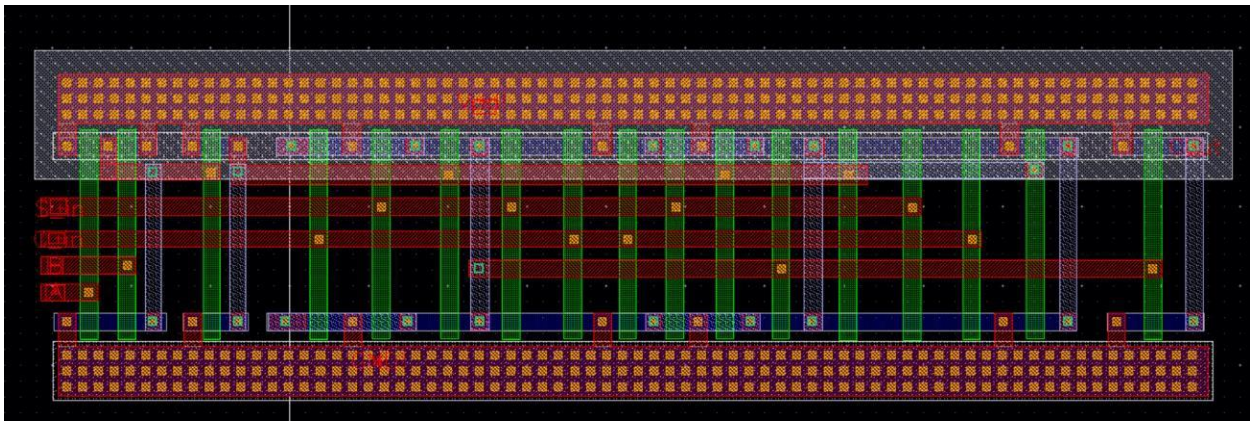


II. Full Adder with AND gate:

a. Gate-Level Design

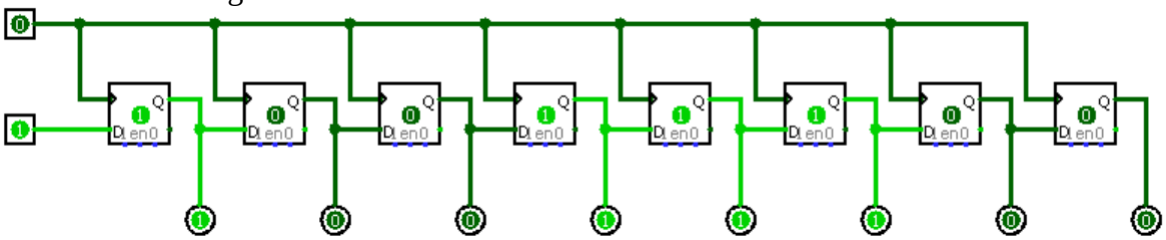


b. Layout Design

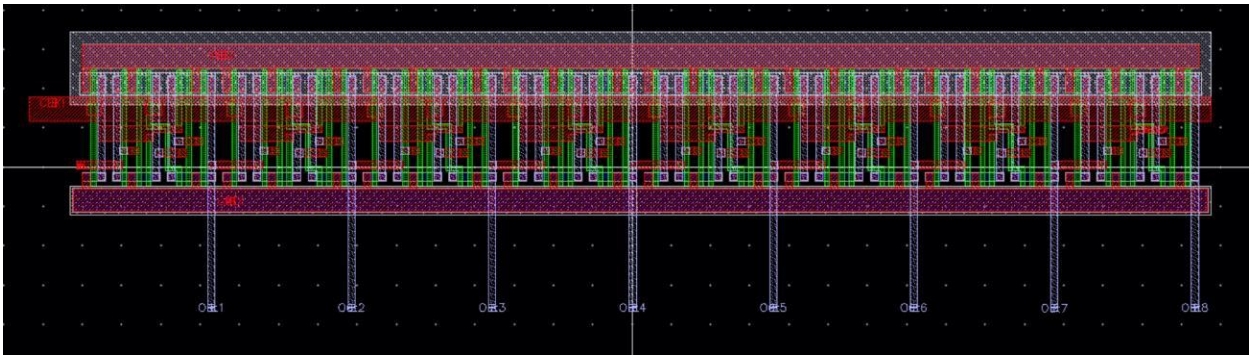


III. Serial In Parallel Out Shift Register

a. Gate-Level Design

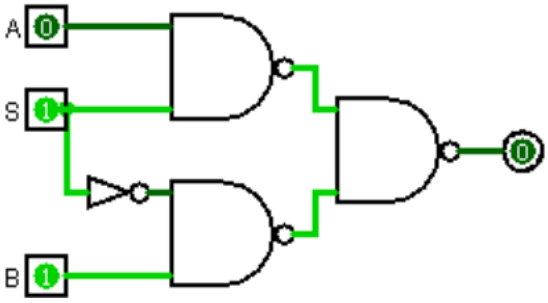


b. Layout Design

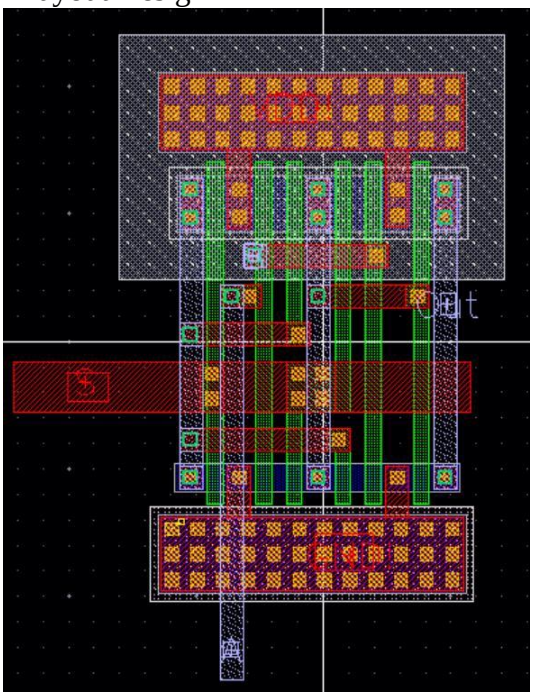


IV. MUX

a. Gate-Level Design



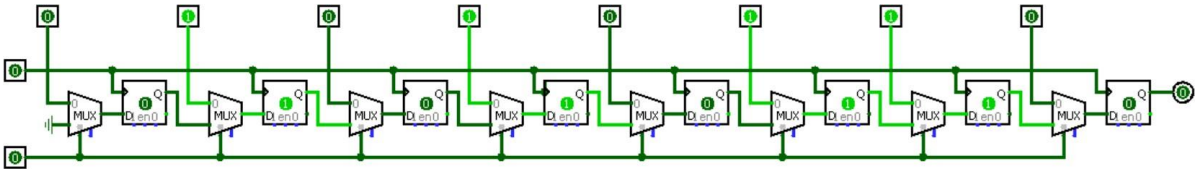
b. Layout Design



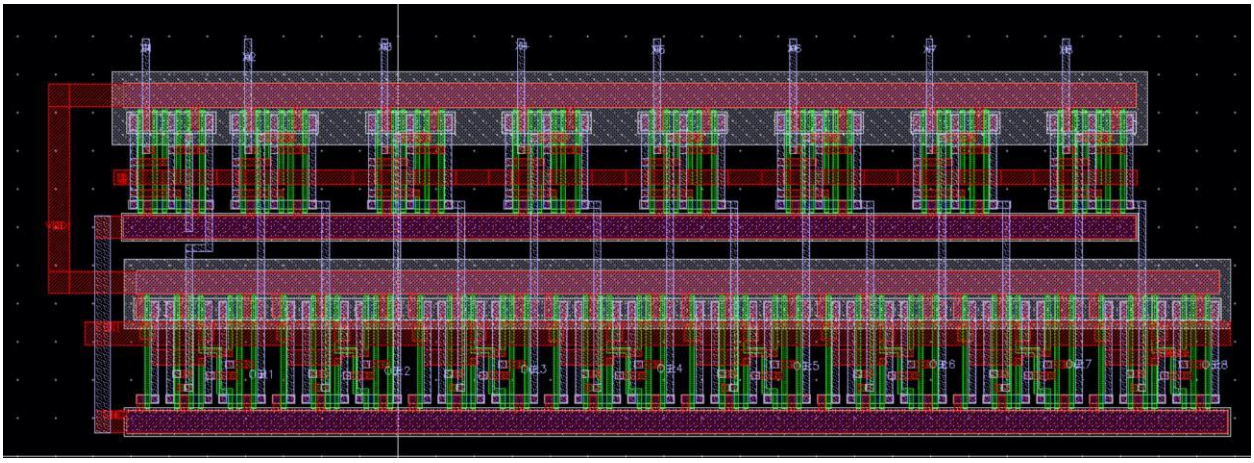
V. Parallel In Series Out Shift Register With MUX

a. Gate-Level Design

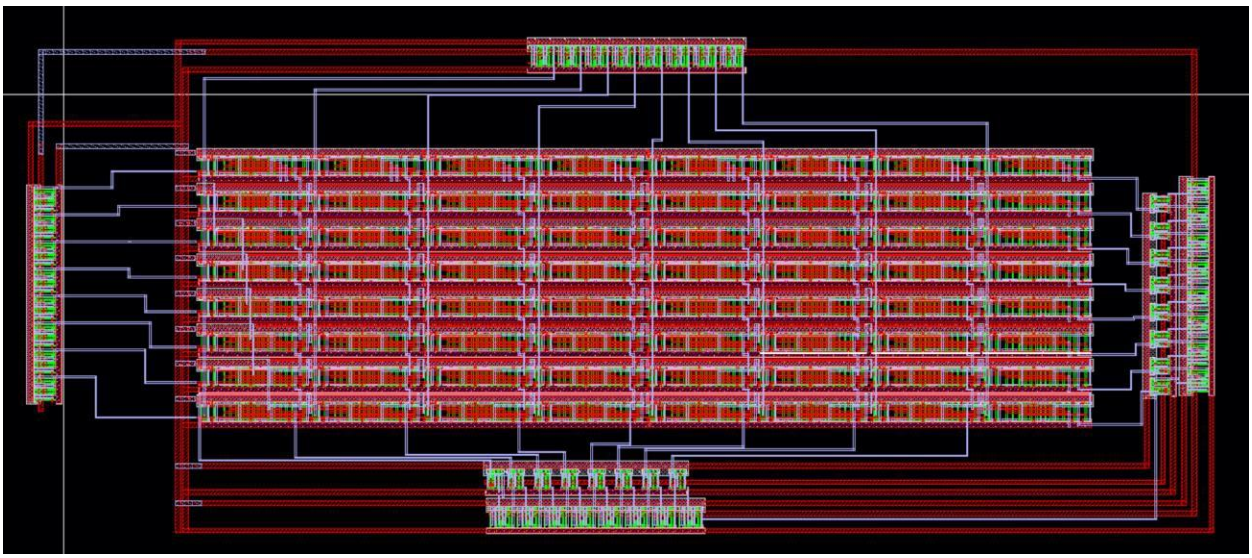
b.



c. Layout Design



(2) **Show the layout of your multiplier with the registers (outside the padframe). Explain the design and functionality of your multiplier.**

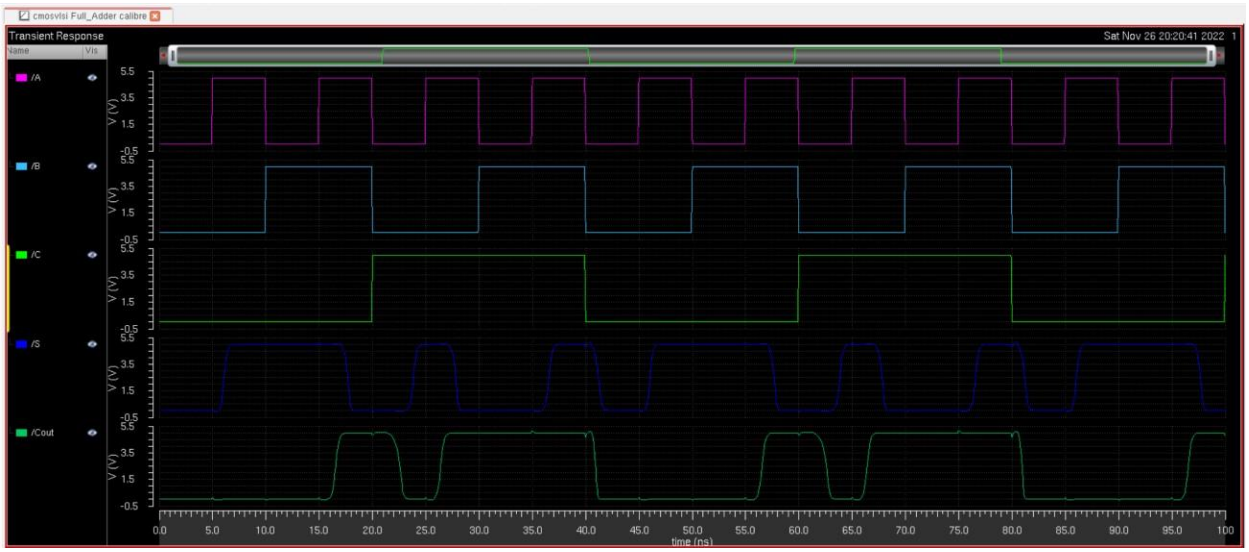


The functionality for the 8x8 multiplier starts with the two SIPO registers located on the top and left side of the design. These SIPO registers represent the X and Y inputs that will get sent through the multiplier. Once all the X and Y inputs get pushed serially, they will be pushed out parallel to the multiplier. Once multiplier finishes calculating the result, the two PISO registers will come in to first take in the result parallelly, then second the MUX will switch from parallel input to serial input so that we can push out the multiplicand result serially from the PISO's giving a 16-bit result.

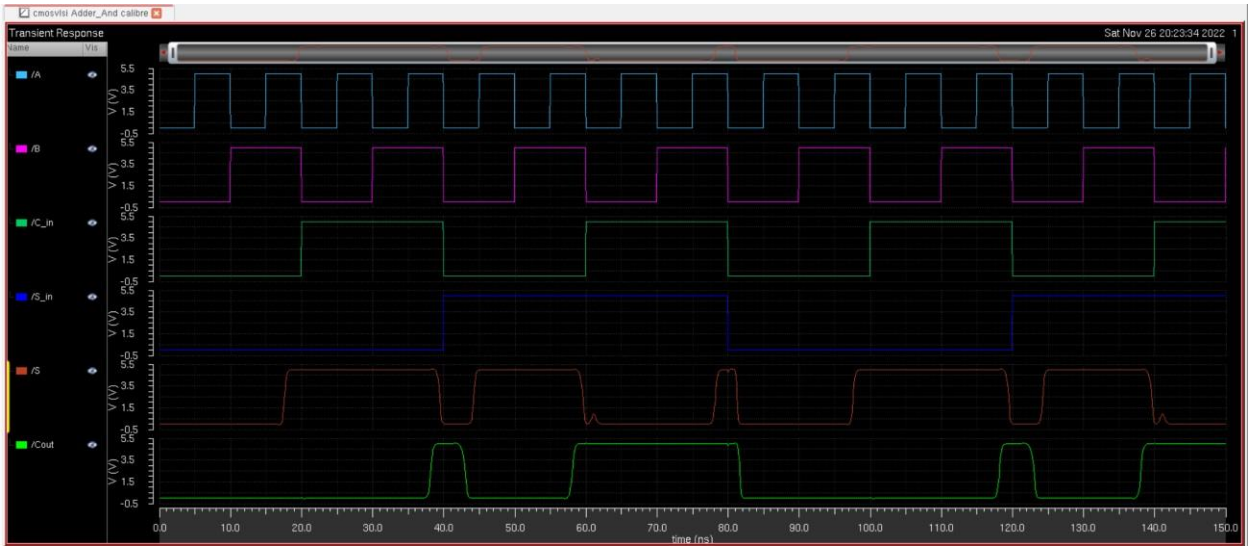
(3) **Simulation Results (without pad frame):**

(a) (5 pts total) Individual cells:

I. Full Adder:

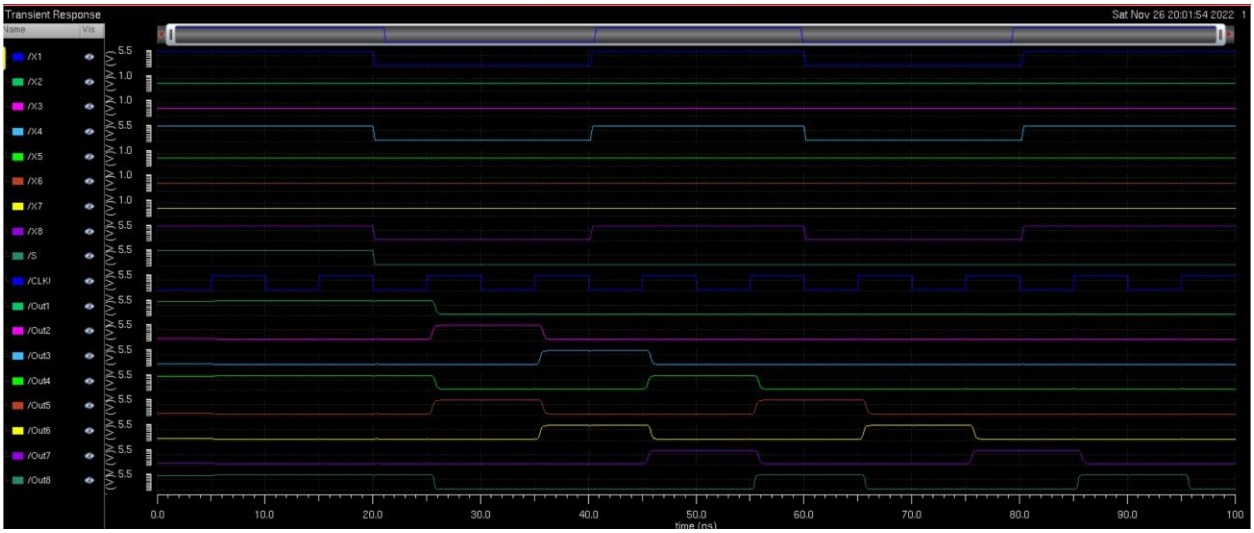


II. Full Adder with AND gate:

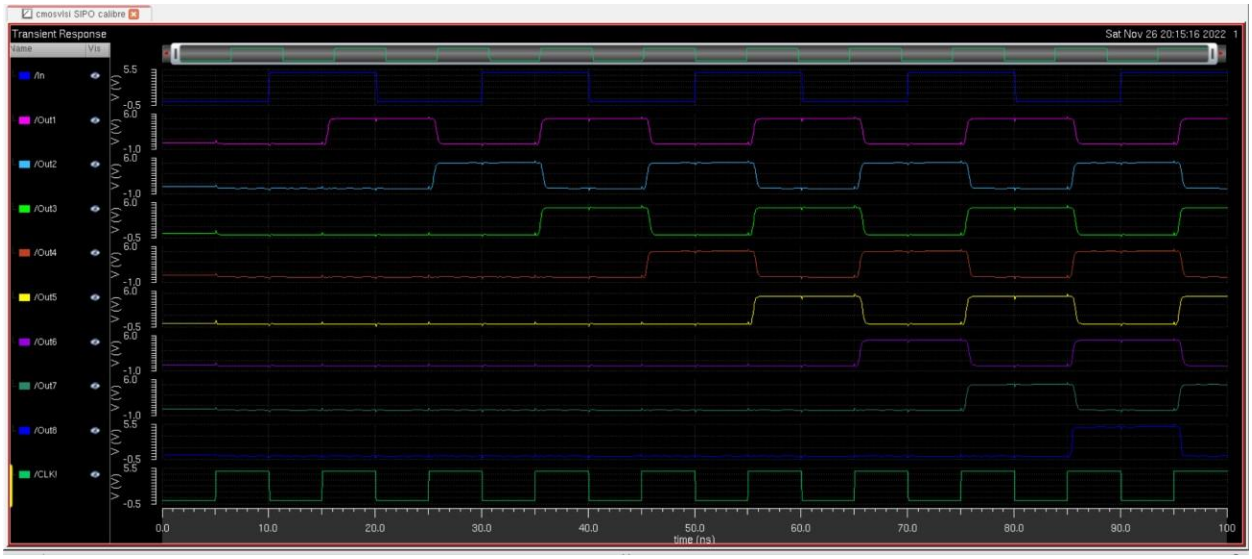


III. Registers (Test Mode):

i. PISO



ii. SIPO

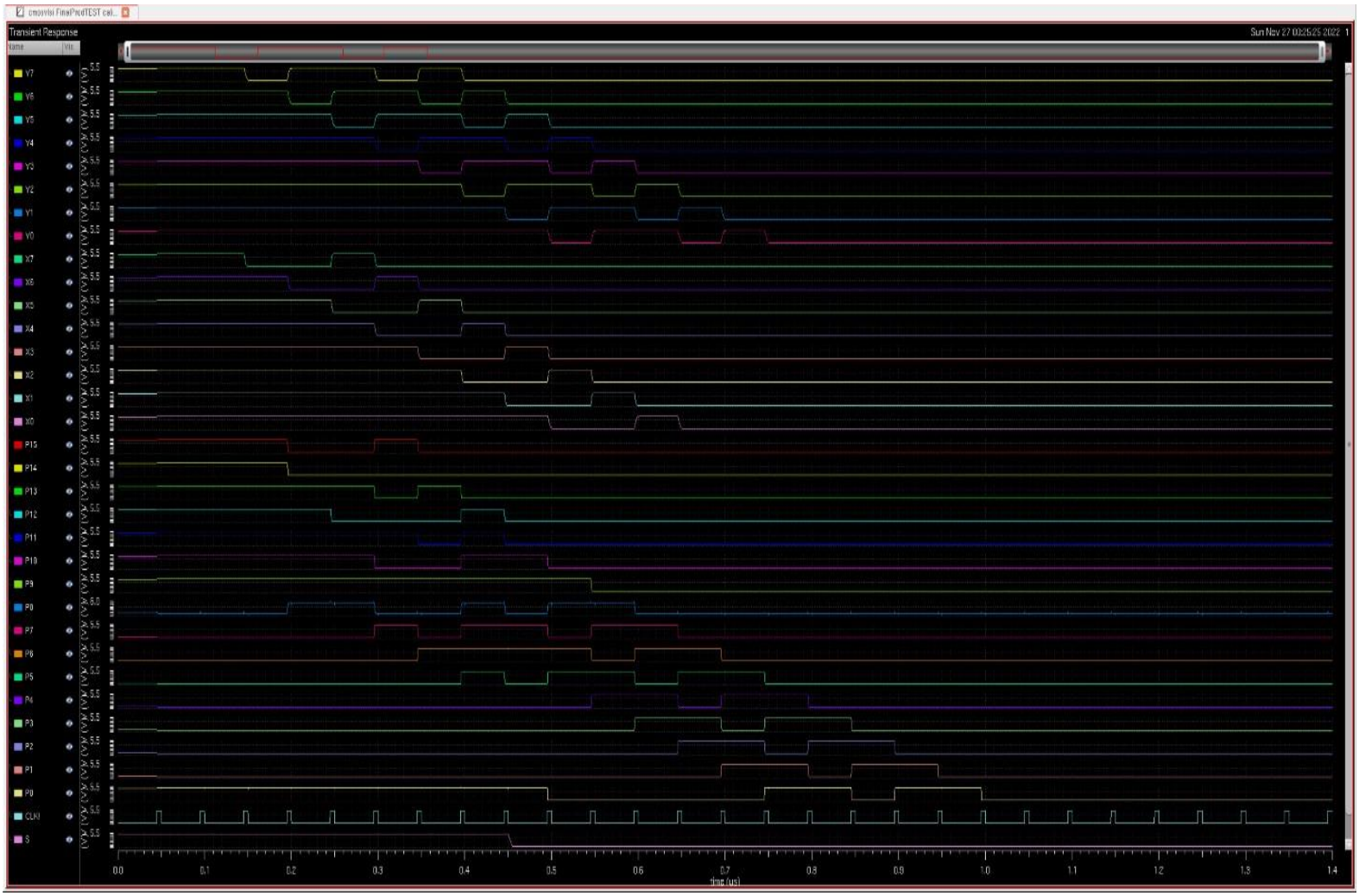


IV. Ring Oscillator (If used):

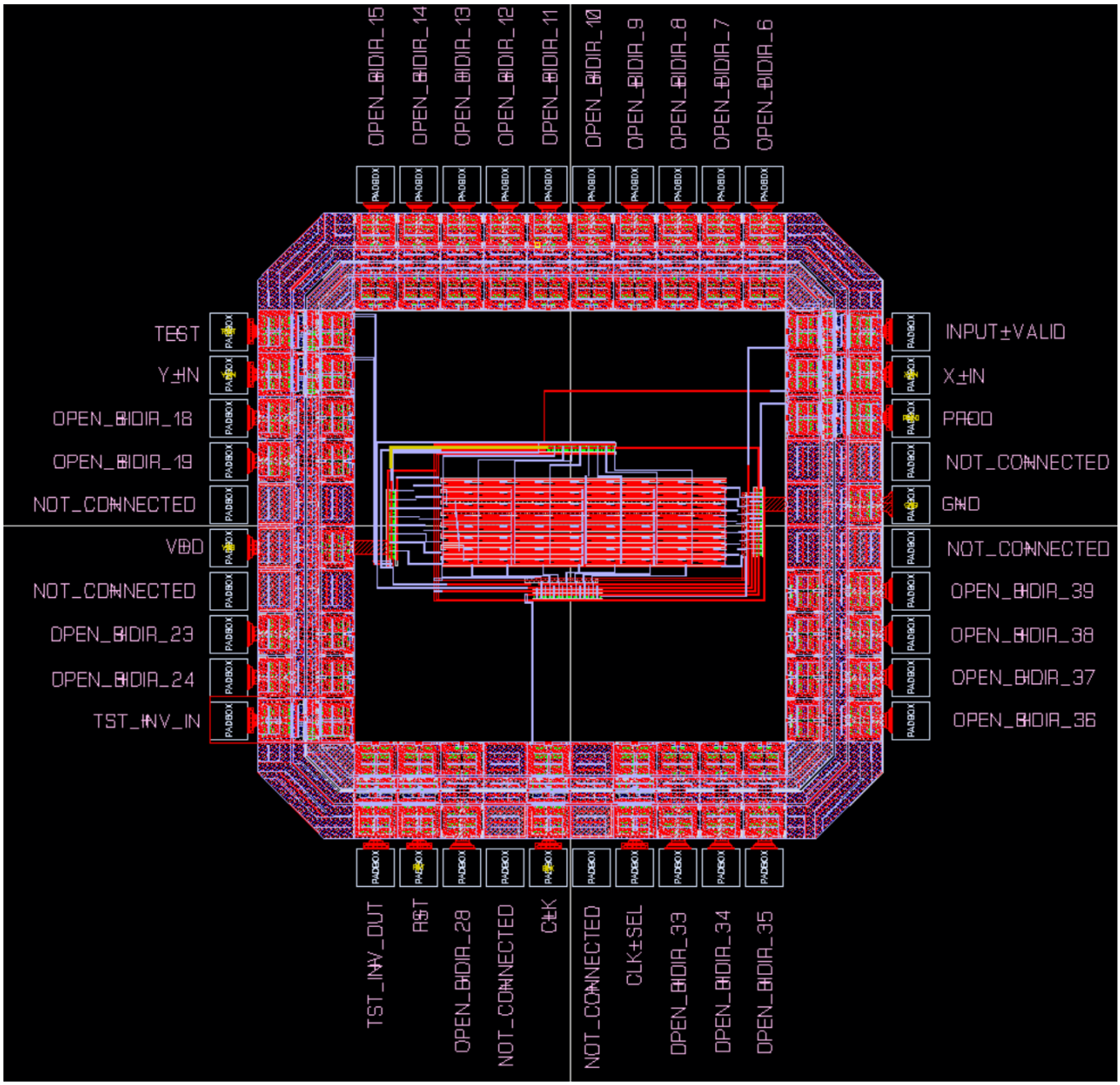
NOT USED

(b) (20 pts) The final multiplier:

Test 5) 19 x 91 = 1729 (00010011 x 01011011 = 0000011011000001)



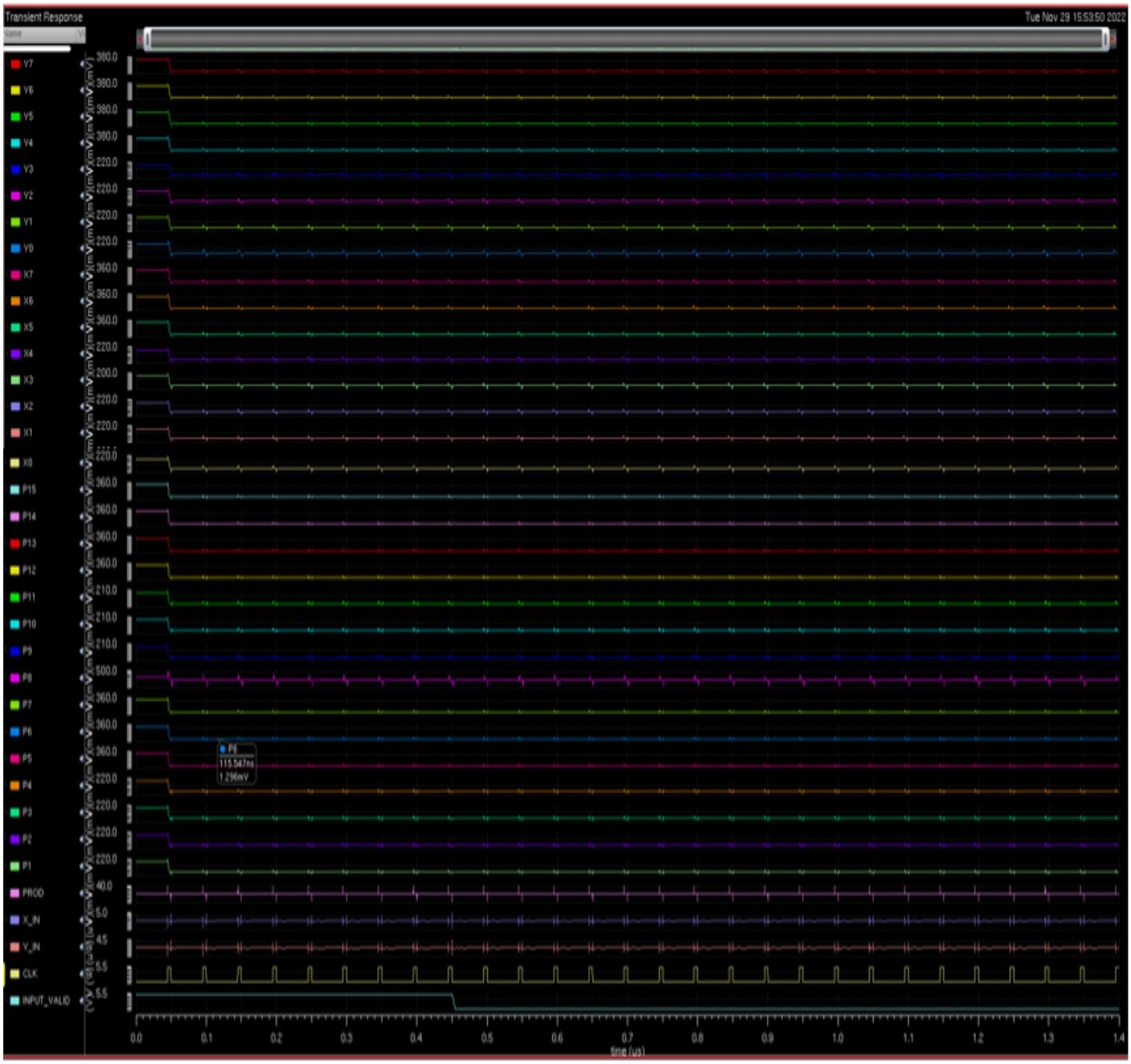
(4) **Layout of the final design (with pad frame):**



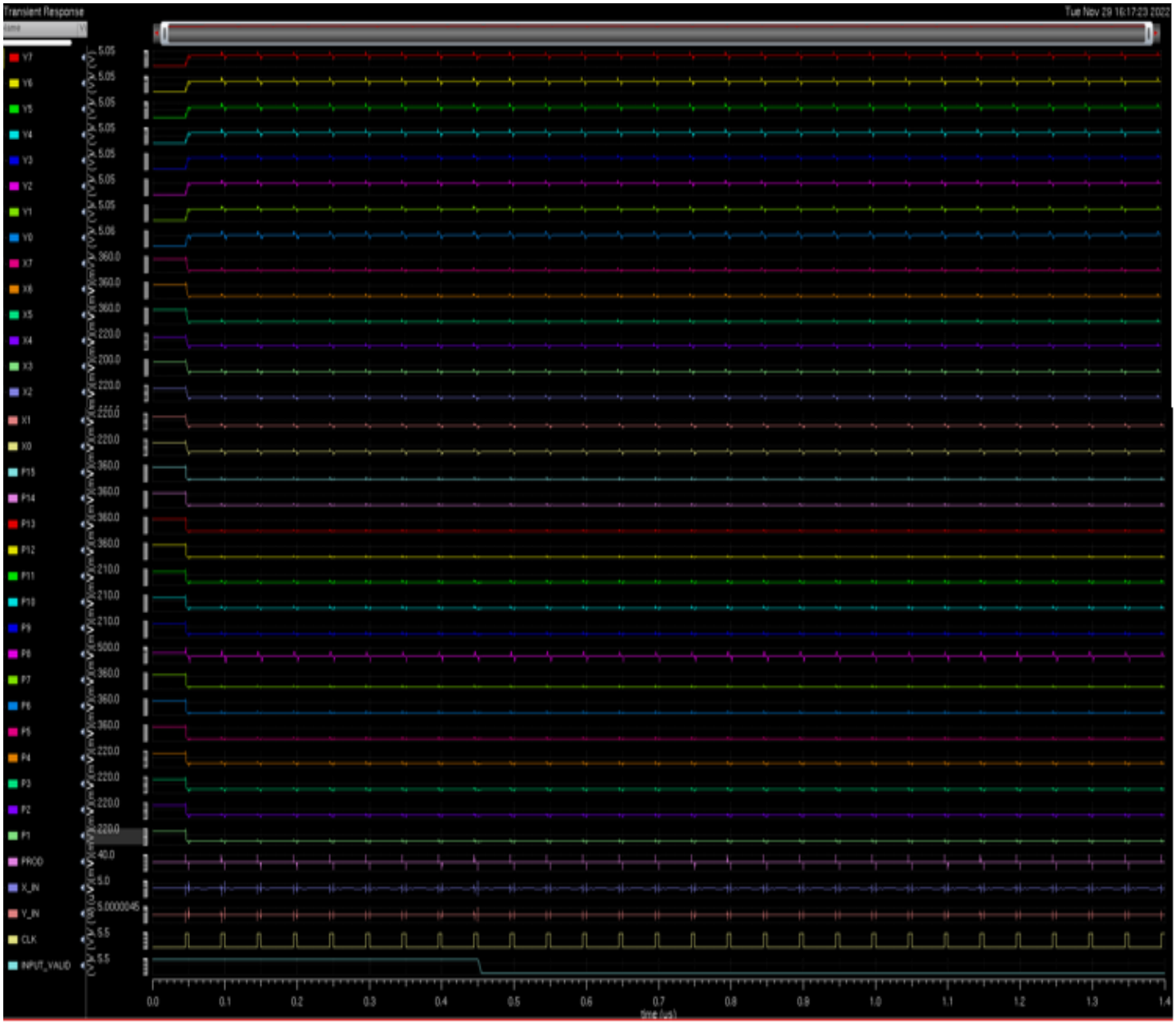
(5) **Simulation waveforms for the final design (with pad frame):**

For 8 x 8 multiplier
With the pad frame

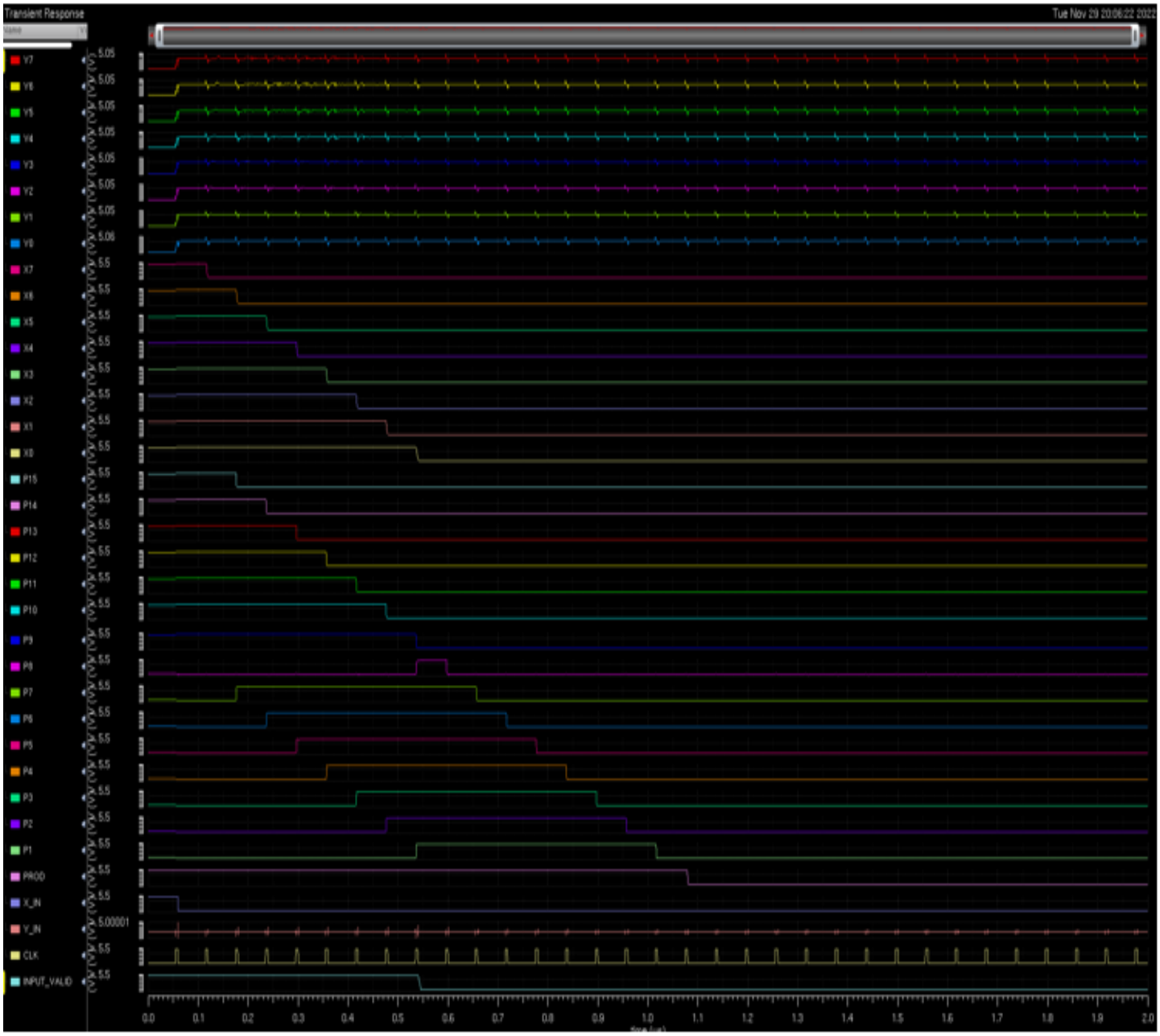
1)0 x 0 = 0



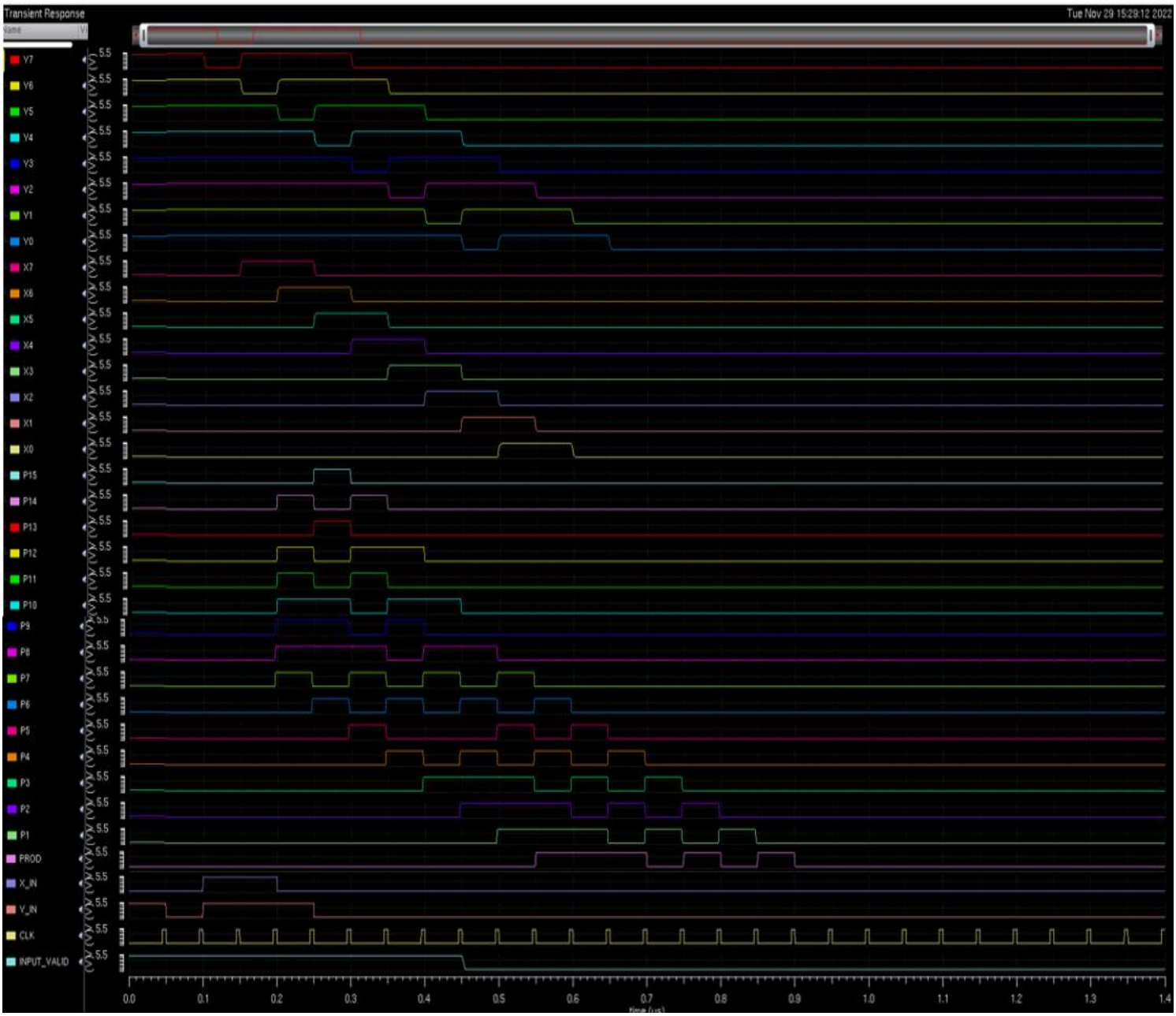
2)0 x 255 = 0


Transient Response
Tue Nov 29 16:17:23 2022
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
X7
X6
X5
X4
X3
X2
X1
X0
P15
P14
P13
P12
P11
P10
P9
P8
P7
P6
P5
P4
P3
P2
P1
PROD
X_IN
Y_IN
CLK
INPUT_VALID
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4

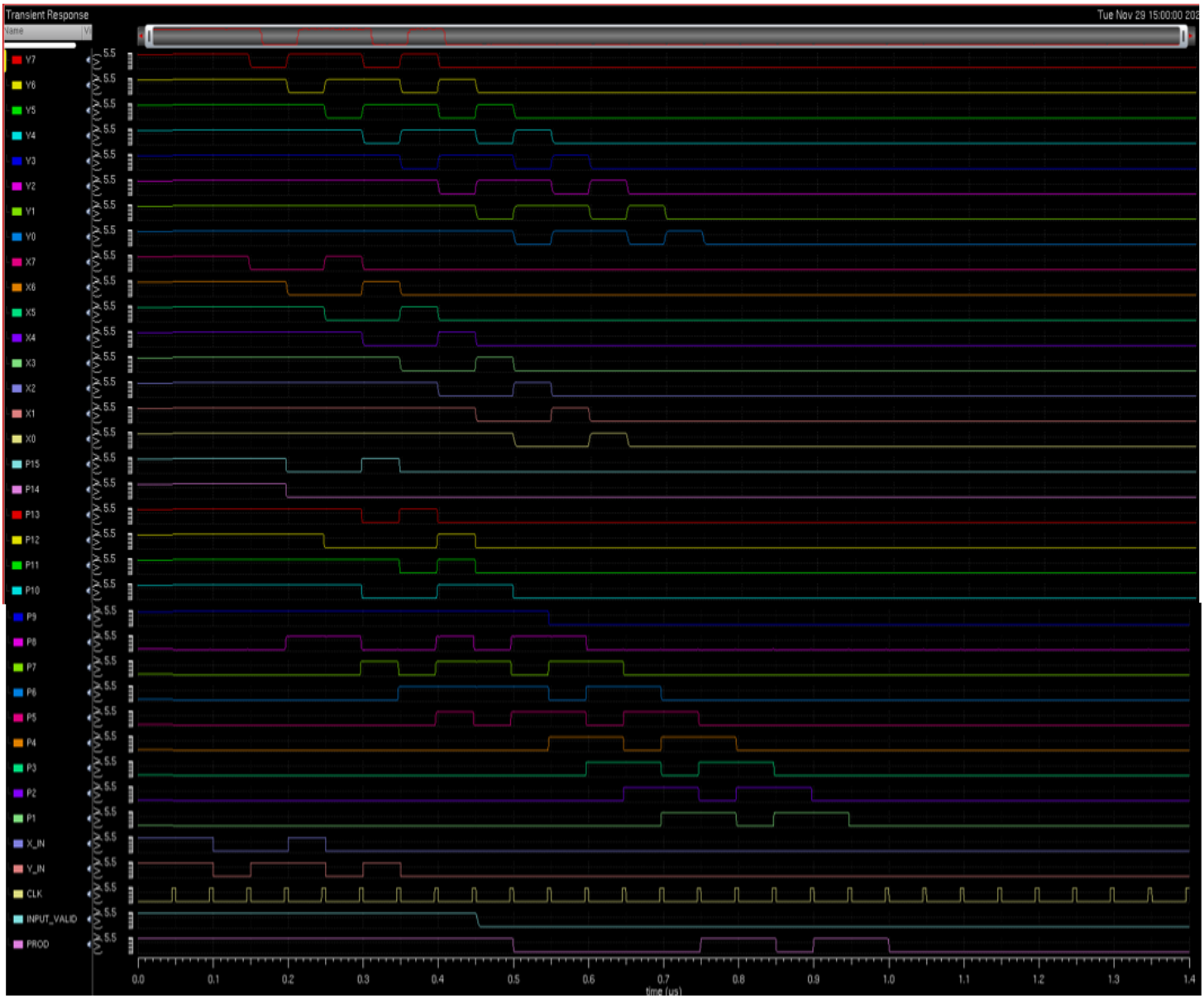
3)1 x 255 = 255 (00000001 x 11111111 = 0000000011111111)



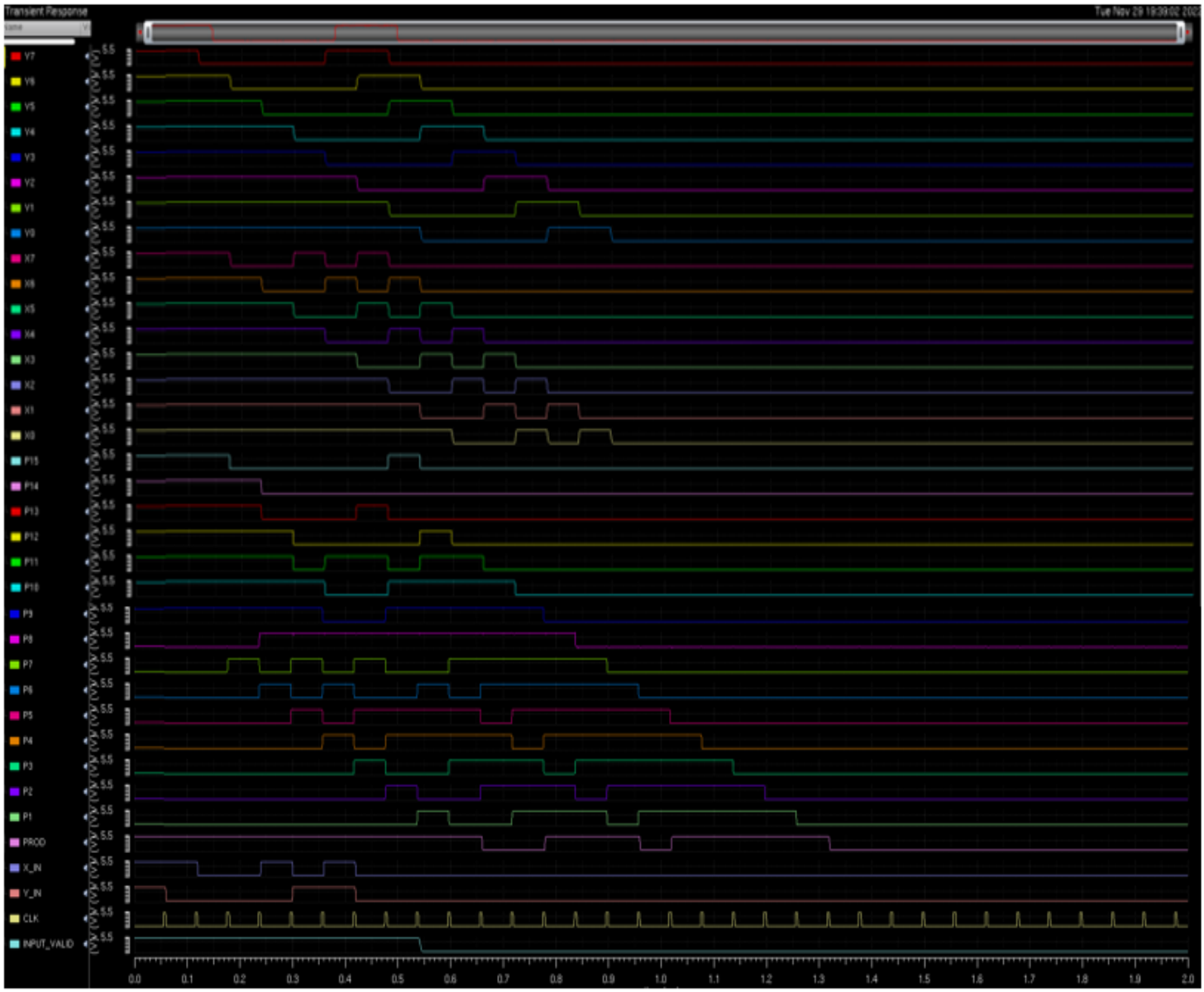
4)12 x 29 = 348 (00001100 x 00011101 = 0000000101011100)



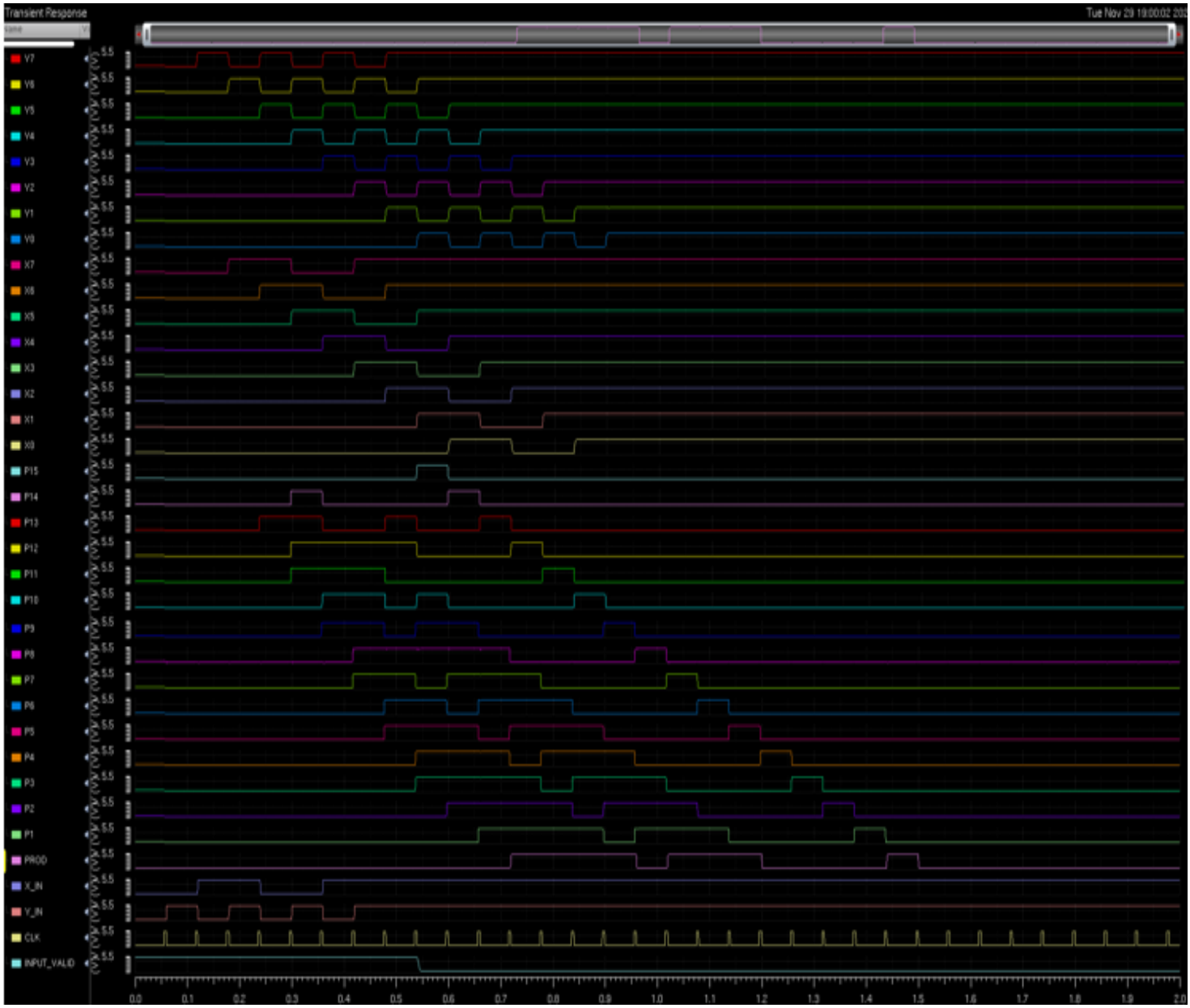
5)19 x 91 = 1729 (00010011 x 01011011 = 0000011011000001) ** Taxicab number



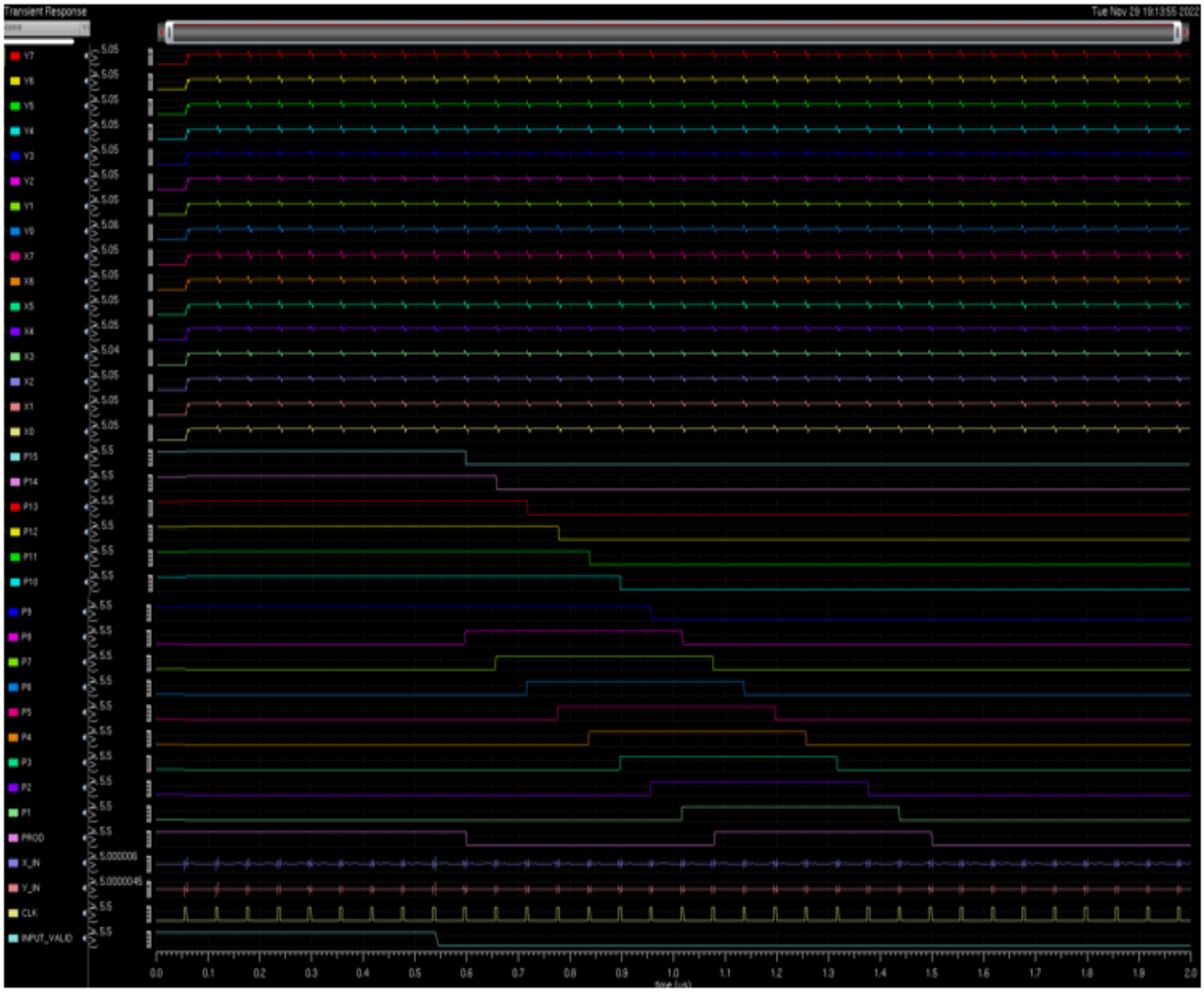
6) 83 x 97 = 8051 (01010011 x 01100001 = 0001111101110011)



7) 170 x 204 = 34680 (10101010 x 11001100 = 1000011101111000)

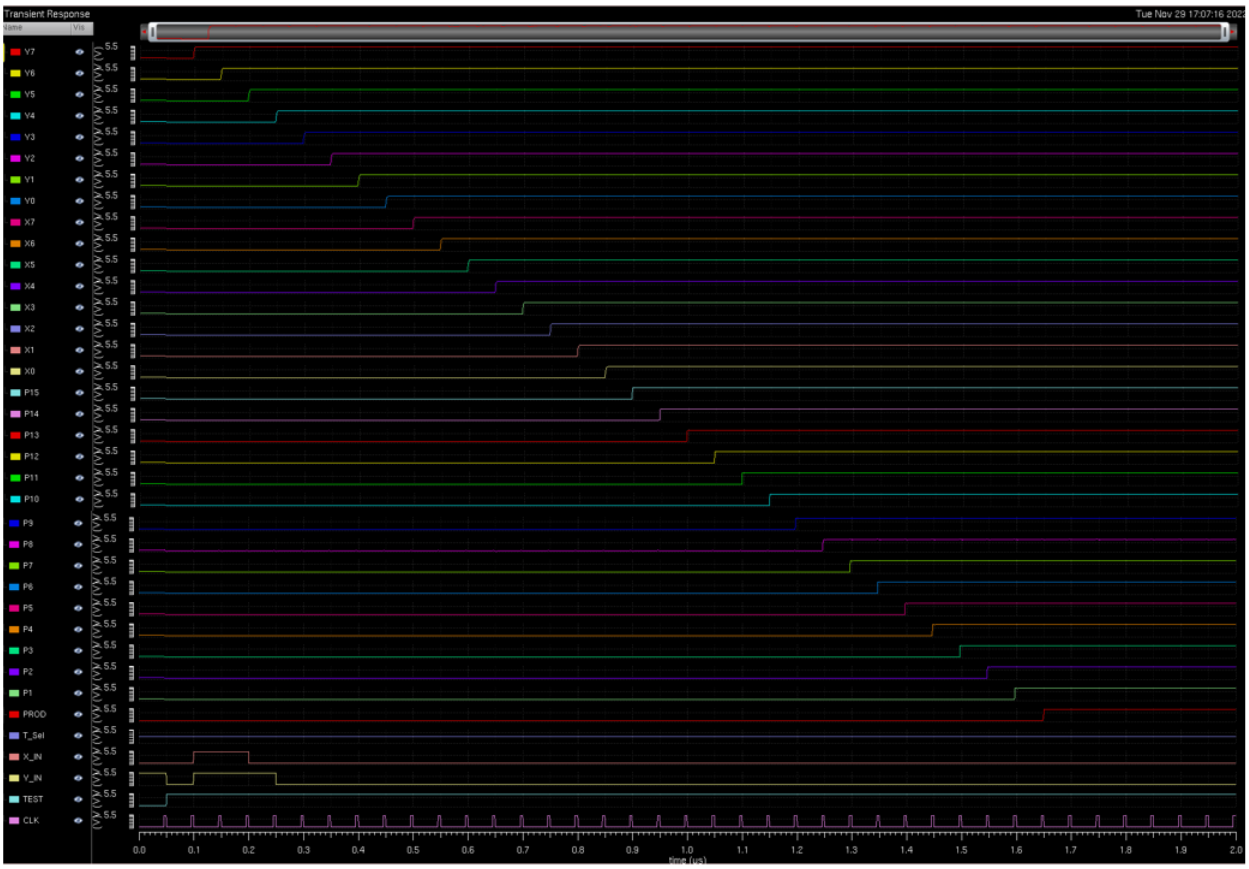


8) 255 x 255 = 65025 (11111111 x 11111111 = 1111111000000001)



TEST MODE

1) all 1's GOOD



2) alternating 0's and 1's i.e., 010101...