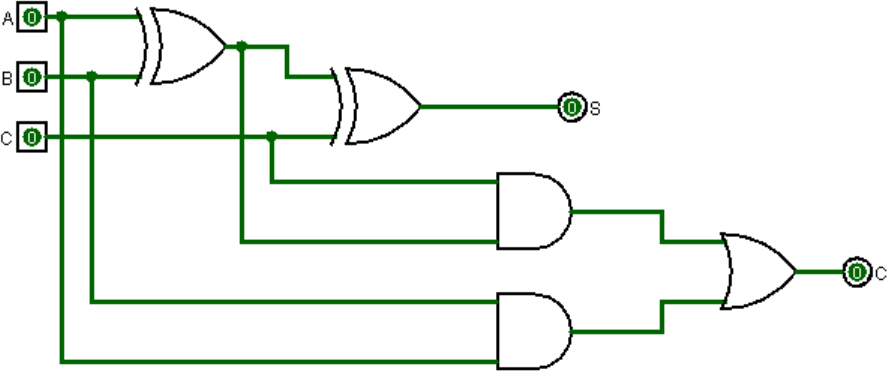
CDA 4213/CIS 6930 CMOS VLSI

Fall 2022

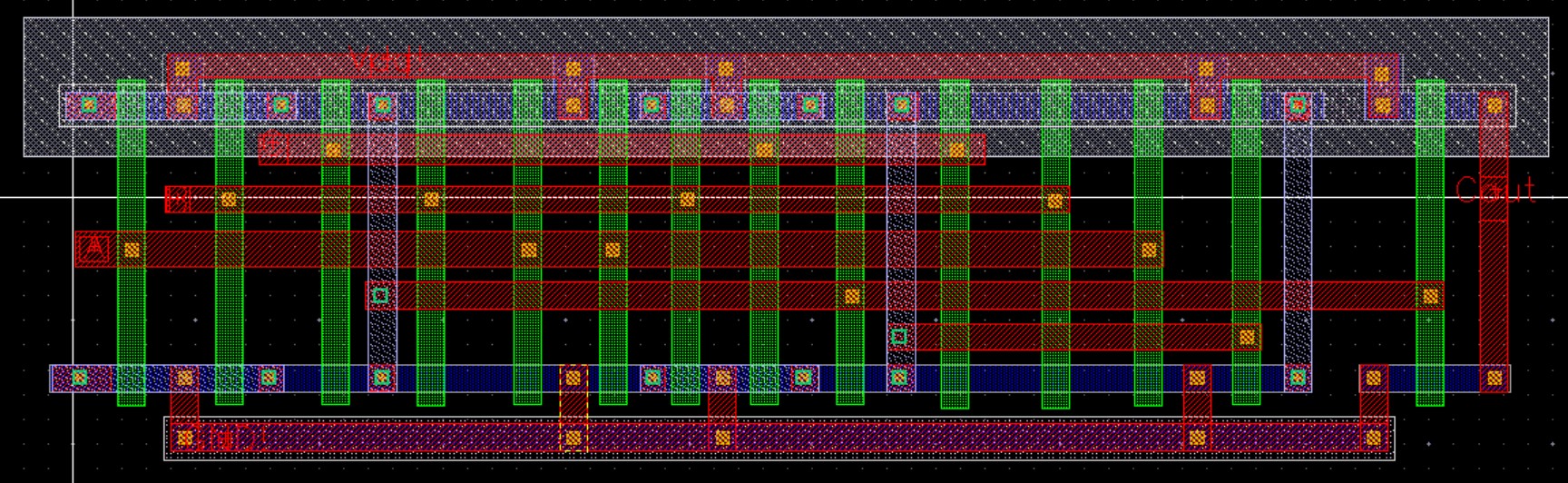
**Final Project**

|  |  |
| --- | --- |
| Today’s Date: | 12/1/2022 |
| Your Team Name | *Team Tesla* |
| Team Members | Jaylen Brown (U53294015) |
| No. of Hours Spent: | 50 hours |
| Exercise Difficulty: (Easy, Average, Hard) | Average |

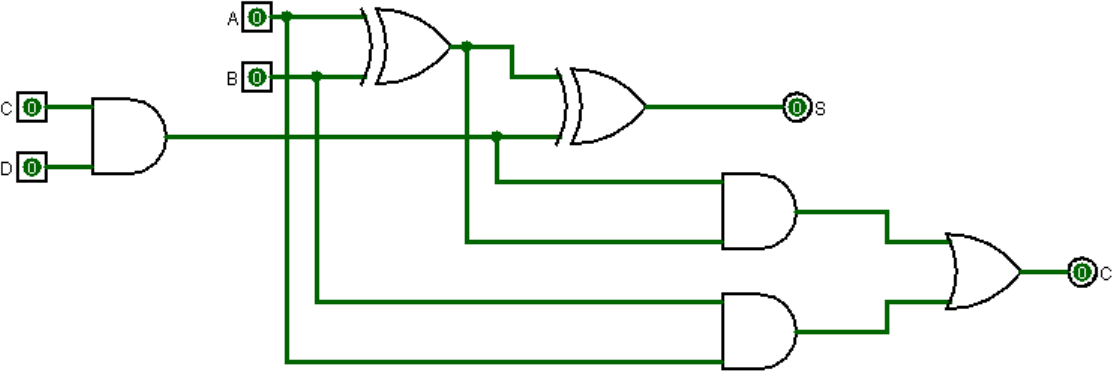
1. **Proposed Design – Bit slice design**
   1. **List all module bit-slices you have used for your design.**
      1. Full Adder:
      2. Full Adder with AND gate:
      3. Serial In Parallel Out Shift Register
      4. Parallel In Series Out Shift Register With MUX
      5. MUX
   2. **For each bit slice, show the gate-level design and layout design:**
      1. Full Adder:
         1. Gate-Level Design



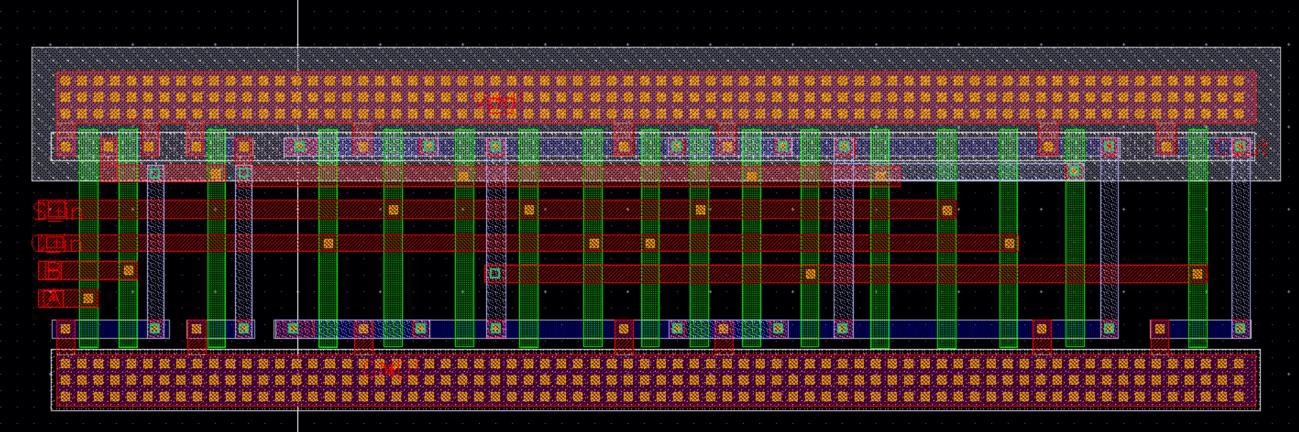
* + - 1. Layout Design



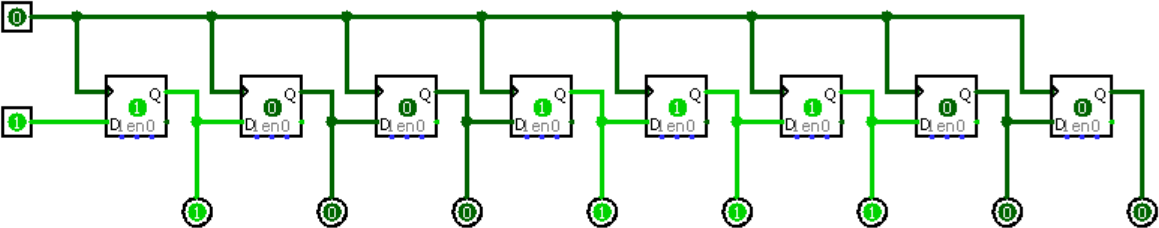
* + 1. Full Adder with AND gate:
       1. Gate-Level Design



* + - 1. Layout Design



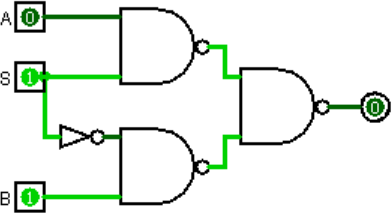
* + 1. Serial In Parallel Out Shift Register
       1. Gate-Level Design



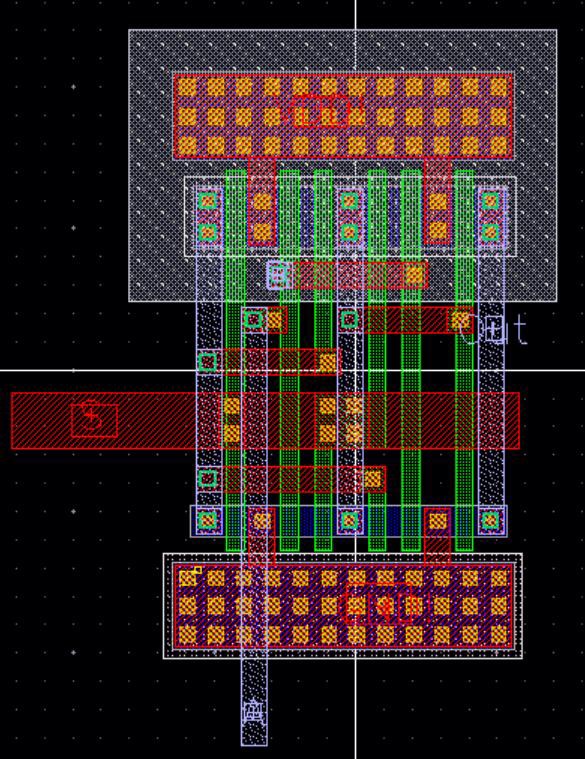
* + - 1. Layout Design



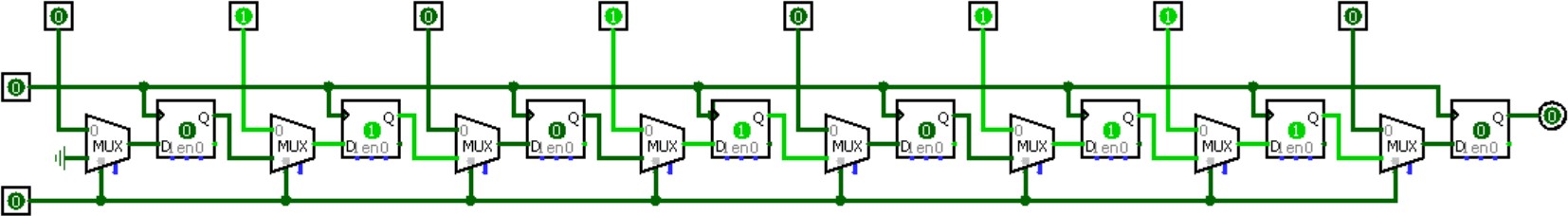
* + 1. MUX
       1. Gate-Level Design



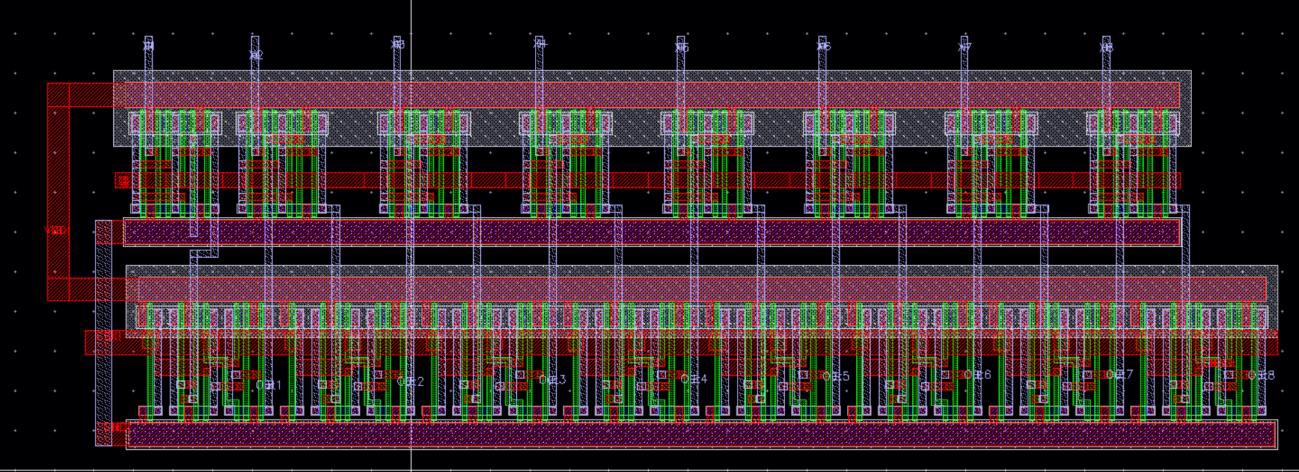
* + - 1. Layout Design



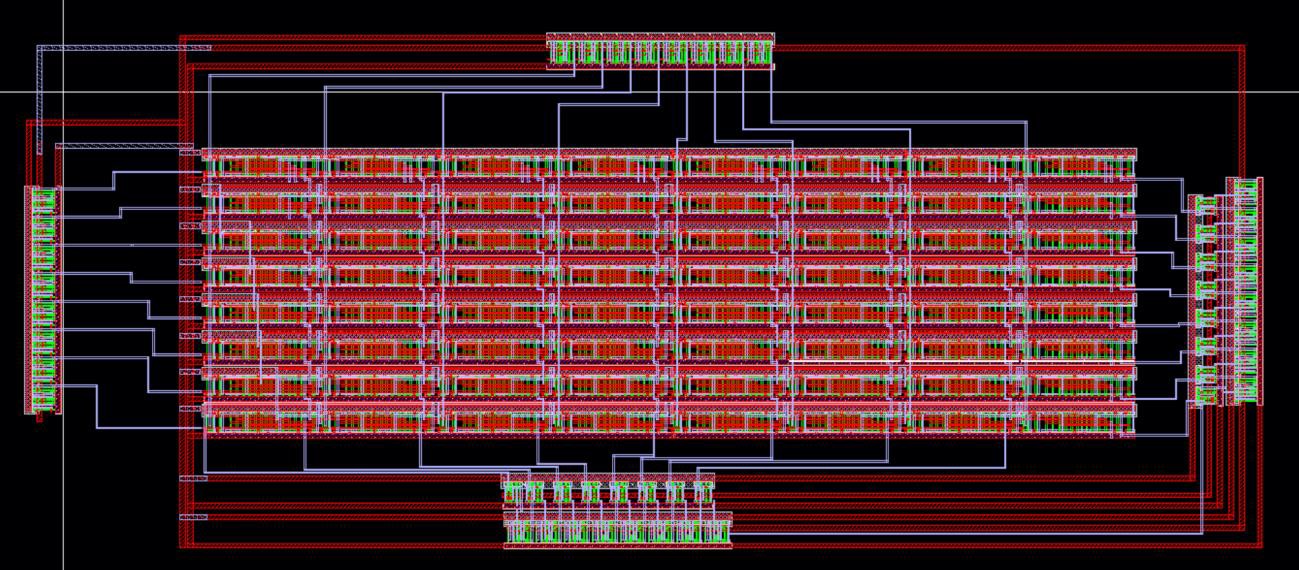
* + 1. Parallel In Series Out Shift Register With MUX
       1. Gate-Level Design



* + - 1. Layout Design



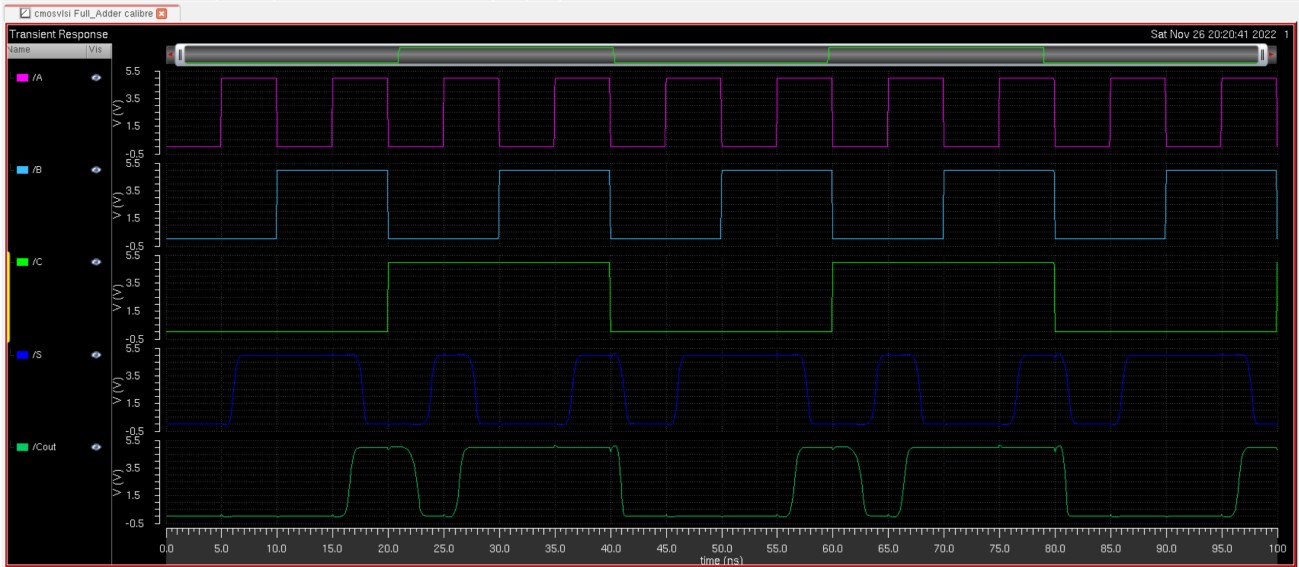
1. **Show the layout of your multiplier with the registers (outside the padframe). Explain the design and functionality of your multiplier.**



The functionality for the 8x8 multiplier starts with the two SIPO registers located on the

top and left side of the design. These SIPO registers represent the X and Y inputs that will get sent through the multiplier. Once all the X and Y inputs get pushed serially, they will be pushed out parallel to the multiplier. Once multiplier finishes calculating the result, the two PISO registers will come in to first take in the result parallelly, then second the MUX will switch from parallel input to serial input so that we can push out the multiplicand result serially from the PISO’s giving a 16-bit result.

1. **Simulation Results (without pad frame):**
   1. (5 pts total) Individual cells:
      1. Full Adder:

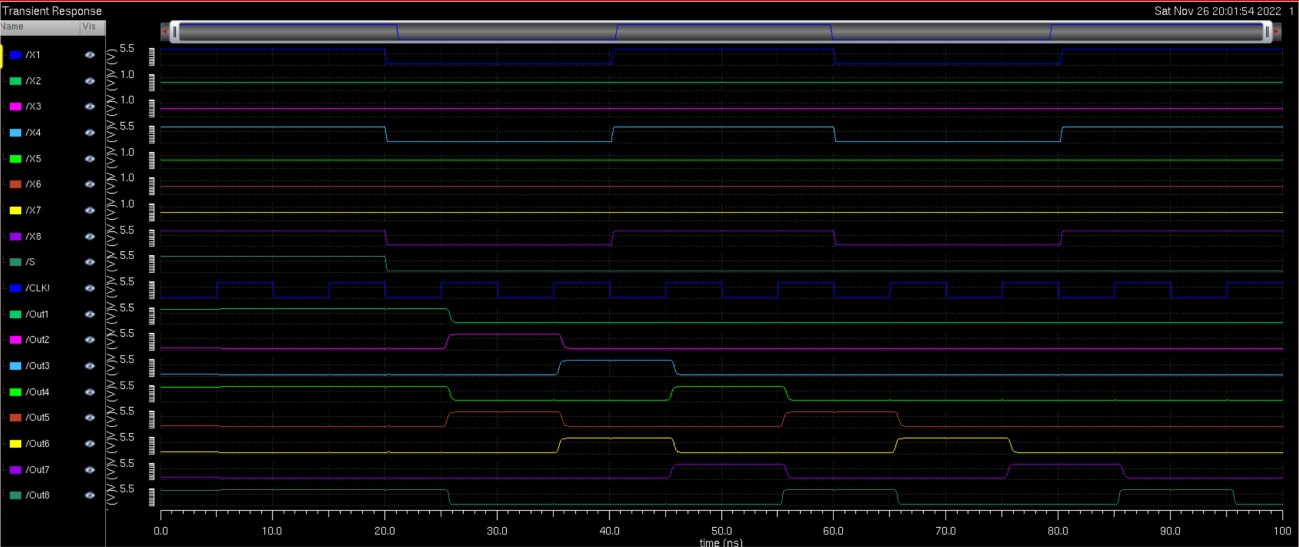


* + 1. Full Adder with AND gate:

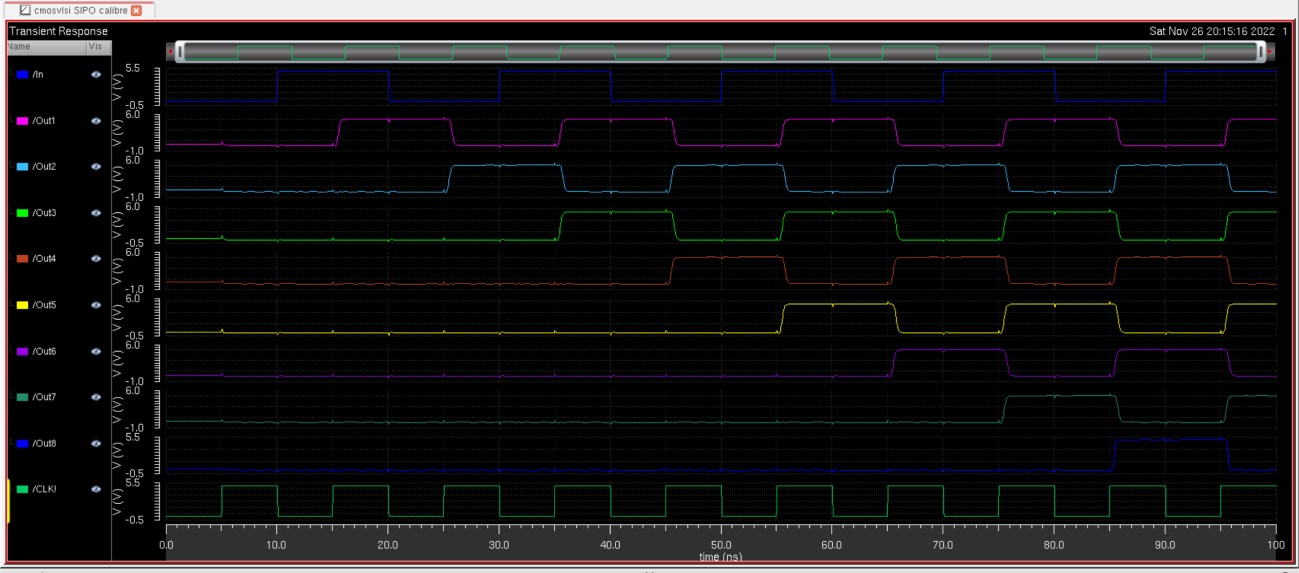


* + 1. Registers (Test Mode):

1. PISO



1. SIPO

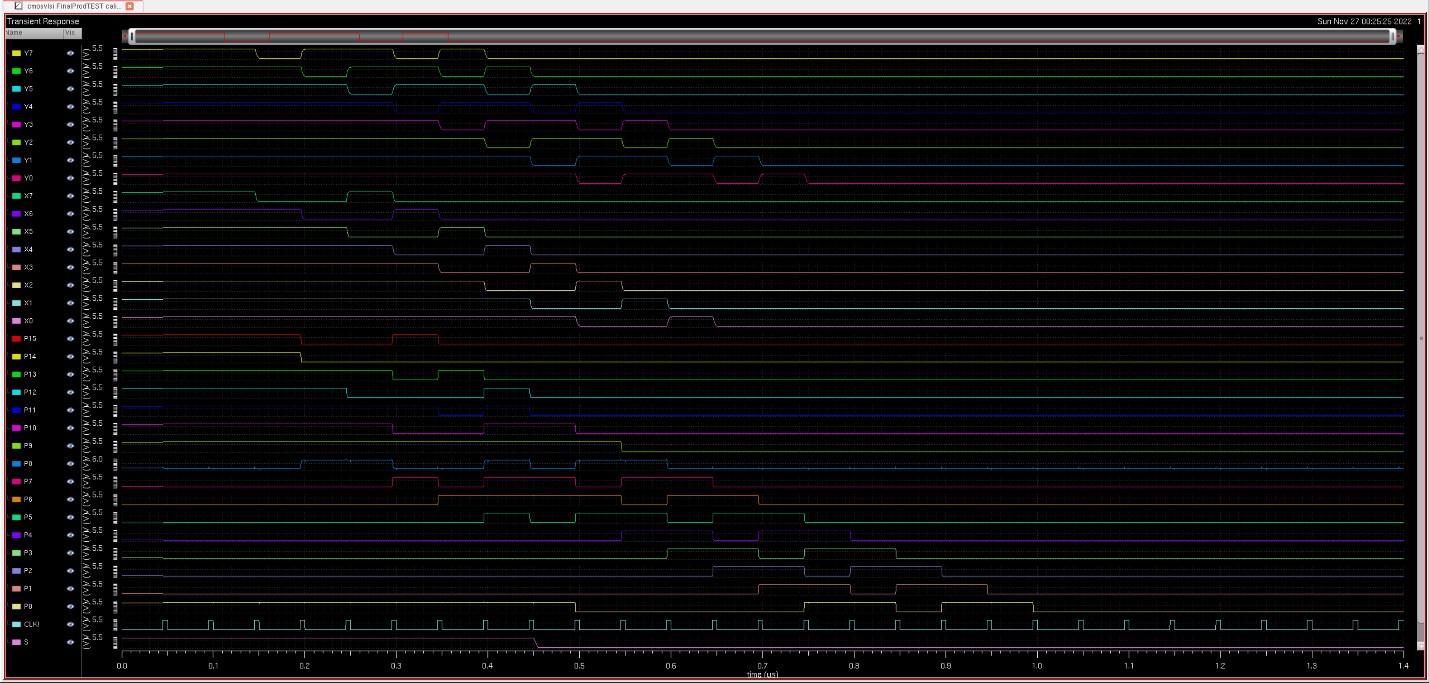


* + 1. Ring Oscillator (If used):

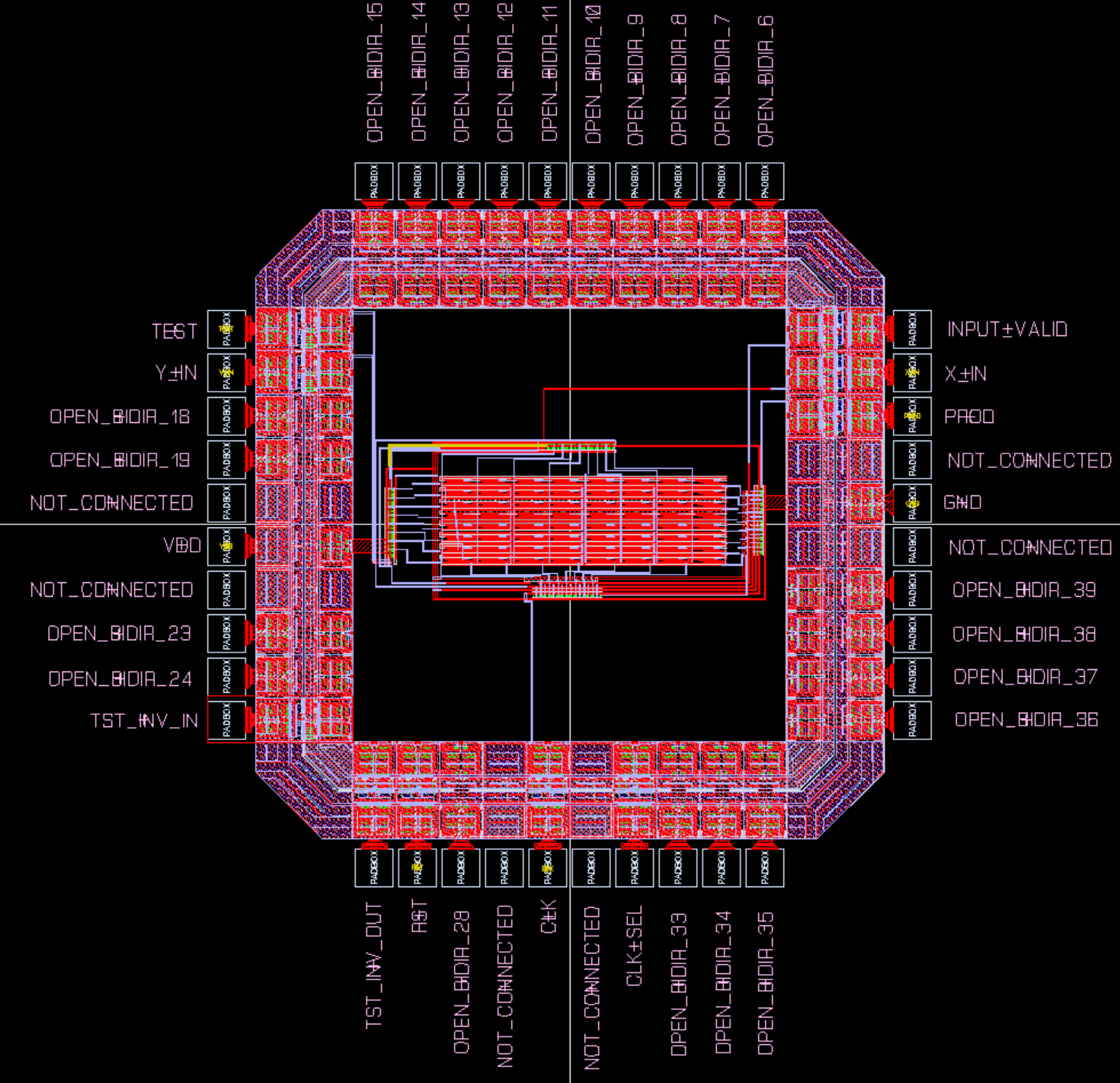
# NOT USED

* 1. (20 pts) The final multiplier:

# Test 5) 19 x 91 = 1729 (00010011 x 01011011 = 0000011011000001)



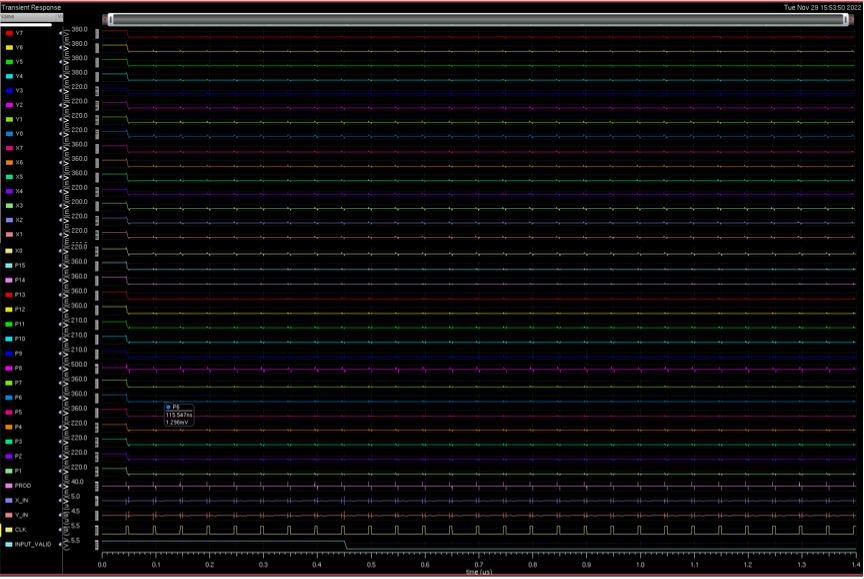
1. **Layout of the final design (with pad frame):**

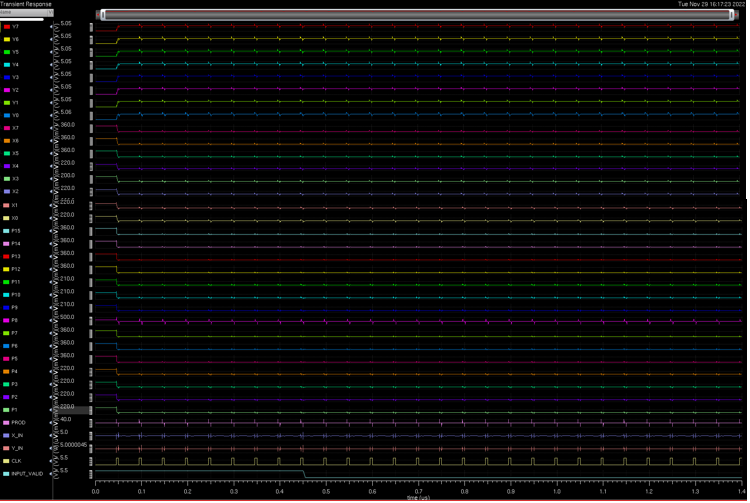


1. **Simulation waveforms for the final design (with pad frame):**

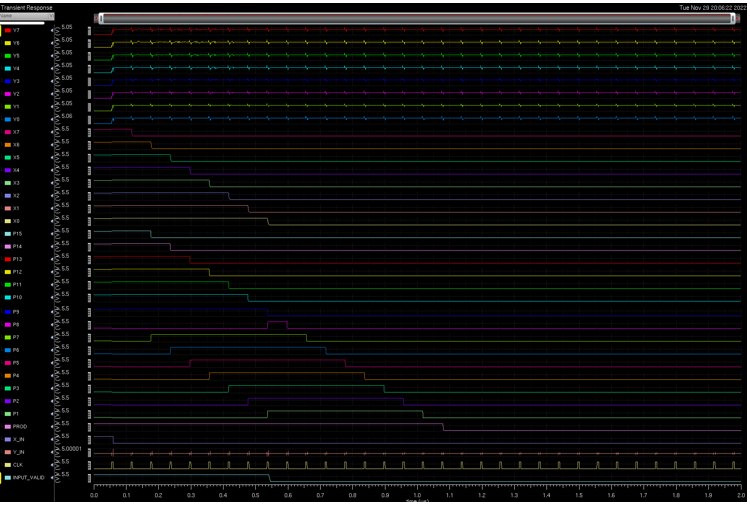
**For 8 x 8 multiplier**

With the pad frame

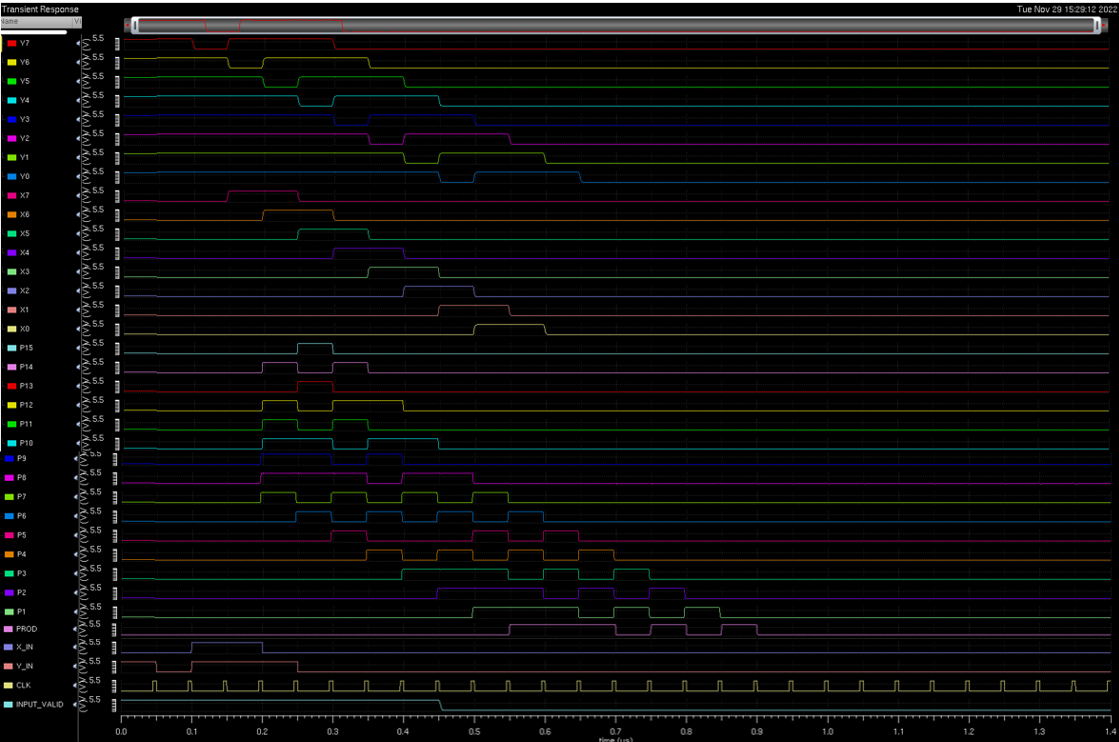
1. x 0 = 0

2)0 x 255 = 0

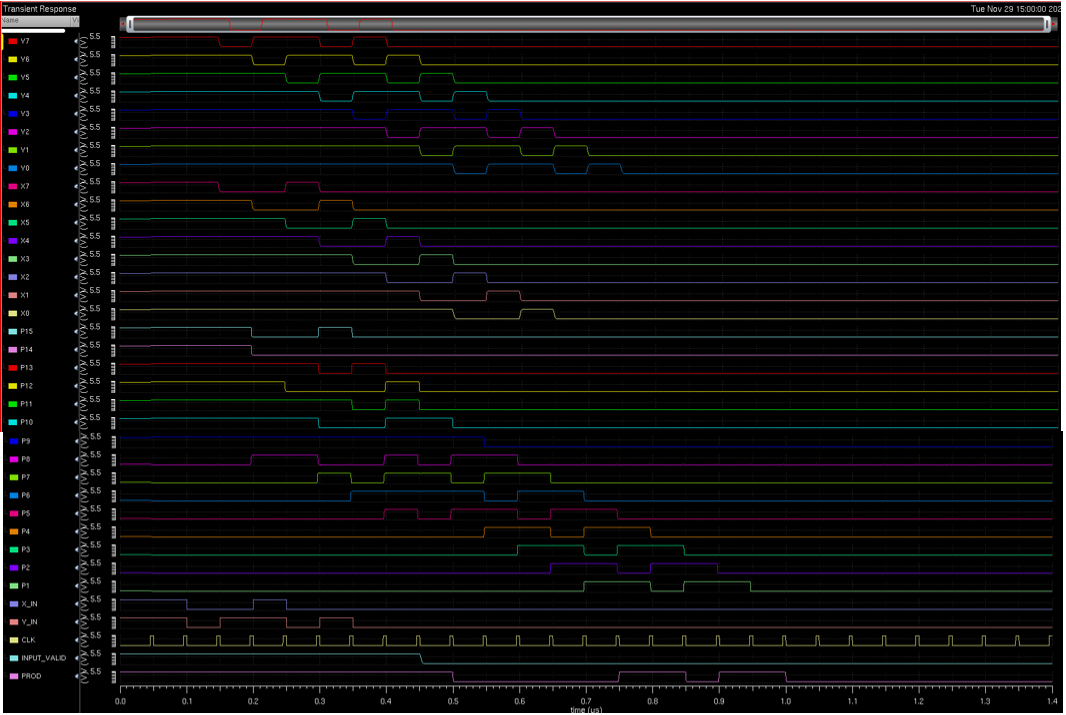
3)1 x 255 = 255 (00000001 x 11111111 = 0000000011111111)



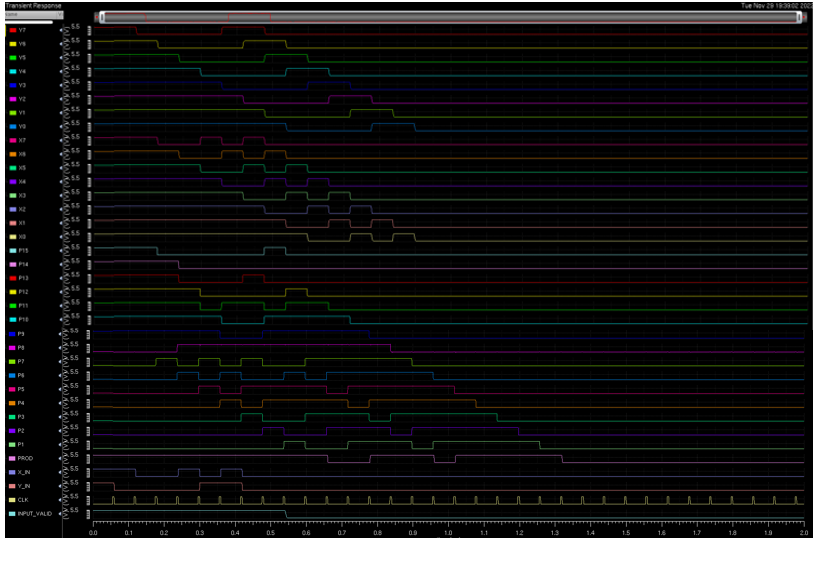
4)12 x 29 = 348 (00001100 x 00011101 = 0000000101011100)



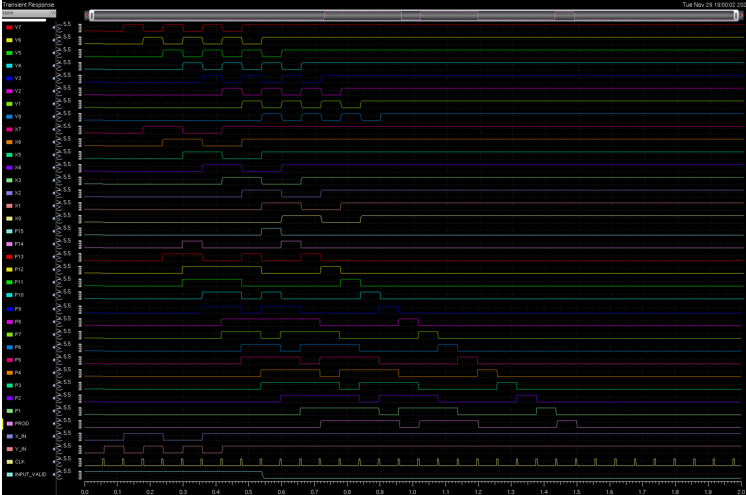
5)19 x 91 = 1729 (00010011 x 01011011 = 0000011011000001) \*\* Taxicab number



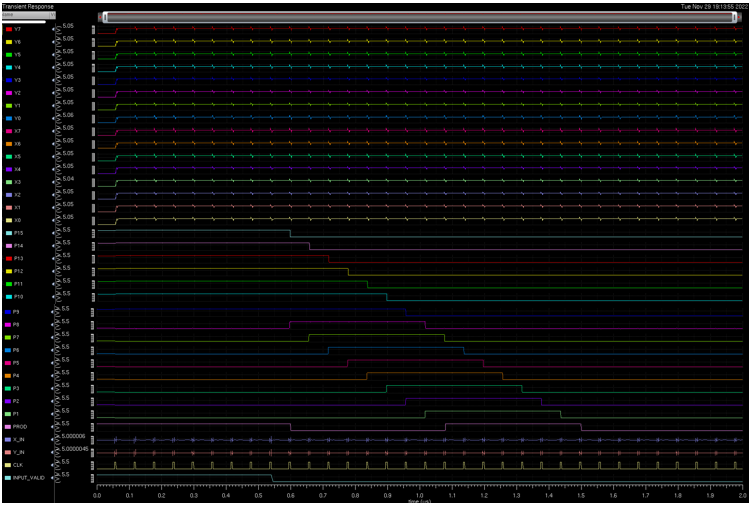
6) 83 x 97 = 8051 (01010011 x 01100001 = 0001111101110011)



7) 170 x 204 = 34680 (10101010 x 11001100 = 1000011101111000)

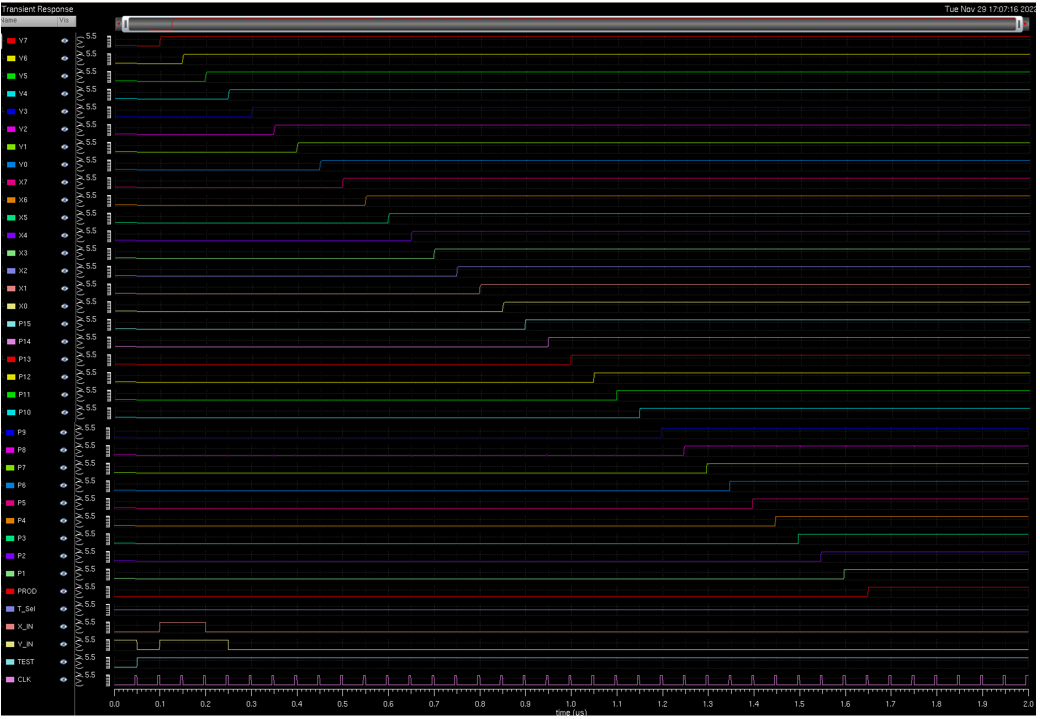


8) 255 x 255 = 65025 (11111111 x 11111111 = 1111111000000001)



**TEST MODE**

1. all 1’s GOOD



1. alternating 0's and 1's i.e., 010101...

