VLSI04 Report 2017160111 안진모

(1) Experimental Goal

Experiment의 main content는 26bit RCA, CSA 20bit CSA에 pipeline을 apply하여 clock speed를 최대로 얻는 것이다. 2stage-Pipe line을 통하여 변화하는 max clk speed 와 area, power를 관찰하고, trade off 를 고찰하자.

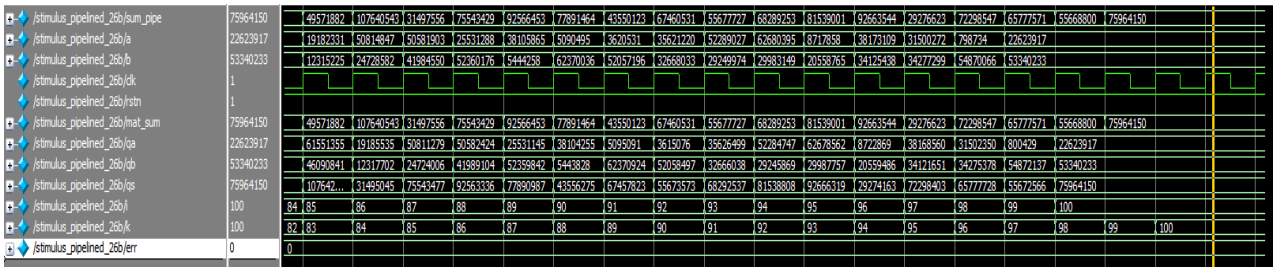
(2) Result

➔ **Zoomed schematic은 부록에 첨부하였습니다.**

➔ **또한, 모든 회로가 성능이 개선되는 사항을 결과 및 토의에 적었습니다.**

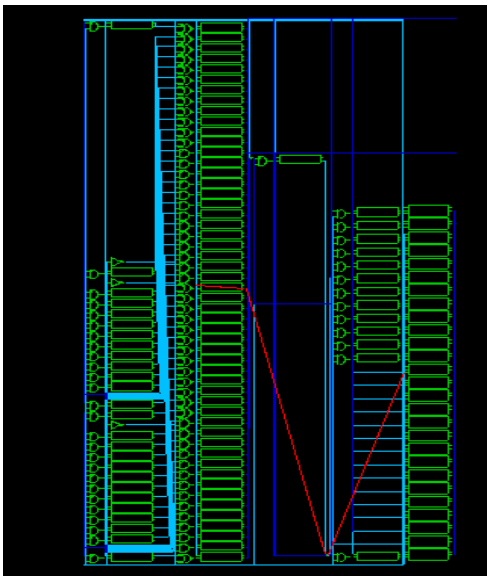
26bit-Full adder with dff, pipeline (gate level)

1. Timing diagram (for 1cycle)



2. Schematic diagram

<before synthesis>



<after synthesis>

3. Synthesis result (Area)

```
****************************************
Report : area
Design : add26bit_withpipe
Version: Z-2007.03-SP4
Date   : Mon Apr  3 16:25:35 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              161
Number of nets:               297
Number of cells:              216
Number of references:           9

Combinational area:       13511.577927
Noncombinational area:    20022.721420
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          33534.300781
Total area:                 undefined
1
```

4. Synthesis result (Timing,power)

```
Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T
    Leakage Power Units = 1pW


  Cell Internal Power  =   6.3793 mW   (65%)
  Net Switching Power  =   3.3896 mW   (35%)
                         ---------
Total Dynamic Power    =   9.7689 mW  (100%)

Cell Leakage Power     = 886.2896 nW

1
design_vision-xg-t>
```

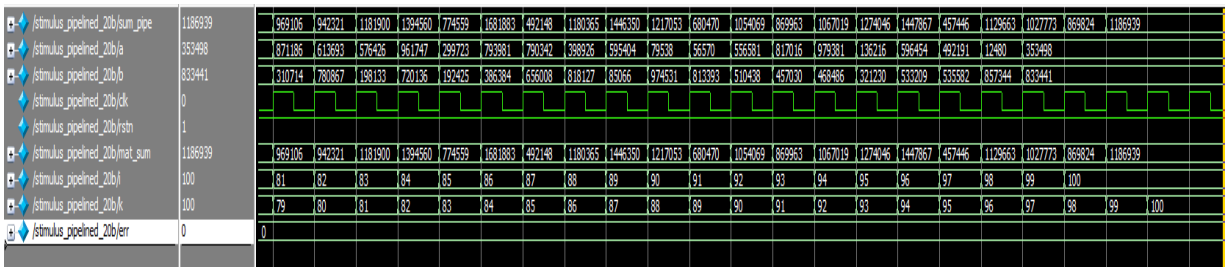
<power>

```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top

  Startpoint: qa_reg[13] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: sum_reg[25]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    2.00       2.00
  clock network delay (ideal)              0.00       2.00
  qa_reg[13]/CLK (dffs2)                   0.00       2.00 r
  qa_reg[13]/Q (dffs2)                     0.28       2.28 r
  ga2/a[0] (fulladd13_gate_1)              0.00       2.28 r
  ga2/gt1/a (fulladd_gate_13)              0.00       2.28 r
  ga2/gt1/U2/Q (oai21s3)                   0.22       2.50 f
  ga2/gt1/U1/Q (nnd2s2)                    0.18       2.68 r
  ga2/gt1/c_out (fulladd_gate_13)          0.00       2.68 r
  ga2/gt2/c_in (fulladd_gate_12)           0.00       2.68 r
  ga2/gt2/U1/Q (nnd2s2)                    0.14       2.82 f

  ga2/gt4/U1/Q (nnd2s3)                          0.10       3.27 f
  ga2/gt4/U2/Q (nnd2s3)                          0.12       3.38 r
  ga2/gt4/c_out (fulladd_gate_10)                0.00       3.38 r
  ga2/gt5/c_in (fulladd_gate_9)                  0.00       3.38 r
  ga2/gt5/U1/Q (nnd2s3)                          0.10       3.48 f
  ga2/gt5/U3/Q (nnd2s3)                          0.12       3.60 r
  ga2/gt5/c_out (fulladd_gate_9)                 0.00       3.60 r
  ga2/gt6/c_in (fulladd_gate_8)                  0.00       3.60 r
  ga2/gt6/U1/Q (nnd2s3)                          0.10       3.70 f
  ga2/gt6/U3/Q (nnd2s3)                          0.12       3.82 r
  ga2/gt6/c_out (fulladd_gate_8)                 0.00       3.82 r
  ga2/gt7/c_in (fulladd_gate_7)                  0.00       3.82 r
  ga2/gt7/U2/Q (nnd2s3)                          0.10       3.92 f
  ga2/gt7/U1/Q (nnd2s3)                          0.12       4.04 r
  ga2/gt7/c_out (fulladd_gate_7)                 0.00       4.04 r
  ga2/gt8/c_in (fulladd_gate_6)                  0.00       4.04 r
  ga2/gt8/U1/Q (nnd2s3)                          0.10       4.14 f
  ga2/gt8/U2/Q (nnd2s3)                          0.11       4.25 r
  ga2/gt8/c_out (fulladd_gate_6)                 0.00       4.25 r
  ga2/gt9/c_in (fulladd_gate_5)                  0.00       4.25 r
  ga2/gt9/U2/Q (nnd2s3)                          0.10       4.35 f
  ga2/gt9/U3/Q (nnd2s3)                          0.12       4.46 r
  ga2/gt9/c_out (fulladd_gate_5)                 0.00       4.46 r
  ga2/gt10/c_in (fulladd_gate_4)                 0.00       4.46 r
  ga2/gt10/U2/Q (nnd2s3)                         0.10       4.56 f
  ga2/gt10/U3/Q (nnd2s3)                         0.11       4.67 r
  ga2/gt10/c_out (fulladd_gate_4)                0.00       4.67 r
  ga2/gt11/c_in (fulladd_gate_3)                 0.00       4.67 r
  ga2/gt11/U2/Q (nnd2s3)                         0.10       4.77 f
  ga2/gt11/U3/Q (nnd2s3)                         0.12       4.89 r
  ga2/gt11/c_out (fulladd_gate_3)                0.00       4.89 r
  ga2/gt12/c_in (fulladd_gate_2)                 0.00       4.89 r
  ga2/gt12/U1/Q (nnd2s3)                         0.10       4.99 f
  ga2/gt12/U2/Q (nnd2s3)                         0.14       5.13 r
  ga2/gt12/c_out (fulladd_gate_2)                0.00       5.13 r
  ga2/gt13/c_in (fulladd_gate_1)                 0.00       5.13 r
  ga2/gt13/U7/Q (nnd2s2)                         0.14       5.26 f
  ga2/gt13/U4/Q (nnd2s3)                         0.16       5.42 r
  ga2/gt13/sum (fulladd_gate_1)                  0.00       5.42 r
  ga2/sum[12] (fulladd13_gate_1)                 0.00       5.42 r
  sum_reg[25]/DIN (dffles1)                      0.00       5.42 r
  data arrival time                                         5.42

  clock clk (rise edge)                          5.90       5.90
  clock network delay (ideal)                    0.00       5.90
  sum_reg[25]/CLK (dffles1)                      0.00       5.90 r
  library setup time                            -0.48       5.42
  data required time                                       5.42
  -----------------------------------------------------------------
  data required time                                       5.42
  data arrival time                                       -5.42
  -----------------------------------------------------------------
  slack (MET)                                              0.00
```

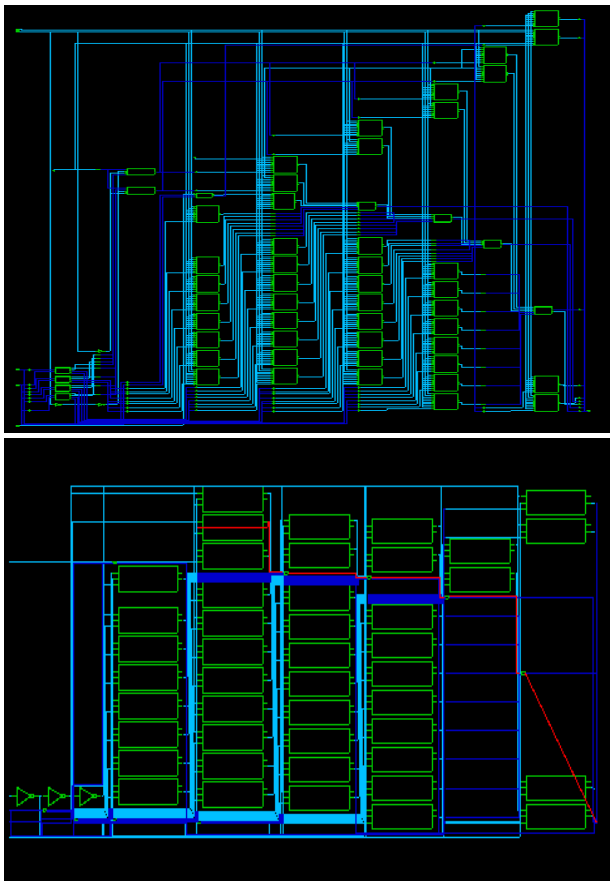
<period 3.9 -MET>

20bit Carry Select Adder with 2stage pipe line

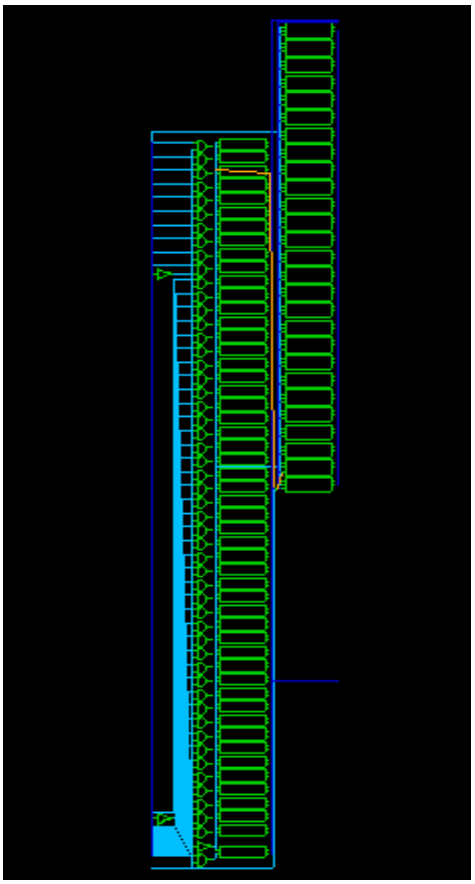
Timing diagram (for 1cycle)



1. Schematic diagram



<before synthesis>



<after synthesis>

2. Synthesis result (Timing)

```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top

  Startpoint: qb_reg[16] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: mode223/qsum2_reg[19]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                    1.00       1.00
  clock network delay (ideal)                              0.00       1.00
  qb_reg[16]/CLK (dffs2)                                   0.00       1.00 r
  qb_reg[16]/Q (dffs2)                                     0.33       1.33 f
  mode223/b[16] (carry_select_adder_20b_pipe)              0.00       1.33 f
  mode223/ad1111/b[0] (d4_adder_1)                         0.00       1.33 f
  mode223/ad1111/fa2/b[0] (fulladd4_gate_1)                0.00       1.33 f
  mode223/ad1111/fa2/gt1/b (fulladd_gate_4)                0.00       1.33 f
  mode223/ad1111/fa2/gt1/U2/Q (xor2s2)                     0.37       1.69 r
  mode223/ad1111/fa2/gt1/U4/Q (nnd2s2)                     0.10       1.79 f
  mode223/ad1111/fa2/gt1/U5/Q (nnd2s2)                     0.15       1.94 r
  mode223/ad1111/fa2/gt1/c_out (fulladd_gate_4)            0.00       1.94 r
  mode223/ad1111/fa2/gt2/c_in (fulladd_gate_3)             0.00       1.94 r
  mode223/ad1111/fa2/gt2/U4/Q (nnd2s2)                     0.11       2.05 f
  mode223/ad1111/fa2/gt2/U5/Q (nnd2s2)                     0.15       2.20 r
  mode223/ad1111/fa2/gt2/c_out (fulladd_gate_3)            0.00       2.20 r
  mode223/ad1111/fa2/gt3/c_in (fulladd_gate_2)             0.00       2.20 r
  mode223/ad1111/fa2/gt3/U5/Q (nnd2s2)                     0.13       2.34 f
  mode223/ad1111/fa2/gt3/U1/Q (nnd2s3)                     0.15       2.48 r
  mode223/ad1111/fa2/gt3/c_out (fulladd_gate_2)            0.00       2.48 r
  mode223/ad1111/fa2/gt4/c_in (fulladd_gate_1)             0.00       2.48 r
  mode223/ad1111/fa2/gt4/U1/Q (xor2s2)                     0.39       2.87 r
  mode223/ad1111/fa2/gt4/sum (fulladd_gate_1)              0.00       2.87 r
  mode223/ad1111/fa2/sum[3] (fulladd4_gate_1)              0.00       2.87 r
  mode223/ad1111/sum2[3] (d4_adder_1)                      0.00       2.87 r
  mode223/qsum2_reg[19]/DIN (dffles1)                      0.00       2.87 r
  data arrival time                                                   2.87

  clock clk (rise edge)                                    3.35       3.35
  clock network delay (ideal)                              0.00       3.35
  mode223/qsum2_reg[19]/CLK (dffles1)                      0.00       3.35 r
  library setup time                                      -0.48       2.87
  data required time                                                  2.87
  ---------------------------------------------------------------------------
  data required time                                                  2.87
  data arrival time                                                  -2.87
  ---------------------------------------------------------------------------
  slack (MET)                                                         0.00
```

<period 2.35-met>

```
Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  11.3827 mW   (79%)
  Net Switching Power  =   2.9433 mW   (21%)
                         ---------
Total Dynamic Power    =  14.3261 mW  (100%)

Cell Leakage Power     =   1.0125 uW

1
```

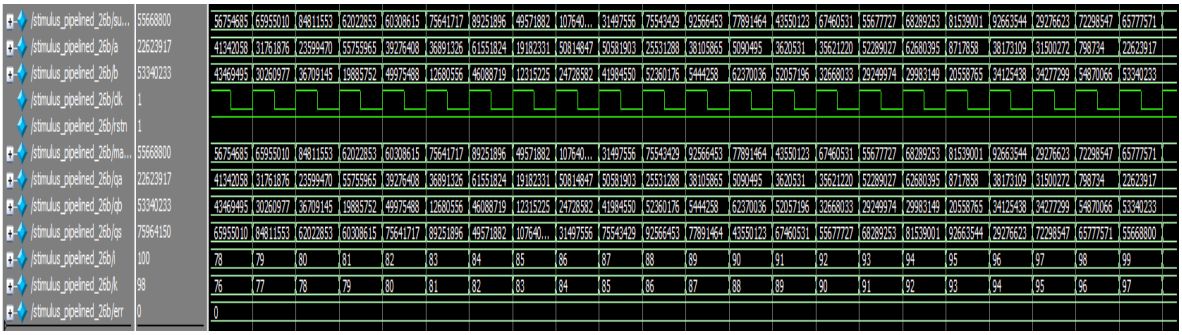
<power>

3. Synthesis result (Area)

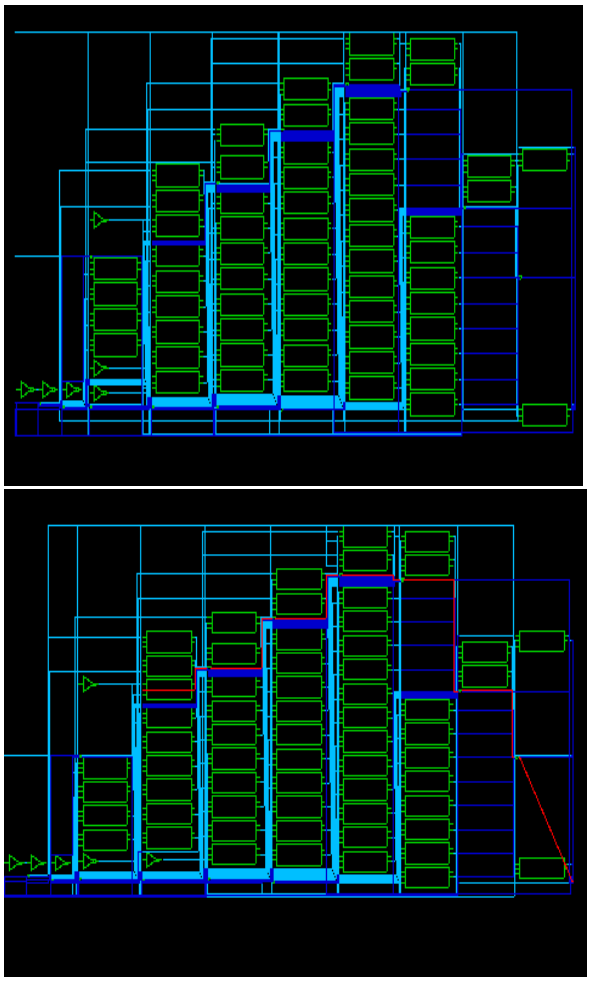
```
****************************************
Report : area
Design : carry_select_adder_20b_4444_pipe
Version: Z-2007.03-SP4
Date   : Tue Apr  4 14:04:54 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:               64
Number of nets:               167
Number of cells:              104
Number of references:           6

Combinational area:       15999.897968
Noncombinational area:    19359.161560
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          35359.058594
Total area:                 undefined
1
```

26bit carry select adder_pipelined

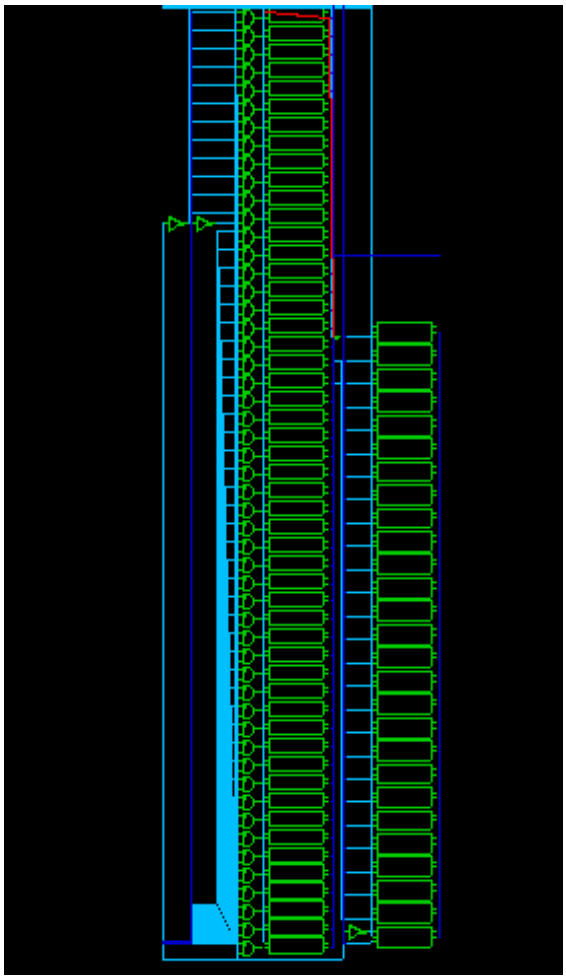
1. Timing Diagram (for 1 cycle)



2. Schematic diagram



< without clock>



<after synthesis with clock>

3. Synthesis result (Timing)

```
Startpoint: qa_reg[16] (rising edge-triggered flip-flop clocked by clk)
Endpoint: csa/qsum1_reg[21]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                    1.00       1.00
clock network delay (ideal)                              0.00       1.00
qa_reg[16]/CLK (dffs2)                                   0.00       1.00 r
qa_reg[16]/Q (dffs2)                                     0.34       1.34 f
csa/a[16] (carry_select_adder_26b_223456)                0.00       1.34 f
csa/ad5/a[0] (d6_adder)                                  0.00       1.34 f
csa/ad5/fa1/a[0] (fulladd6_gate_0)                       0.00       1.34 f
csa/ad5/fa1/gt1/a (fulladd_gate_56)                      0.00       1.34 f
csa/ad5/fa1/gt1/U1/Q (xor2s2)                            0.38       1.72 r
csa/ad5/fa1/gt1/U4/Q (nnd2s2)                            0.10       1.82 f
csa/ad5/fa1/gt1/U5/Q (nnd2s2)                            0.15       1.97 r
csa/ad5/fa1/gt1/c_out (fulladd_gate_56)                  0.00       1.97 r
csa/ad5/fa1/gt2/c_in (fulladd_gate_55)                   0.00       1.97 r
csa/ad5/fa1/gt2/U4/Q (nnd2s2)                            0.11       2.08 f
csa/ad5/fa1/gt2/U5/Q (nnd2s2)                            0.15       2.23 r
csa/ad5/fa1/gt2/c_out (fulladd_gate_55)                  0.00       2.23 r
csa/ad5/fa1/gt3/c_in (fulladd_gate_54)                   0.00       2.23 r
csa/ad5/fa1/gt3/U4/Q (nnd2s2)                            0.11       2.34 f
csa/ad5/fa1/gt3/U5/Q (nnd2s2)                            0.15       2.49 r
csa/ad5/fa1/gt3/c_out (fulladd_gate_54)                  0.00       2.49 r
csa/ad5/fa1/gt4/c_in (fulladd_gate_53)                   0.00       2.49 r
csa/ad5/fa1/gt4/U4/Q (nnd2s2)                            0.11       2.60 f
csa/ad5/fa1/gt4/U5/Q (nnd2s2)                            0.15       2.75 r
csa/ad5/fa1/gt4/c_out (fulladd_gate_53)                  0.00       2.75 r
csa/ad5/fa1/gt5/c_in (fulladd_gate_52)                   0.00       2.75 r
csa/ad5/fa1/gt5/U4/Q (nnd2s2)                            0.11       2.85 f
csa/ad5/fa1/gt5/U5/Q (nnd2s2)                            0.17       3.02 r
csa/ad5/fa1/gt5/c_out (fulladd_gate_52)                  0.00       3.02 r
csa/ad5/fa1/gt6/c_in (fulladd_gate_51)                   0.00       3.02 r
csa/ad5/fa1/gt6/U1/Q (xor2s2)                            0.39       3.42 r
csa/ad5/fa1/gt6/sum (fulladd_gate_51)                    0.00       3.42 r
csa/ad5/fa1/sum[5] (fulladd6_gate_0)                     0.00       3.42 r
csa/ad5/sum1[5] (d6_adder)                               0.00       3.42 r
csa/qsum1_reg[21]/DIN (dffles1)                          0.00       3.42 r
data arrival time                                                   3.42

clock clk (rise edge)                                    3.90       3.90
clock network delay (ideal)                              0.00       3.90
csa/qsum1_reg[21]/CLK (dffles1)                          0.00       3.90 r
library setup time                                      -0.48       3.42
data required time                                                  3.42
-----------------------------------------------------------------------------
data required time                                                  3.42
data arrival time                                                  -3.42
-----------------------------------------------------------------------------
slack (MET)                                                         0.00
```

<period 2.90-MET>

4. Synthesis result (power)

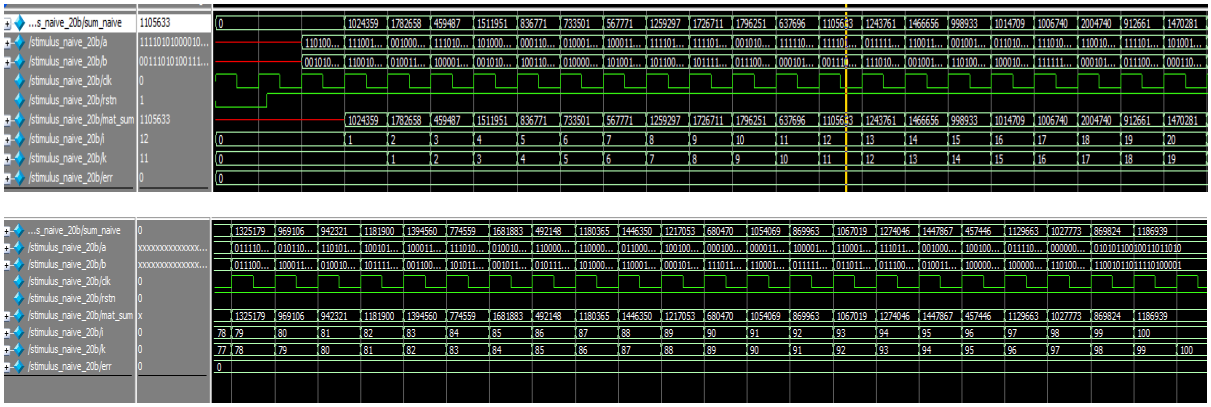
```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  12.2558 mW   (80%)
  Net Switching Power  =   3.0266 mW   (20%)
                         ---------
Total Dynamic Power    =  15.2824 mW  (100%)

Cell Leakage Power     =   1.2255 uW

1
```

5. Synthesis result (Area)

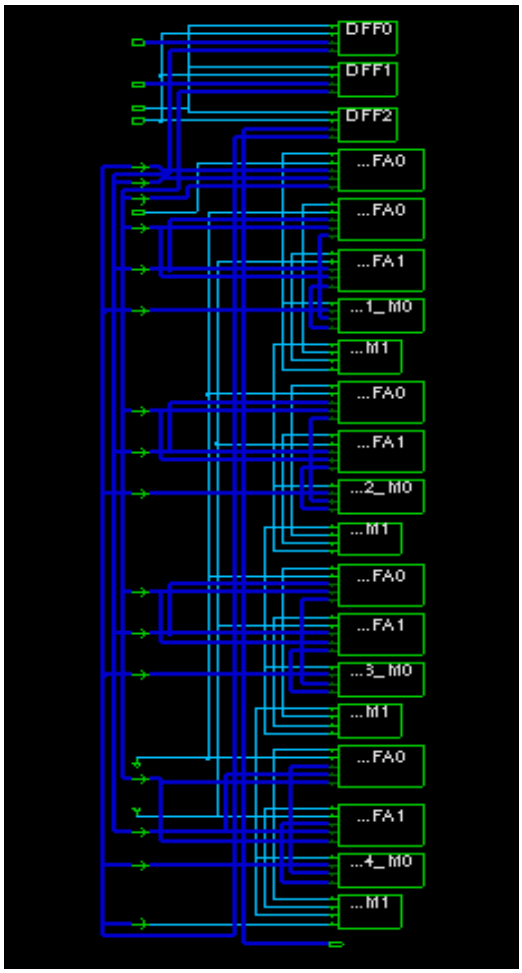
```
design_vision-xg-t> report_area

****************************************
Report : area
Design : carryselectadder1234
Version: Z-2007.03-SP4
Date   : Tue Apr  4 20:20:55 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              161
Number of nets:               216
Number of cells:              135
Number of references:           6

Combinational area:       20835.533585
Noncombinational area:    25795.629364
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          46631.164062
Total area:                 undefined
1
design_vision-xg-t>
```

Naïve 20bit carry select adder_pipelined

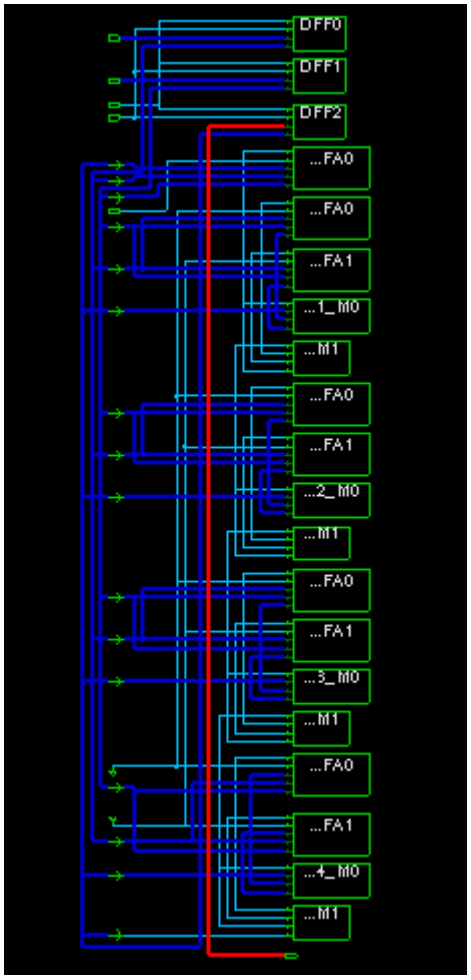
1. Timing Diagram (for 1 cycle)



2. Schematic diagram



< without clock>



<after synthesis with clock>

3. Synthesis result (Timing)

```
Startpoint: DFF0/out_reg[16]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: DFF2/out_reg[19]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                    1.00       1.00
clock network delay (ideal)                              0.00       1.00
DFF0/out_reg[16]/CLK (dffcs2)                            0.00       1.00 r
DFF0/out_reg[16]/QN (dffcs2)                             0.25       1.25 f
DFF0/out_reg[16]/Q (dffcs2)                              0.12       1.37 r
DFF0/out[16] (dff_20b_0)                                 0.00       1.37 r
STAGE_4_FA1/a[0] (full_adder_4b_1)                       0.00       1.37 r
STAGE_4_FA1/FA0/a (full_adder_1b_4)                      0.00       1.37 r
STAGE_4_FA1/FA0/U1/Q (xor2s1)                            0.43       1.80 r
STAGE_4_FA1/FA0/U3/Q (aoi22s2)                           0.26       2.06 f
STAGE_4_FA1/FA0/U2/Q (ib1s1)                             0.18       2.24 r
STAGE_4_FA1/FA0/cout (full_adder_1b_4)                   0.00       2.24 r
STAGE_4_FA1/FA1/cin (full_adder_1b_3)                    0.00       2.24 r
STAGE_4_FA1/FA1/U4/Q (aoi22s2)                           0.25       2.50 f
STAGE_4_FA1/FA1/U1/Q (ib1s1)                             0.18       2.68 r
STAGE_4_FA1/FA1/cout (full_adder_1b_3)                   0.00       2.68 r
STAGE_4_FA1/FA2/cin (full_adder_1b_2)                    0.00       2.68 r
STAGE_4_FA1/FA2/U4/Q (aoi22s2)                           0.25       2.93 f
STAGE_4_FA1/FA2/U1/Q (ib1s1)                             0.18       3.11 r
STAGE_4_FA1/FA2/cout (full_adder_1b_2)                   0.00       3.11 r
STAGE_4_FA1/FA3/cin (full_adder_1b_1)                    0.00       3.11 r
STAGE_4_FA1/FA3/U1/Q (xor2s1)                            0.40       3.51 r
STAGE_4_FA1/FA3/sum (full_adder_1b_1)                    0.00       3.51 r
STAGE_4_FA1/sum[3] (full_adder_4b_1)                     0.00       3.51 r
STAGE_4_M0/i1[3] (mux_2to1_4b_1)                         0.00       3.51 r
STAGE_4_M0/M3/i1 (mux_2to1_1b_1)                         0.00       3.51 r
STAGE_4_M0/M3/U3/Q (ib1s1)                               0.14       3.65 f
STAGE_4_M0/M3/U2/Q (mxi21s2)                             0.17       3.82 r
STAGE_4_M0/M3/out (mux_2to1_1b_1)                        0.00       3.82 r
STAGE_4_M0/out[3] (mux_2to1_4b_1)                        0.00       3.82 r
DFF2/in[19] (dff_21b)                                    0.00       3.82 r
DFF2/out_reg[19]/CLRB (dffcs1)                           0.00       3.82 r
data arrival time                                                   3.82

clock clk (rise edge)                                    4.30       4.30
clock network delay (ideal)                              0.00       4.30
DFF2/out_reg[19]/CLK (dffcs1)                            0.00       4.30 r
library setup time                                      -0.48       3.82
data required time                                                  3.82
-----------------------------------------------------------------------------
data required time                                                  3.82
data arrival time                                                  -3.82
-----------------------------------------------------------------------------
slack (MET)                                                         0.00
```

<period 3.30-MET>

4. Synthesis result (power)

```
Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)


Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   6.1169 mW   (83%)
  Net Switching Power  =   1.2407 mW   (17%)
                         ---------
Total Dynamic Power    =   7.3576 mW  (100%)

Cell Leakage Power     = 671.8207 nW
```

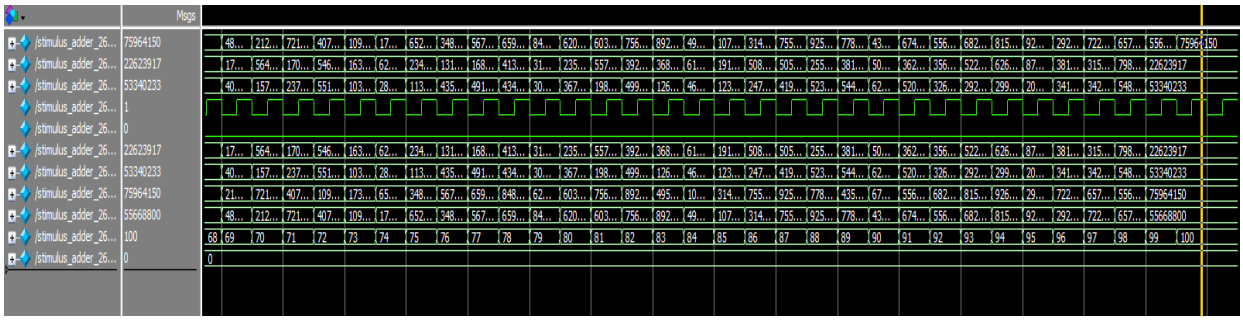
<power_report>

5. Synthesis result (Area)

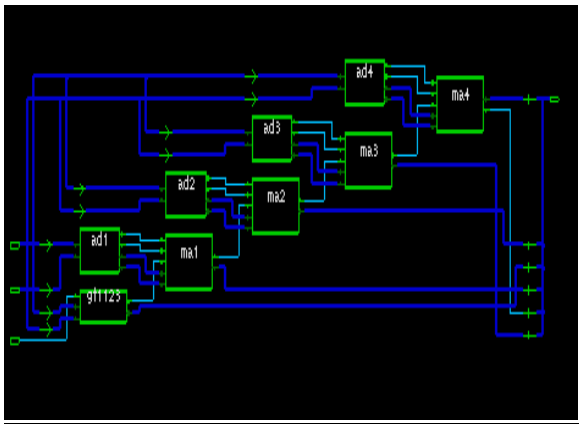
```
design_vision-xg-t> report_area

****************************************
Report : area
Design : naive_carry_select_adder_20b
Version: Z-2007.03-SP4
Date   : Tue Apr  4 21:32:06 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              64
Number of nets:              175
Number of cells:              24
Number of references:         23

Combinational area:       13511.578239
Noncombinational area:    10285.058075
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          23796.636719
Total area:                 undefined
```

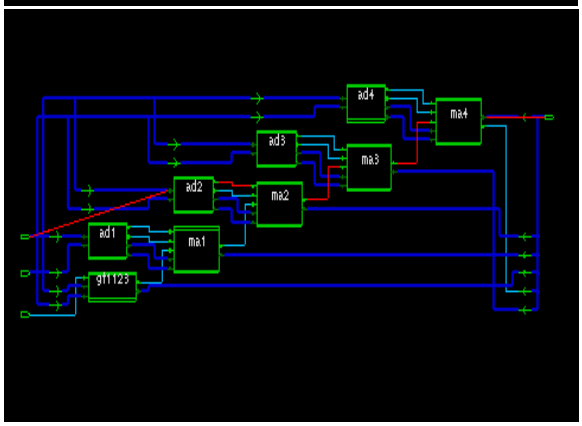
Naïve 26bit CSA

1. Timing Diagram (for 1 cycle)

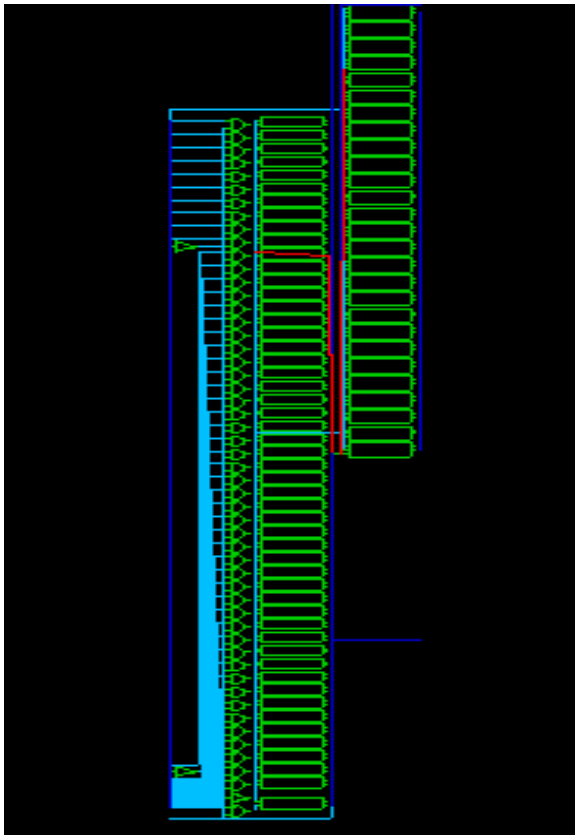


2. Schematic diagram





< without clock>



<after synthesis with clock>

3. Synthesis result (Timing)

```
Startpoint: qa_reg[19] (rising edge-triggered flip-flop clocked by clk')
Endpoint: sum_reg[25]
          (rising edge-triggered flip-flop clocked by clk')
Path Group: clk
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk' (rise edge)                                   2.00       2.00
clock network delay (ideal)                              0.00       2.00
qa_reg[19]/CLK (dffs2)                                   0.00       2.00 r
qa_reg[19]/Q (dffs2)                                     0.36       2.36 f
csa/a[19] (carry_select_adder_26b_44567)                 0.00       2.36 f
csa/ad4/a[0] (d7_adder)                                  0.00       2.36 f
csa/ad4/fa1/a[0] (fulladd7_gate_0)                       0.00       2.36 f
csa/ad4/fa1/gt1/a (fulladd_gate_14)                      0.00       2.36 f
csa/ad4/fa1/gt1/U1/Q (xnr2s2)                            0.38       2.74 f
csa/ad4/fa1/gt1/U3/Q (nnd2s2)                            0.13       2.87 r
csa/ad4/fa1/gt1/U6/Q (nnd2s2)                            0.12       2.99 f
csa/ad4/fa1/gt1/c_out (fulladd_gate_14)                  0.00       2.99 f
csa/ad4/fa1/gt2/c_in (fulladd_gate_13)                   0.00       2.99 f
csa/ad4/fa1/gt2/U5/Q (nnd2s2)                            0.11       3.10 r
csa/ad4/fa1/gt2/U6/Q (nnd2s2)                            0.12       3.22 f
csa/ad4/fa1/gt2/c_out (fulladd_gate_13)                  0.00       3.22 f
csa/ad4/fa1/gt3/c_in (fulladd_gate_12)                   0.00       3.22 f
csa/ad4/fa1/gt3/U5/Q (nnd2s2)                            0.11       3.33 r
csa/ad4/fa1/gt3/U6/Q (nnd2s2)                            0.12       3.45 f
csa/ad4/fa1/gt3/c_out (fulladd_gate_12)                  0.00       3.45 f
csa/ad4/fa1/gt4/c_in (fulladd_gate_11)                   0.00       3.45 f
csa/ad4/fa1/gt4/U6/Q (nnd2s2)                            0.11       3.56 r
csa/ad4/fa1/gt4/U7/Q (nnd2s2)                            0.13       3.70 f
csa/ad4/fa1/gt4/c_out (fulladd_gate_11)                  0.00       3.70 f
csa/ad4/fa1/gt5/c_in (fulladd_gate_10)                   0.00       3.70 f

csa/ad4/fa1/gt5/U5/Q (nnd2s2)                            0.14       3.84 r
csa/ad4/fa1/gt5/U1/Q (nnd2s3)                            0.12       3.96 f
csa/ad4/fa1/gt5/c_out (fulladd_gate_10)                  0.00       3.96 f
csa/ad4/fa1/gt6/c_in (fulladd_gate_9)                    0.00       3.96 f
csa/ad4/fa1/gt6/U1/Q (nnd2s3)                            0.11       4.07 r
csa/ad4/fa1/gt6/U2/Q (nnd2s3)                            0.11       4.18 f
csa/ad4/fa1/gt6/c_out (fulladd_gate_9)                   0.00       4.18 f
csa/ad4/fa1/gt7/c_in (fulladd_gate_8)                    0.00       4.18 f
csa/ad4/fa1/gt7/U1/Q (ib1s2)                             0.07       4.25 r
csa/ad4/fa1/gt7/U4/Q (nnd2s2)                            0.12       4.37 f
csa/ad4/fa1/gt7/U3/Q (nnd2s3)                            0.16       4.53 r
csa/ad4/fa1/gt7/sum (fulladd_gate_8)                     0.00       4.53 r
csa/ad4/fa1/sum[6] (fulladd7_gate_0)                     0.00       4.53 r
csa/ad4/sum1[6] (d7_adder)                               0.00       4.53 r
csa/ma4/s1[6] (mux_add7to1)                              0.00       4.53 r
csa/ma4/m8/DO (m21_2)                                    0.00       4.53 r
csa/ma4/m8/U1/Q (mxi21s3)                                0.20       4.73 f
csa/ma4/m8/U2/Q (i1s3)                                   0.10       4.82 r
csa/ma4/m8/Y (m21_2)                                     0.00       4.82 r
csa/ma4/sum[6] (mux_add7to1)                             0.00       4.82 r
csa/sum[25] (carry_select_adder_26b_44567)               0.00       4.82 r
sum_reg[25]/DIN (dffles1)                                0.00       4.82 r
data arrival time                                                   4.82

clock clk' (rise edge)                                   5.30       5.30
clock network delay (ideal)                              0.00       5.30
sum_reg[25]/CLK (dffles1)                                0.00       5.30 r
library setup time                                      -0.48       4.82
data required time                                                  4.82
-----------------------------------------------------------------------------
data required time                                                  4.82
data arrival time                                                  -4.82
-----------------------------------------------------------------------------
slack (MET)                                                         0.00
```

<period 3.30-MET>

4. Synthesis result (Area)

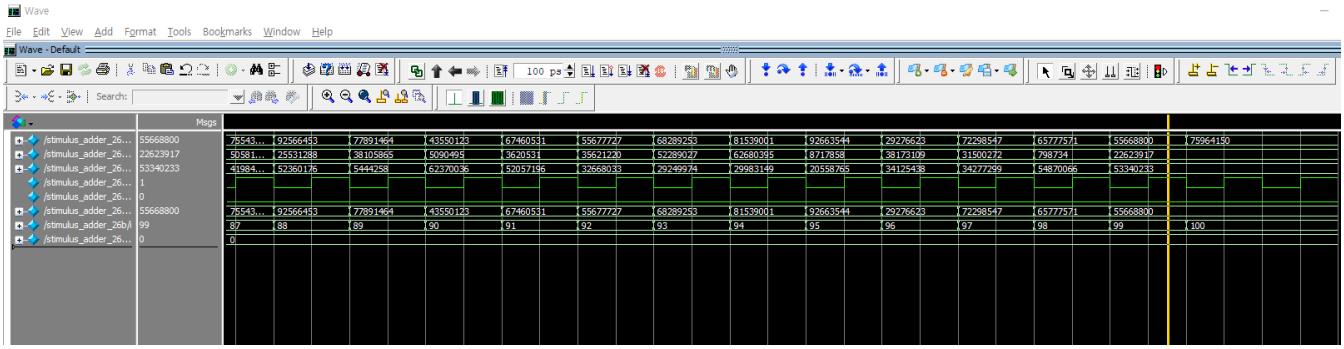
```
design_vision-xg-t> report_area

****************************************
Report : area
Design : ripple_carry_adder_26b_dff
Version: Z-2007.03-SP4
Date   : Mon Mar 27 21:50:27 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.

Number of ports:              161
Number of nets:               216
Number of cells:              135
Number of references:           6

Combinational area:       23506.331333
Noncombinational area:    13835.077744
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          37341.410156
Total area:                 undefined
1
design_vision-xg-t>
```

5. Synthesis result (power)

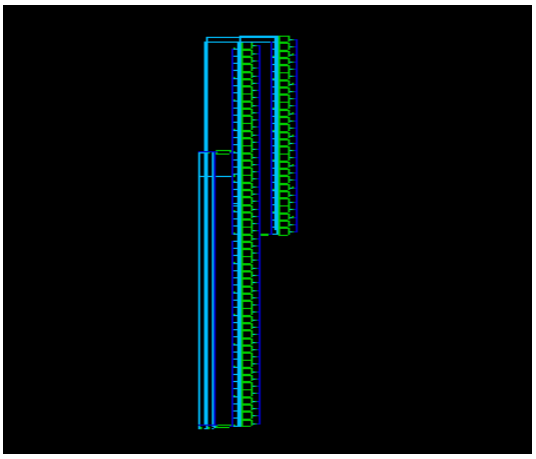
```
****************************************
Report : power
         -analysis_effort low
Design : carryselectadder
Version: Z-2007.03-SP4
Date   : Tue Apr  4 21:37:44 2023
****************************************


Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)


Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   7.8986 mW   (65%)
  Net Switching Power  =   4.2652 mW   (35%)
                         ---------
Total Dynamic Power    =  12.1637 mW  (100%)

Cell Leakage Power     =   1.0543 uW
```

Naïve 26bit-Full adder with dff (gate level)

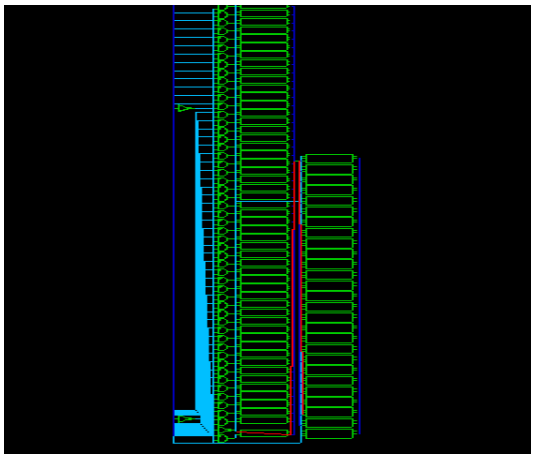
1. Timing diagram (for 1cycle)



2. Schematic diagram



<before synthesis>



<after synthesis>

3. Synthesis result (Area)

```
design_vision-xg-t> report_area

****************************************
Report : area
Design : check_rcc
Version: Z-2007.03-SP4
Date   : Mon Mar 27 21:59:02 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              81
Number of nets:              215
Number of cells:             135
Number of references:          6

Combinational area:       12698.726902
Noncombinational area:    13636.021591
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          26334.748047
Total area:                 undefined
```

4. Synthesis result (Timing)

```
rcc/fa23/U2/Q (nnd2s3)                    0.10       7.36 f
rcc/fa23/U1/Q (nnd2s3)                    0.12       7.48 r
rcc/fa23/c_out (Full_adder_3)             0.00       7.48 r
rcc/fa24/c_in (Full_adder_2)              0.00       7.48 r
rcc/fa24/U2/Q (nnd2s3)                    0.10       7.58 f
rcc/fa24/U1/Q (nnd2s3)                    0.12       7.70 r
rcc/fa24/c_out (Full_adder_2)             0.00       7.70 r
rcc/fa25/c_in (Full_adder_1)              0.00       7.70 r
rcc/fa25/U1/Q (xnr2s3)                    0.27       7.97 r
rcc/fa25/sum (Full_adder_1)               0.00       7.97 r
rcc/sum[25] (Full_adder_26)               0.00       7.97 r
sum_reg[25]/DIN (dffles1)                 0.00       7.97 r
data arrival time                                    7.97

clock CLK' (rise edge)                    8.40       8.40
clock network delay (ideal)               0.00       8.40
sum_reg[25]/CLK (dffles1)                 0.00       8.40 r
library setup time                       -0.48       7.92
data required time                                   7.92
-----------------------------------------------------------
data required time                                   7.92
data arrival time                                   -7.97
-----------------------------------------------------------
slack (VIOLATED)                                    -0.05
```

<period 6.40-Violated>

```
Startpoint: a_d_reg[0] (rising edge-triggered flip-flop clocked by CLK')
Endpoint: sum_reg[25]
          (rising edge-triggered flip-flop clocked by CLK')
Path Group: CLK
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK' (rise edge)                   2.00       2.00
clock network delay (ideal)              0.00       2.00
a_d_reg[0]/CLK (dffs2)                   0.00       2.00 r
a_d_reg[0]/Q (dffs2)                     0.27       2.27 r
rcc/a[0] (Full_adder_26)                 0.00       2.27 r
rcc/fa0/a (Full_adder_0)                 0.00       2.27 r
rcc/fa0/U3/Q (oai21s3)                   0.25       2.52 f
rcc/fa0/U2/Q (nnd2s3)                    0.14       2.66 r
rcc/fa0/c_out (Full_adder_0)             0.00       2.66 r
rcc/fa1/c_in (Full_adder_25)             0.00       2.66 r
rcc/fa1/U2/Q (nnd2s3)                    0.10       2.76 f
rcc/fa1/U6/Q (nnd2s3)                    0.11       2.87 r
rcc/fa1/c_out (Full_adder_25)            0.00       2.87 r
rcc/fa2/c_in (Full_adder_24)             0.00       2.87 r
rcc/fa2/U6/Q (nnd2s3)                    0.10       2.97 f
rcc/fa2/U5/Q (nnd2s3)                    0.11       3.08 r
rcc/fa2/c_out (Full_adder_24)            0.00       3.08 r
rcc/fa3/c_in (Full_adder_23)             0.00       3.08 r
rcc/fa3/U5/Q (nnd2s3)                    0.10       3.18 f
rcc/fa3/U4/Q (nnd2s3)                    0.11       3.29 r
rcc/fa3/c_out (Full_adder_23)            0.00       3.29 r
rcc/fa4/c_in (Full_adder_22)             0.00       3.29 r
rcc/fa4/U5/Q (nnd2s3)                    0.10       3.39 f
rcc/fa4/U4/Q (nnd2s3)                    0.11       3.50 r
rcc/fa4/c_out (Full_adder_22)            0.00       3.50 r
rcc/fa5/c_in (Full_adder_21)             0.00       3.50 r
rcc/fa5/U5/Q (nnd2s3)                    0.10       3.60 f
rcc/fa5/U4/Q (nnd2s3)                    0.11       3.71 r
rcc/fa5/c_out (Full_adder_21)            0.00       3.71 r
rcc/fa6/c_in (Full_adder_20)             0.00       3.71 r
rcc/fa6/U5/Q (nnd2s3)                    0.10       3.81 f
```

```
  rcc/fa14/U4/Q (nnd2s3)                  0.12       5.60 r
  rcc/fa14/c_out (Full_adder_12)          0.00       5.60 r
  rcc/fa15/c_in (Full_adder_11)           0.00       5.60 r
  rcc/fa15/U4/Q (nnd2s3)                  0.10       5.70 f
  rcc/fa15/U3/Q (nnd2s3)                  0.11       5.81 r
  rcc/fa15/c_out (Full_adder_11)          0.00       5.81 r
  rcc/fa16/c_in (Full_adder_10)           0.00       5.81 r
  rcc/fa16/U5/Q (nnd2s3)                  0.10       5.91 f
  rcc/fa16/U4/Q (nnd2s3)                  0.11       6.02 r
  rcc/fa16/c_out (Full_adder_10)          0.00       6.02 r
  rcc/fa17/c_in (Full_adder_9)            0.00       6.02 r
  rcc/fa17/U4/Q (nnd2s3)                  0.10       6.12 f
  rcc/fa17/U5/Q (nnd2s3)                  0.11       6.23 r
  rcc/fa17/c_out (Full_adder_9)           0.00       6.23 r
  rcc/fa18/c_in (Full_adder_8)            0.00       6.23 r
  rcc/fa18/U5/Q (nnd2s3)                  0.10       6.32 f
  rcc/fa18/U4/Q (nnd2s3)                  0.11       6.44 r
  rcc/fa18/c_out (Full_adder_8)           0.00       6.44 r
  rcc/fa19/c_in (Full_adder_7)            0.00       6.44 r
  rcc/fa19/U5/Q (nnd2s3)                  0.10       6.53 f
  rcc/fa19/U4/Q (nnd2s3)                  0.11       6.64 r
  rcc/fa19/c_out (Full_adder_7)           0.00       6.64 r
  rcc/fa20/c_in (Full_adder_6)            0.00       6.64 r
  rcc/fa20/U5/Q (nnd2s3)                  0.10       6.74 f
  rcc/fa20/U4/Q (nnd2s3)                  0.11       6.85 r
  rcc/fa20/c_out (Full_adder_6)           0.00       6.85 r
  rcc/fa21/c_in (Full_adder_5)            0.00       6.85 r
  rcc/fa21/U5/Q (nnd2s3)                  0.10       6.95 f
  rcc/fa21/U4/Q (nnd2s3)                  0.11       7.06 r
  rcc/fa21/c_out (Full_adder_5)           0.00       7.06 r
  rcc/fa22/c_in (Full_adder_4)            0.00       7.06 r
  rcc/fa22/U4/Q (nnd2s3)                  0.10       7.16 f
  rcc/fa22/U5/Q (nnd2s3)                  0.11       7.27 r
  rcc/fa22/c_out (Full_adder_4)           0.00       7.27 r
  rcc/fa23/c_in (Full_adder_3)            0.00       7.27 r
  rcc/fa23/U9/Q (nnd2s3)                  0.10       7.37 f
  rcc/fa23/U8/Q (nnd2s3)                  0.12       7.49 r
  rcc/fa23/c_out (Full_adder_3)           0.00       7.49 r
  rcc/fa24/c_in (Full_adder_2)            0.00       7.49 r
  rcc/fa24/U4/Q (nnd2s3)                  0.10       7.59 f
  rcc/fa24/U3/Q (nnd2s3)                  0.13       7.72 r
  rcc/fa24/c_out (Full_adder_2)           0.00       7.72 r
  rcc/fa25/c_in (Full_adder_1)            0.00       7.72 r
  rcc/fa25/U5/Q (nnd2s2)                  0.14       7.86 f
  rcc/fa25/U3/Q (nnd2s3)                  0.16       8.02 r
  rcc/fa25/sum (Full_adder_1)             0.00       8.02 r
  rcc/sum[25] (Full_adder_26)             0.00       8.02 r
  sum_reg[25]/DIN (dffles1)               0.00       8.02 r
  data arrival time                                  8.02

  clock CLK' (rise edge)                  8.50       8.50
  clock network delay (ideal)             0.00       8.50
  sum_reg[25]/CLK (dffles1)               0.00       8.50 r
  library setup time                     -0.48       8.02
  data required time                                 8.02
  ---------------------------------------------------------
  data required time                                 8.02
  data arrival time                                 -8.02
  ---------------------------------------------------------
  slack (MET)                                        0.00
```

<period 6.5 -MET>

5. Synthesis result (power)

```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   3.0972 mW   (66%)
  Net Switching Power  =   1.6135 mW   (34%)
                         ---------
Total Dynamic Power    =   4.7108 mW  (100%)

Cell Leakage Power     = 734.0646 nW
```

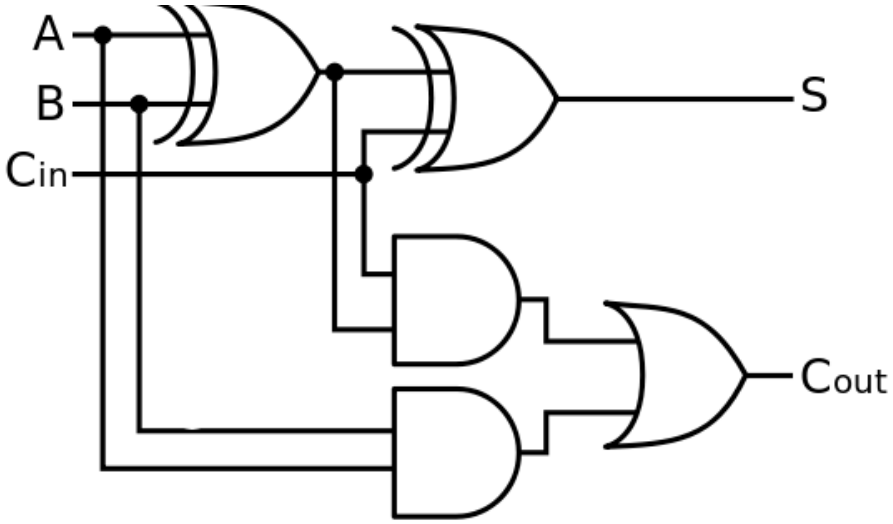
(3) Discussion

먼저 Adder 자체의 Time complexity에 대하여 고민해보자. 알려진 Instruction별 Time complexity를 조사한 결과,

	8-bit	16-bit	32-bit	r-bit
Addition	0.38	0.83	1.69	$(5r-3)T_B$
Subtraction	0.36	0.82	1.67	$(5r-3)T_B$
Multiplication	4.85	17.96	69.07	$(6_r^2+4)T_B+4rT_X$
Division	6.89	27.48	109.86	$(8r^2-4r+4)T_B+(r^2+2r)T_X$
Absolute value	0.33	0.64	1.35	$2rT_B+rT_X$
2's compliment	0.14	0.31	0.66	$(2r-3)T_B$
Power	8.78	34.09	135.53	$(12r^2+5r+5)T_B+8rT_X$
Logarithm	23.85	152.55	1123.13	$3r^3T_B+55rT_B-33T_B+2rT_X$

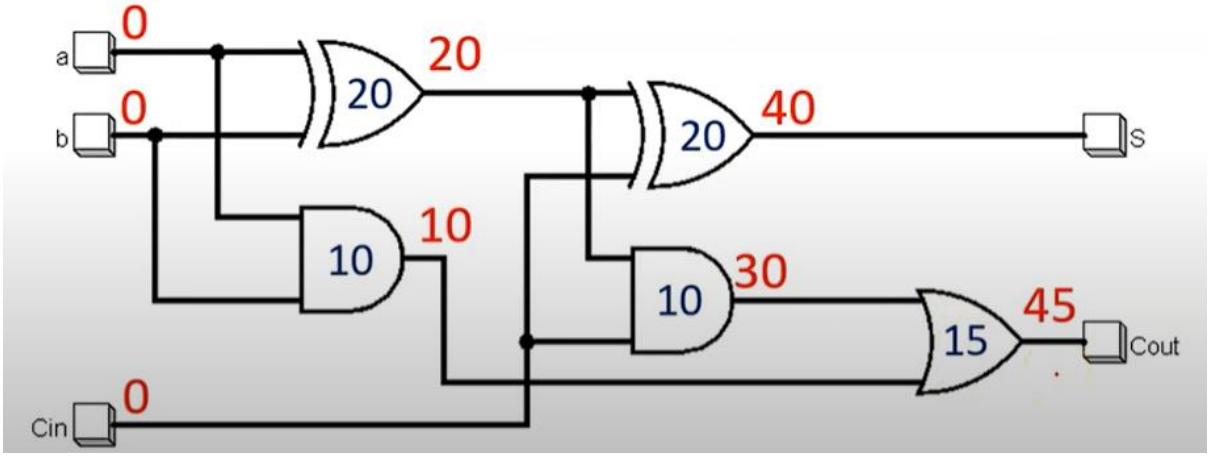
<Research gate-time complexity>

위와 같다. 위를 검증하기 위하여 이전의 02번 Report의 보고서의 discussion part를 참조하면 다음과 같이 분석할 수 있다. -26bitAdder의 경우 실제 Performance 와 Critical path를 analysis하는 방향으로 진행하자. 이제 Critical path에 대한 분석을 진행하자. 먼저 16bit full Adder이므로, Bottom up 방식의 분석을 위하여 Full adder의 schematic으로 생각하자.

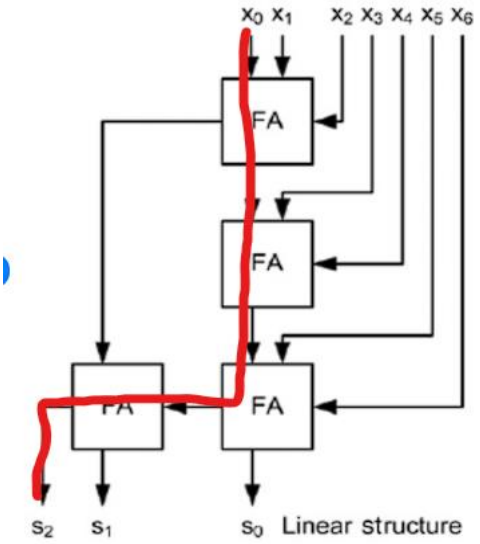


<full adder's schematic>

위의 Full adder 는 working left to right 하며, 각각의 gate delay 의 sum 이 회로의 largest input delay 라고 하자. 이때, and gate 의 gate delay 를 10ns, or gate 는 15ns, XOR gate 는 20ns 라고 가정하고 각각의 gate delay 를 sum 하면,

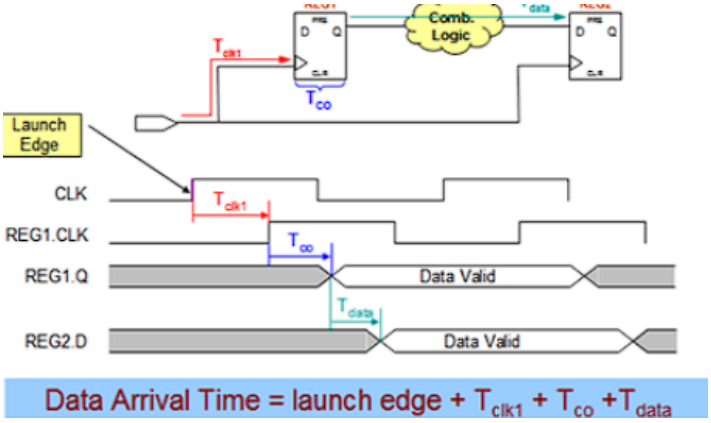


위와 같은 상황이 되고 최종적으로 회로의 max gate delay는 45ns가 된다. 따라서 critical path는 45ns를 만드는 path가 될 것이다. 이제 N-bit Full adder의 경우를 살펴보자.



<4bit adder schematic>

앞선 논의를 그대로 가져올 경우 위의 schematic에서 Full adder를 1개의 gate 로 보았을 때 45ns gate delay를 갖는 logic gate로 생각할 수 있고 위의 그림에서 4bit full adder의 경우 45ns *4 = 180ns의 gate delay를 갖게 된다. 따라서 해당 논의에서 N-bit full adder의 경우 N*45ns의 delay를 갖게 될 것이다. 같은 원리를 Experimental result에 apply해보자. 앞선 실험에서 DFF가 apply되지 않은 16bit Full adder의 data arrival time은 11.61ns과 같다. 이때, data arrival time에 대하여 간략히 설명하면,



위의 사진을 예로 들 수 있다. Data arrival time은 실제로 Data가 register2의 input D에 도달하는 시간이다. 위의 그림을 보면, Launch edge에서 시작해서 T_clk1(register1의 clock skew)과 T_co(register1의 clock to output delay)및 T_data(Comb. Logic의 delay)를 더한 value가 Data Arrival time이다. 이제 우리가 위에서 구한 N*(FA-delay) algorithm은 Combinational logic delay라는 것을 알 수 있다. 하지만, 그 외 Clock to output delay나 Clock skew등이 존재한다. 그렇다면 이들이 영향을 미치는 것을 알아보기 위해 N-bit FA를 design하고 이에 대한 timing report를 fitting하자. 너무 많은 bit수를 apply하지 않고, 각 2bit, 4bit 8bit를 더 넣어, timing을 비교하여 fitting해보도록 하자.

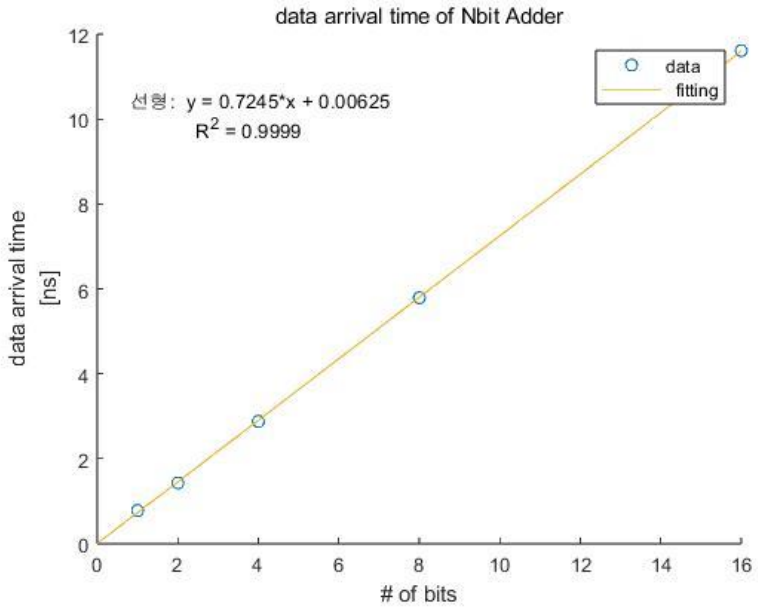
```
Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
a (in)                                   0.00       0.00 r
U8/Q (xor2s1)                            0.38       0.38 r
U7/Q (aoi22s1)                           0.26       0.64 f
U6/Q (hi1s1)                             0.14       0.78 r
c_out (out)                              0.00       0.78 r
data arrival time                                   0.78
-----------------------------------------------------------
(Path is unconstrained)
```

```
Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
a[0] (in)                                0.00       0.00 r
__tmp100/a (fulladd_gate_0)              0.00       0.00 r
__tmp100/U4/Q (xor2s1)                   0.38       0.38 r
__tmp100/U3/Q (aoi22s1)                  0.26       0.64 f
__tmp100/U2/Q (hi1s1)                    0.36       1.00 r
__tmp100/c_out (fulladd_gate_0)          0.00       1.00 r
__tmp101/c_in (fulladd_gate_1)           0.00       1.00 r
__tmp101/U3/Q (aoi22s1)                  0.29       1.29 f
__tmp101/U2/Q (hi1s1)                    0.14       1.43 r
__tmp101/c_out (fulladd_gate_1)          0.00       1.43 r
sum[2] (out)                             0.00       1.43 r
data arrival time                                   1.43
-----------------------------------------------------------
(Path is unconstrained)
```

```
Point                                          Incr       Path
-------------------------------------------------------------
input external delay                           0.00       0.00 f
a[0] (in)                                      0.00       0.00 f
__tmp150/a (fulladd_gate_0)                    0.00       0.00 f
__tmp150/U8/Q (xor2s1)                         0.32       0.32 f
__tmp150/U7/Q (aoi22s1)                        0.25       0.57 r
__tmp150/U6/Q (hi1s1)                          0.38       0.95 f
__tmp150/c_out (fulladd_gate_0)                0.00       0.95 f
__tmp151/c_in (fulladd_gate_3)                 0.00       0.95 f
__tmp151/U7/Q (aoi22s1)                        0.33       1.28 r
__tmp151/U6/Q (hi1s1)                          0.40       1.68 f
__tmp151/c_out (fulladd_gate_3)                0.00       1.68 f
__tmp152/c_in (fulladd_gate_2)                 0.00       1.68 f
__tmp152/U7/Q (aoi22s1)                        0.33       2.01 r
__tmp152/U6/Q (hi1s1)                          0.40       2.40 f
__tmp152/c_out (fulladd_gate_2)                0.00       2.40 f
__tmp153/c_in (fulladd_gate_1)                 0.00       2.40 f
__tmp153/U7/Q (aoi22s1)                        0.33       2.73 r
__tmp153/U6/Q (hi1s1)                          0.14       2.88 f
__tmp153/c_out (fulladd_gate_1)                0.00       2.88 f
sum[4] (out)                                   0.00       2.88 f
data arrival time                                         2.88
-------------------------------------------------------------
(Path is unconstrained)
```

```
__tmp102/U6/Q (hi1s1)                          0.40       2.40 f
__tmp102/c_out (fulladd_gate_10)               0.00       2.40 f
__tmp103/c_in (fulladd_gate_9)                 0.00       2.40 f
__tmp103/U7/Q (aoi22s1)                        0.33       2.73 r
__tmp103/U6/Q (hi1s1)                          0.40       3.13 f
__tmp103/c_out (fulladd_gate_9)                0.00       3.13 f
__tmp104/c_in (fulladd_gate_8)                 0.00       3.13 f
__tmp104/U7/Q (aoi22s1)                        0.33       3.46 r
__tmp104/U6/Q (hi1s1)                          0.40       3.86 f
__tmp104/c_out (fulladd_gate_8)                0.00       3.86 f
__tmp105/c_in (fulladd_gate_7)                 0.00       3.86 f
__tmp105/U7/Q (aoi22s1)                        0.33       4.19 r
__tmp105/U6/Q (hi1s1)                          0.40       4.59 f
__tmp105/c_out (fulladd_gate_7)                0.00       4.59 f
__tmp106/c_in (fulladd_gate_6)                 0.00       4.59 f
__tmp106/U7/Q (aoi22s1)                        0.33       4.92 r
__tmp106/U6/Q (hi1s1)                          0.40       5.31 f
__tmp106/c_out (fulladd_gate_6)                0.00       5.31 f
__tmp107/c_in (fulladd_gate_5)                 0.00       5.31 f
__tmp107/U7/Q (aoi22s1)                        0.33       5.65 r
__tmp107/U6/Q (hi1s1)                          0.14       5.79 f
__tmp107/c_out (fulladd_gate_5)                0.00       5.79 f
sum[8] (out)                                   0.00       5.79 f
data arrival time                                         5.79
-------------------------------------------------------------
(Path is unconstrained)
```

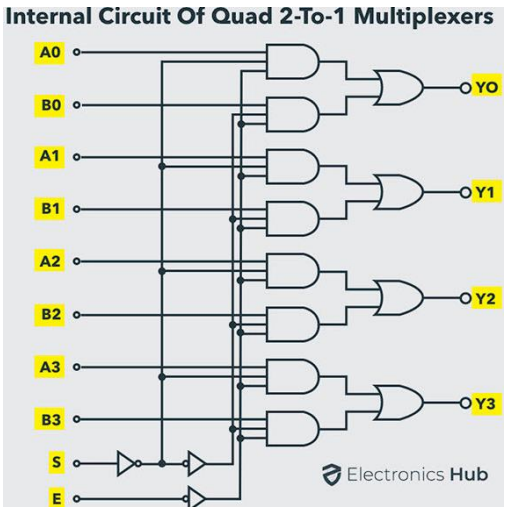
위의 Timing report는 순서대로 1bit, 2bit ,4bit ,8bit Adder이다. 이를 total data arrival time 을 이용하여 해당 값들을 fitting해보면,



<Fitting result>

위와 같고, 놀랍게도 R^2 value가 0.9999로, bit가 n배 될 때마다, delay가 n배 되는 것을 알 수 있었다. 이를 통하여, 1개의 Full adder가 갖는 Avg data arrival time 은 0.7245ns와 같고, FA의 개수가 증가할 때마다, 선형적으로 Timing이 증가하는 사실을 실험적으로 check할 수 있었다. -

이제 Mux에 대한 검증을 시작하자.



Mux는 input bit의 개수에 상관없이, 회로의 Critical path가 동일한 모습을 살펴볼 수 있다. 이를 검증하기 위하여 Design Vision에 Nbit MUX를 apply하여 timing을 측정하고, 그 result value를 check하자.

```
Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
s_in (in)                                0.00       0.00 r
m2/S (m21_30)                            0.00       0.00 r
m2/U1/Q (dsmxc31s1)                      0.41       0.41 f
m2/Y (m21_30)                            0.00       0.41 f
sum[1] (out)                             0.00       0.41 f
data arrival time                                   0.41
-----------------------------------------------------------
(Path is unconstrained)
```

```
Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
s_in (in)                                0.00       0.00 r
m4/S (m21_21)                            0.00       0.00 r
m4/U1/Q (dsmxc31s1)                      0.41       0.41 f
m4/Y (m21_21)                            0.00       0.41 f
sum[3] (out)                             0.00       0.41 f
data arrival time                                   0.41
-----------------------------------------------------------
(Path is unconstrained)
```

```
Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
s_in (in)                                0.00       0.00 r
m8/S (m21_33)                            0.00       0.00 r
m8/U1/Q (dsmxc31s1)                      0.41       0.41 f
m8/Y (m21_33)                            0.00       0.41 f
sum[6] (out)                             0.00       0.41 f
data arrival time                                   0.41
-----------------------------------------------------------
(Path is unconstrained)
```

위의 사진은 순서대로 2,4,7bit MUX의 timing report이다. 위의 Adder의 Result와 동일하게, Mux역시 예상한 그대로 constant timing을 보여주었다. 이를 이용하면, Adder는 bit에 비례하게 data arrival time(이하 DAT)이 증가하고, MUX는 constant DAT가 걸린다면, 수업에서 사용한 Idea인 Select adder를 사용할 수 있을 것이다. 이때, 우리는 Mux가 circuit에서 직전 gate의 output dependent하다는 것을 기억하자. adder의 경우엔 회로 전체 최고 bit수에 의지하지만, MUX는 design한 개수에 의존한다는 사실이다. 즉, MUX는 결국 이전 MUX의 output data에 의존하므로, 이 역시 개수에 Linear하게 증가한다. 결국 Adder는 bit에 Linear하게, MUX는 사용한 MUX개수에 Linear하게 증가한다는 사실을 알 수 있다. 그렇다면 두 가지 Result를 apply하여 1bit adder의 DAT를 0.7245ns로 쓰고, MUX의 DAT를 0.41ns로 쓰자. 이후 Optimization을 진행하기 위해 MUX의 개수를 fix하자. MUX의 개수가 0개이면 기본 26bit adder와 동일하고, 1개이면 13bit,13bit으로 쪼갤 수 있다. 2개이면 8 9 9 와 같다. 3개이면, 6 6 7 7과 동일하다. 4개인 경우, 44567과 같다. 5개인 경우, 334565와 같다. 이를 통해 SUM한 결과를 표로 나타내보자.

이제 Critical path를 분석하자. 이를 분석하기 위해 간략한 Select adder의 사진을 쓰자.

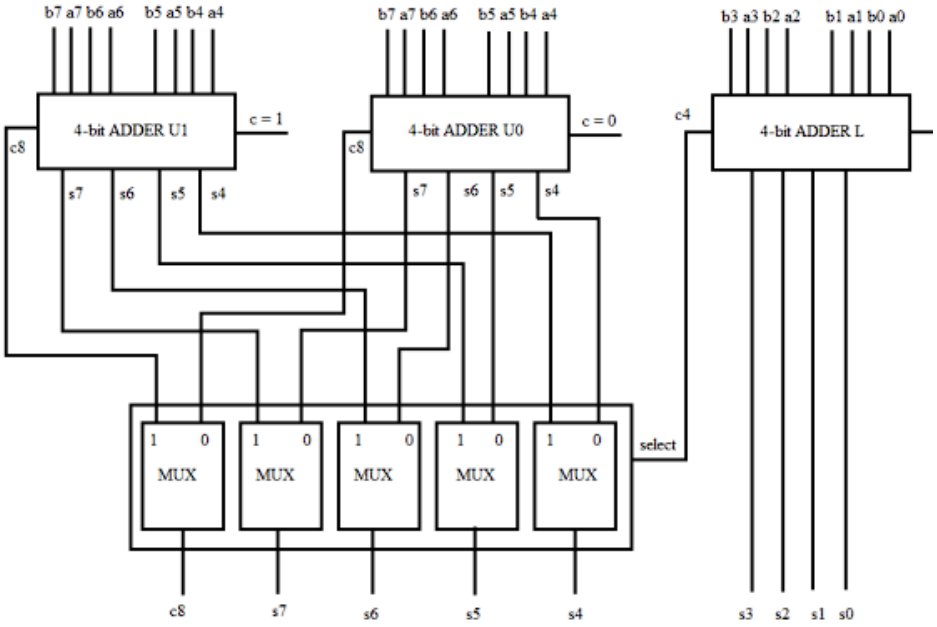


Fig1. *8-bit Carry Select Adder*

위의 사진은 8bit carry adder이다. 이번에는 마지막 bit로부터 따라서 올라가면, MUX에 input으로 들어오는 path들의 gate delay가 같고, 모든 input이 Simultaneous하게 apply 되는데, Mux에서 Output이 동시에 출력되므로 delay가 같다. 이를 이용하여 생각해보면, 마지막 MUX의 input으로 들어오는 bit들이 같은 정도의 Time delay를 가짐을 알 수 있다. 이를 통하여 마지막 Mux로 출력되는 모든 path가 모두 Critical path임을 알 수 있다. 실제로 위의 Timing report를 살펴보면, 다 output의 위치나 input의 위치가 계속 바뀌는 현상을 볼 수 있다.

이번엔 pipelining에 대하여 살펴보자. Pipeline architecture란 여러가지 operation을 병렬성을 apply하여 빠르게 작업하는 방법을 이야기한다. 보통 하나의 input으로부터 Critical path를 구하여 이를 N개의 stage로 나누는 방법으로 apply되며, 이를 통해 Clock frequency의 향상을 얻을 수 있다. 이를 살펴보기 위하여 이전과의 비교를 진행하기 위하여 표를 사용하면,

	Naïve 26bit RCA	Pipelined 26bit RCA	증감폭 [%]
Min clock period [ns]	6.50	3.90	66.7
Total cell area [μm^2]	26335	33534	27.3

Total dynamic power [mW]	4.71	9.76	107.2

	Naïve 20bit CSA	Pipelined 20bit CSA	증감폭 [%]
Min clock period [ns]	3.30	2.35	41.3
Critical path delay [ns]	3.82	2.87	-26.5
Total cell area [μm^2]	23796	35359	48.6
Total dynamic power [mW]	7.35	14.3	94.6

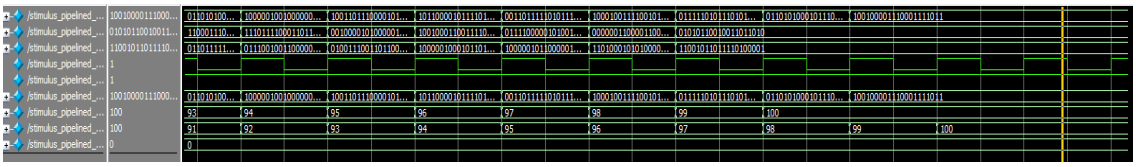
	Naïve 26bit RCA	Pipelined 26bit RCA	증감폭 [%]
Min clock period [ns]	3.30	2.90	14.0
Critical path delay [ns]	4.82	3.42	-29.1
Total cell area [μm^2]	37341	46631	24.9
Total dynamic power [mW]	12.2	15.3	25.4

위와 같다.

전체적으로 꽤나 큰 폭의 Clock period 향상을 얻을 수 있었는데, 기존 회로의 Complexity나 clock speed에 따라 향상 폭이 차이가 있음을 알 수 있었다. 특히 두드러지는 사실은, 성능 향상폭의 1.8x만큼 Dynamic power가 증가하는 모습이었는데, 이는 pipelining으로 circuit의 resistor및 기타 logic gate들의 Transition rate이 증가하고, 이에 따라 energy consumption이 증가하는 것으로 알 수 있다. 또한 pipelining으로 인하여 circuit의 operation frequency가 증가하기에, voltage와 current의 변화량 역시 증가하여 더 큰 energy consumption을 이끌어낸다. 이러한 문제를 해결하기 위해선 dynamic voltage scheduler 등을 이용하여 전력을 관리하기도 한다.

Area역시, Pipeline이 apply되면서, 자연스럽게 port가 증가하는 만큼 증가하고, 더 tight 하게 clock을 push하면서 더 큰 capacitor를 apply된다. 이에 따라 Area는 자연스럽게 증가하는 모습을 볼 수 있다. 특히나 20bit CSA는 dynamic voltage와 area가 유의미하게 크게 증가하는 모습을 볼 수 있었는데 이는 기존의 naïve한 26bit RCA에 비하여 performance 증가/ Energy consumption and Area improvement range 가 상대적으로 큰 것을 알 수 있다. 즉, 더 작은 성능증가를 얻어내기 위하여 더 큰 전력과 면적이 필요해짐을 의미한다. 이는 후에 회로를 설계할 때 고려할 만한 사항이라고 생각한다.

성능을 더 개선하기 위하여 기본적인 Verilog notation과 Architecture를 개선해보자. (개선되는 사항의 코드는 뒤에 부록으로 첨부하겠습니다.) 이전 3번 report에서 adder가 mux에 비하여 더 clock friendly한 모습을 보여주었다. 이를 이용하여 20bit pipelined CSA와 26bit pipelined CSA를 개선해보자. 또한 불필요한 port들을 줄이면서 Area나 Power가 개선되는지 살펴보자. 첫째로 20bit pipelined CSA에서 mux를 바꿔보자. 먼저 내가 사용했던 mux의 경우, 4bit mux 일 때에, carry 와 Sum을 동시에 계산하는 구조였는데, 이를 carry 와 sum을 분리하여 회로가 작동하도록 하면, 불필요한 mux의 area가 줄어들 것이라고 판단하였다. 이를 4bit mux, 2bit mux로 분리하여 block처럼 이용하자. 먼저 error가 0임을 check하면,



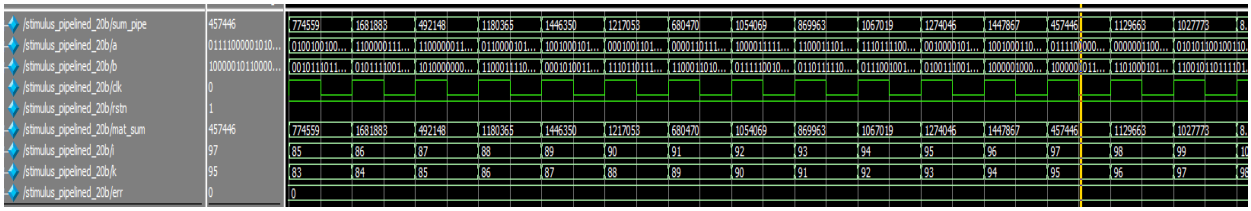
와 같고 error가 없음을 알 수 있었다. 하지만 random성이 있는 Synthesis에도, Power와 Area의 결과가 더 나빠지는 현상을 볼 수 있었다. (같은 Clk) 따라서 mux는 분리하지 않고, 그대로 사용하는 것이 더 나은 Area와 power consumption을 보여줌을 알 수 있었다.

```
Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  11.7503 mW   (79%)
  Net Switching Power  =   3.0981 mW   (21%)
                         ---------
Total Dynamic Power    =  14.8484 mW  (100%)

Cell Leakage Power     =   1.0304 uW

1
```

```
Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              64
Number of nets:              168
Number of cells:             105
Number of references:          6

Combinational area:      16986.931210
Noncombinational area:   19375.748581
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:         36362.679688
Total area:                undefined
1
```

이번에는 flip flop을 모듈화를 진행시켜 apply해보도록하자. Ref에 주어진 코드 20bit,21bit flipflop을 apply하니, area, clk speed, power까지 향상되었을 뿐 아니라 schematic역시 직관적으로 바뀌는 것을 볼 수 있었다. 이를 첨부하기 앞서 report 결과를

보면, 아래와 같이 error가 0임을 확인할 수 있다.



	Pipelined 20bit CSA	Pipelined 20bit CSA _improved	증감폭 [%]
Min clock period [ns]	2.35	2.20	6.9
Critical path delay [ns]	2.87	2.72	-5.4
Total cell area [μm^2]	35359	34173	4.3
Total dynamic power [mW]	14.3	16.2	13.3

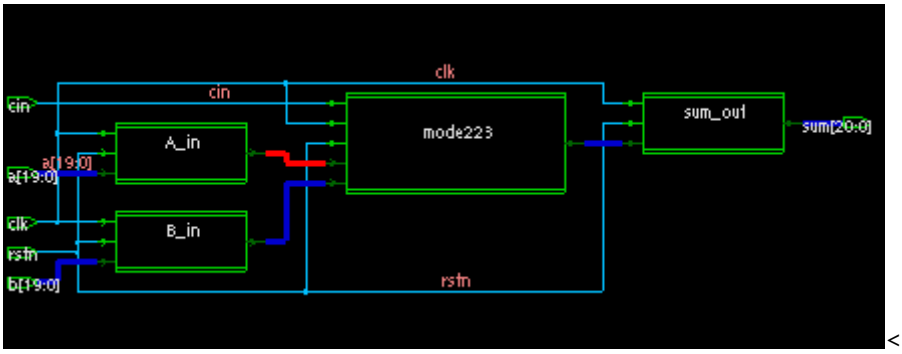
```
****************************************
Report : power
        -analysis_effort low
Design : carry_select_adder_20b_4444_pipe_1
Version: Z-2007.03-SP4
Date   : Thu Apr  6 01:56:51 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.d

Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top

Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  13.6308 mW   (84%)
  Net Switching Power  =   2.6104 mW   (16%)
                         ---------
Total Dynamic Power    =  16.2413 mW  (100%)

Cell Leakage Power     = 933.1904 nW
```

```
****************************************
Report : area
Design : carry_select_adder_20b_4444_pipe_1
Version: Z-2007.03-SP4
Date   : Thu Apr  6 01:55:41 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db)

Number of ports:              64
Number of nets:              125
Number of cells:               4
Number of references:          4

Combinational area:      14946.511211
Noncombinational area:   19226.438934
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:         34172.949219
Total area:                undefined
1
```

```
)perating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top

  Startpoint: A_in/q_reg[12]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: mode223/qsum1_reg[15]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  ----------------------------------------------------------------------
  clock clk (rise edge)                                   1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  A_in/q_reg[12]/CLK (dffcs2)                             0.00       1.00 r
  A_in/q_reg[12]/QN (dffcs2)                              0.25       1.25 f
  A_in/q_reg[12]/Q (dffcs2)                               0.14       1.39 r
  A_in/q[12] (d_ff_20b_4)                                 0.00       1.39 r
  mode223/a[12] (carry_select_adder_20b_pipe)             0.00       1.39 r
  mode223/ad4/a[0] (d4_adder_6)                           0.00       1.39 r
  mode223/ad4/fa1/a[0] (fulladd4_gate_13)                 0.00       1.39 r
```

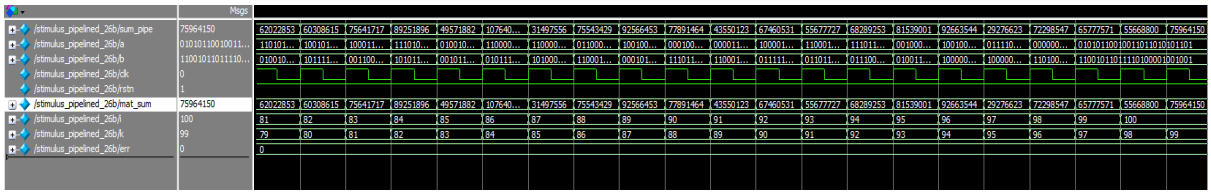
```
mode223/a[12] (carry_select_adder_20b_pipe)             0.00       1.39 r
mode223/ad4/a[0] (d4_adder_6)                           0.00       1.39 r
mode223/ad4/fa1/a[0] (fulladd4_gate_13)                 0.00       1.39 r
mode223/ad4/fa1/gt1/a (fulladd_gate_88)                 0.00       1.39 r
mode223/ad4/fa1/gt1/U1/Q (oai21s2)                      0.25       1.64 f
mode223/ad4/fa1/gt1/U4/Q (nnd2s2)                       0.20       1.84 r
mode223/ad4/fa1/gt1/c_out (fulladd_gate_88)             0.00       1.84 r
mode223/ad4/fa1/gt2/c_in (fulladd_gate_87)              0.00       1.84 r
mode223/ad4/fa1/gt2/U2/Q (aoi22s3)                      0.19       2.03 f
mode223/ad4/fa1/gt2/U4/Q (ils3)                         0.12       2.15 r
mode223/ad4/fa1/gt2/c_out (fulladd_gate_87)             0.00       2.15 r
mode223/ad4/fa1/gt3/c_in (fulladd_gate_86)              0.00       2.15 r
mode223/ad4/fa1/gt3/U2/Q (nnd2s2)                       0.10       2.25 f
mode223/ad4/fa1/gt3/U1/Q (nnd2s2)                       0.16       2.40 r
mode223/ad4/fa1/gt3/c_out (fulladd_gate_86)             0.00       2.40 r
mode223/ad4/fa1/gt4/c_in (fulladd_gate_85)              0.00       2.40 r
mode223/ad4/fa1/gt4/U1/Q (xor2s2)                       0.31       2.72 r
mode223/ad4/fa1/gt4/sum (fulladd_gate_85)               0.00       2.72 r
mode223/ad4/fa1/sum[3] (fulladd4_gate_13)               0.00       2.72 r
mode223/ad4/sum1[3] (d4_adder_6)                        0.00       2.72 r
mode223/qsum1_reg[15]/DIN (dffles1)                     0.00       2.72 r
data arrival time                                                  2.72

clock clk (rise edge)                                   3.20       3.20
clock network delay (ideal)                             0.00       3.20
mode223/qsum1_reg[15]/CLK (dffles1)                     0.00       3.20 r
library setup time                                     -0.48       2.72
data required time                                                 2.72
----------------------------------------------------------------------
data required time                                                 2.72
data arrival time                                                 -2.72
----------------------------------------------------------------------

slack (MET)                                                        0.00
```

더불어 더 나은 schematic을 얻을 수 있었다.



<20bit CSA schematic>

이를 통해 Flipflop을 module로써, 일종의 block처럼 활용하는 것과 Mux는 묶어서 사용하는 것이 더 나은 performance를 보여주는 것을 알 수 있었다. 이를 26bit CSA에도 apply해보자. Verification을 먼저 진행하면 아래와 같이 error가 0가 되는 것을 볼 수 있다.



	Pipelined 26bit CSA	Pipelined 26bit CSA _improved	증감폭 [%]
Min clock period [ns]	2.90	2.65	8.7
Critical path delay [ns]	3.42	3.17	-7.4
Total cell area [μm^2]	46631	43255	-7.3
Total dynamic power [mW]	15.3	16.5	7.8

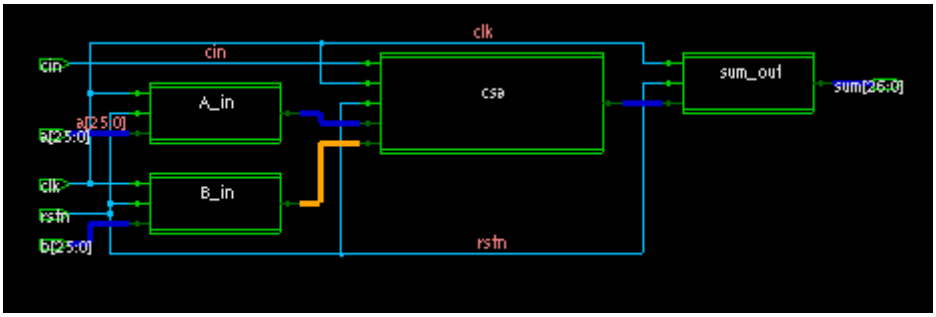
```
Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25

Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  14.5200 mW   (88%)
  Net Switching Power  =   2.0187 mW   (12%)
                         ---------
Total Dynamic Power    =  16.5387 mW  (100%)

Cell Leakage Power     =   1.2149 uW

1
```

```
****************************************
Report : area
Design : carryselectadder1234
Version: Z-2007.03-SP4
Date   : Thu Apr  6 04:21:45 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.

Number of ports:              82
Number of nets:              161
Number of cells:               4
Number of references:          4

Combinational area:      18620.928417
Noncombinational area:   24634.369095
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:         43255.296875
Total area:                undefined
```

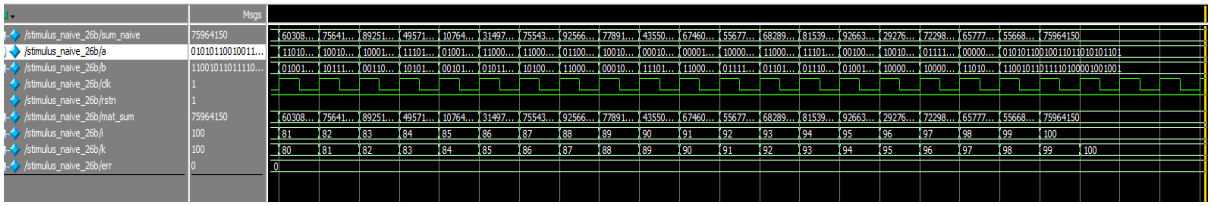
```
Startpoint: B_in/q_reg[16]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: csa/qs21/q_reg[21]
            (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                    1.00       1.00
clock network delay (ideal)                              0.00       1.00
B_in/q_reg[16]/CLK (dffcs2)                              0.00       1.00 r
B_in/q_reg[16]/QN (dffcs2)                               0.25       1.25 f
B_in/q_reg[16]/Q (dffcs2)                                0.13       1.38 r
B_in/q[16] (d_ff_26b_3)                                  0.00       1.38 r
csa/b[16] (carry_select_adder_26b_223456)                0.00       1.38 r
csa/ad5/b[0] (d6_adder)                                  0.00       1.38 r
csa/ad5/fa2/b[0] (fulladd6_gate_1)                       0.00       1.38 r
csa/ad5/fa2/gt1/b (fulladd_gate_14)                      0.00       1.38 r
csa/ad5/fa2/gt1/U4/Q (xor2s2)                            0.35       1.74 r
csa/ad5/fa2/gt1/U2/Q (aoi22s3)                           0.17       1.91 f
csa/ad5/fa2/gt1/U5/Q (i1s3)                              0.11       2.02 r
csa/ad5/fa2/gt1/c_out (fulladd_gate_14)                  0.00       2.02 r
csa/ad5/fa2/gt2/c_in (fulladd_gate_13)                   0.00       2.02 r
csa/ad5/fa2/gt2/U1/Q (nnd2s2)                            0.13       2.15 f
csa/ad5/fa2/gt2/U6/Q (nnd2s3)                            0.12       2.27 r
csa/ad5/fa2/gt2/c_out (fulladd_gate_13)                  0.00       2.27 r
csa/ad5/fa2/gt3/c_in (fulladd_gate_12)                   0.00       2.27 r
csa/ad5/fa2/gt3/U5/Q (nnd2s3)                            0.10       2.37 f
csa/ad5/fa2/gt3/U4/Q (nnd2s3)                            0.14       2.51 r
csa/ad5/fa2/gt3/c_out (fulladd_gate_12)                  0.00       2.51 r
csa/ad5/fa2/gt4/c_in (fulladd_gate_11)                   0.00       2.51 r
csa/ad5/fa2/gt4/U5/Q (nnd2s3)                            0.10       2.61 f
csa/ad5/fa2/gt4/U4/Q (nnd2s3)                            0.12       2.72 r
csa/ad5/fa2/gt4/c_out (fulladd_gate_11)                  0.00       2.72 r
csa/ad5/fa2/gt5/c_in (fulladd_gate_10)                   0.00       2.72 r
csa/ad5/fa2/gt5/U2/Q (nnd2s3)                            0.10       2.82 f
csa/ad5/fa2/gt5/U4/Q (nnd2s3)                            0.10       2.93 r
csa/ad5/fa2/gt5/c_out (fulladd_gate_10)                  0.00       2.93 r
csa/ad5/fa2/gt6/c_in (fulladd_gate_9)                    0.00       2.93 r
csa/ad5/fa2/gt6/U1/Q (xor2s2)                            0.24       3.17 r
csa/ad5/fa2/gt6/sum (fulladd_gate_9)                     0.00       3.17 r
csa/ad5/fa2/sum[5] (fulladd6_gate_1)                     0.00       3.17 r
csa/ad5/sum2[5] (d6_adder)                               0.00       3.17 r
csa/qs21/d[21] (d_ff_26b_1)                              0.00       3.17 r
csa/qs21/q_reg[21]/CLRB (dffcs1)                         0.00       3.17 r
data arrival time                                                   3.17

clock clk (rise edge)                                    3.65       3.65
clock network delay (ideal)                              0.00       3.65
csa/qs21/q_reg[21]/CLK (dffcs1)                          0.00       3.65 r
library setup time                                      -0.48       3.17
data required time                                                  3.17
-----------------------------------------------------------------------------
data required time                                                  3.17
data arrival time                                                  -3.17
-----------------------------------------------------------------------------
slack (MET)                                                         0.00
```

위에서 적용한 기법으로 다시 26bit CSA에 apply해본 결과, Area와 performance가 대폭 증가한 것을 알 수 있었다. 이를 통해, Flipflop은 module화하여 block처럼 사용하는 것이 design compiler의 expectation value를 높여줄 수 있음을 알 수 있었다.

또한 schematic 역시, 더욱 직관적으로 볼 수 있도록 바꿀 수 있었다.



이 기법을 26bit pipelined RCA에 apply하자. 먼저 verification을 진행하면, error가 0임을 확인할 수 있다. (이 때, module이 naïve RCA라고 되어있는데 code로 첨부하겠습니다. Pipelined RCA입니다.)



	Pipelined 26bit RCA	Pipelined 26bit RCA _improved	증감폭 [%]
Min clock period [ns]	3.90	3.50	11.3
Total cell area [μm^2]	33534	31411	-6.3
Total dynamic power [mW]	9.76	9.13	-6.4

```
****************************************
Report : area
Design : carryselectadder1
Version: Z-2007.03-SP4
Date   : Thu Apr  6 04:50:10 2023
****************************************

Library(s) Used:

    lec25dscc25_SS (File: /home/admin/lib/lec25/lec25dscc25_SS.db

Number of ports:              82
Number of nets:              161
Number of cells:               4
Number of references:          4

Combinational area:      18139.854279
Noncombinational area:   13271.042084
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:         31410.896484
Total area:                undefined
1
```

```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top


Global Operating Voltage = 2.25
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   7.5496 mW   (83%)
  Net Switching Power  =   1.5817 mW   (17%)
                         ---------
Total Dynamic Power    =   9.1313 mW  (100%)

Cell Leakage Power     = 892.7196 nW
```

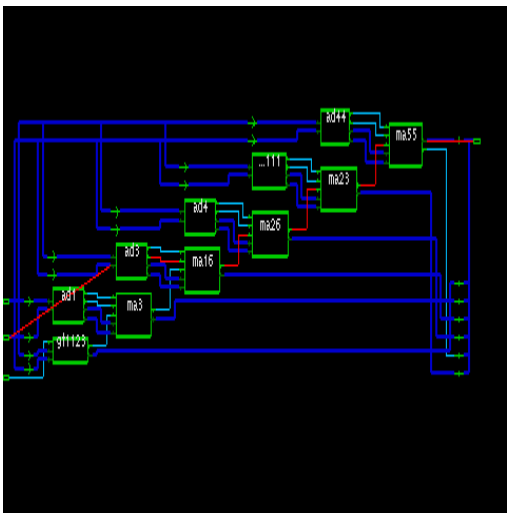
```
csa/ma26/m5/U3/Q (mxi21s3)                          0.28       3.38 f
csa/ma26/m5/Y (m21_13)                              0.00       3.38 f
csa/ma26/c (mux_add4to1_2)                          0.00       3.38 f
csa/ma23/s_in (mux_add4to1_1)                       0.00       3.38 f
csa/ma23/m5/S (m21_8)                               0.00       3.38 f
csa/ma23/m5/U3/Q (mxi21s3)                          0.34       3.72 r
csa/ma23/m5/Y (m21_8)                               0.00       3.72 r
csa/ma23/c (mux_add4to1_1)                          0.00       3.72 r
csa/ma55/s_in (mux_add6to1)                         0.00       3.72 r
csa/ma55/m2/S (m21_6)                               0.00       3.72 r
csa/ma55/m2/U1/Q (mxi21s2)                          0.28       4.00 f
csa/ma55/m2/Y (m21_6)                               0.00       4.00 f
csa/ma55/sum[1] (mux_add6to1)                       0.00       4.00 f
csa/sum[21] (carry_select_adder_26b_4444)           0.00       4.00 f
sum_out/d[21] (d_ff_27b)                            0.00       4.00 f
sum_out/q_reg[21]/CLRB (dffcs1)                     0.00       4.00 f
data arrival time                                              4.00

clock clk (rise edge)                               4.50       4.50
clock network delay (ideal)                         0.00       4.50
sum_out/q_reg[21]/CLK (dffcs1)                      0.00       4.50 r
library setup time                                 -0.50       4.00
data required time                                             4.00
-----------------------------------------------------------------------------
data required time                                             4.00
data arrival time                                             -4.00
-----------------------------------------------------------------------------
slack (MET)                                                    0.00
```

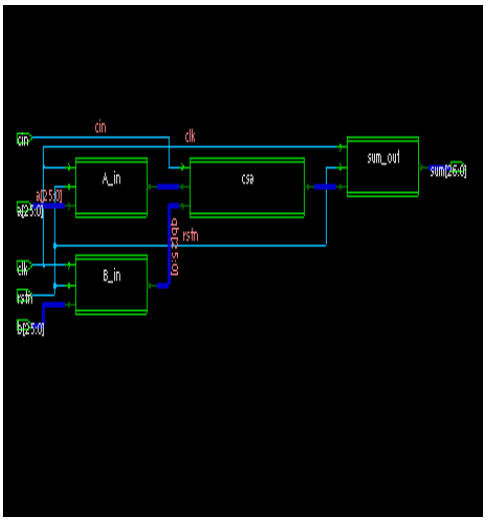
```
Operating Conditions: nom_pvt   Library: lec25dscc25_SS
Wire Load Model Mode: top

  Startpoint: B_in/q_reg[8]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: sum_out/q_reg[21]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    1.00       1.00
  clock network delay (ideal)              0.00       1.00
  B_in/q_reg[8]/CLK (dffcs2)               0.00       1.00 r
  B_in/q_reg[8]/QN (dffcs2)                0.25       1.25 f
  B_in/q_reg[8]/Q (dffcs2)                 0.17       1.43 r
  B_in/w[8] (d_ff_26b_1)                   0.00       1.43 r
```

위와 같이 이번에는 performance, Area , power consumption까지 개선된 모습을 보였다.

위에서 적용한 기법으로 다시 26bit RCA에 apply해본 결과, Area와 performance가 대폭 증가한 것을 알 수 있었다. 이를 통해, Flipflop은 module화하여 block처럼 사용하는 것이 design compiler의 expectation value를 높여줄 수 있음을 알 수 있었다.

또한 schematic 역시, 더욱 직관적으로 볼 수 있도록 바꿀 수 있었다.





마지막으로 회로의 본질적으로 중요한 점인 Verification을 보자. Test bench는 내가 verification하는 design의 input을 만들어 주어야 하며, Reference model과 동일하게 operation하는지 output을 check하는 부분으로 이루어져 있다. Operating 시나리오를 기반으로 test case의 constraint를 만들고 그 안에서 random한 input을 apply한다. 이를 마지막 score board에서 Wave form으로 check하며, RTL algorithm이 동일하게 구현되었는지 error를 check한다 IP의 모든 부분이 connected 되었는지 check하기 위하여 coverage를

check하는 것도 필요하다. 이제 Verification 결과를 간단하게 확인하자. 우리는 Matlab을 통하여 input과 해당 value 간의 덧셈을 이용한 output 결과를 만들었다. 즉, 앞서 언급한 operating 시나리오를 위한 constraint를 matlab을 통하여 txt로 만든 것이다. 이를 testbench file에 apply하고, 앞에서 본 결과를 살펴보면 먼저 a와 b의 sum이 잘 되었는지 확인하기 위하여 시나리오 상의 output constraint와 실제 회로의 output과 비교를 진행했고, 이후 해당 값과 오차를 error로 출력하였다. 앞의 Testbench의 결과로 clk를 apply한 것의 유무에 관계없이, error가 0을 유지하는 것을 볼 수 있다. 이를 통하여 회로의 logic이 26bit adder의 역할을 잘 수행하고 있음을 알 수 있었다.

(4) Conclusion

해당 실습에서 중요한 요소인 Pipe lining은 circuit의 flow를 parallelize시켜, circuit의 performance를 증가시키는 요인으로 작용하였다. 해당 방법의 critical point는 각 stage별로 execution time이 동일한, 즉 각 단계가 같은 수의 stage로 이루어져야 한다는 사실이었다. 해당 지점에 오류가 생기면 이를 Hazard라고 한다. 실제로 내가 코드를 하는 과정에서 stage를 생각하지 않고 code를 apply했다가 bit가 하나씩 밀리는 hazard가 발생했었다. 이러한 data hazard를 방지하기 위하여 dff를 추가하면서 stage 수를 계산하고 circuit의 verification을 확인할 수 있었다.

Pipelining은 circuit의 overall performance를 크게 향상시키고, Area와 Dynamic Voltage를 증가시키는 성질이 있음을 확인할 수 있었다. 또한 기존 circuit의 성능을 향상시키기 위하여 모듈화와, MUX를 한 번에 묶는 시도를 하여 성능의 큰 향상을 얻을 수 있었다. 이를 통해 pipelining과 위의 시도들로 얻어진 최종적 성능 증가를 표로 나타내면,

	Naïve 26bit RCA	Pipelined 26bit RCA _improved	증가율 [%]
Min clock period [ns]	6.50	3.50	86.2
Total cell area [μm^2]	26335	31411	19.2
Total dynamic power [mW]	4.71	9.13	93.8

	Naïve 26bit RCA	Pipelined 26bit CSA _improved	증가율 [%]
Min clock period [ns]	3.30	2.65	24.5
Critical path delay [ns]	4.82	3.17	-34.3
Total cell area [μm^2]	37341	43255	-7.3
Total dynamic power [mW]	12.2	16.5	35.2

	Naïve 20bit CSA	Pipelined 20bit CSA _improved	증가율 [%]
Min clock period [ns]	3.30	2.20	50.0
Critical path delay [ns]	3.82	2.72	-28.8
Total cell area [μm^2]	23796	34173	42.8
Total dynamic power [mW]	7.35	16.2	124

와 같았다. 간단하게 여기서 흥미로운 사실은 26bit adder(CSA,RCA)의 경우 간단한 Total energy 계산인 Power * critical path delay 의 경우 RCA 의 경우 11.1% , 3.21%가 개선되었다는 사실이다. 이는 성능도 증가하였지만, 전력 효율면에서도 같은 작업량을 처리하는데 더 나은 결과를 가졌다는 사실로 받아들일 수 있었다. 즉, pipelining 과 notation 의 개선을 통하여 성능과 전력효율 모두를 잡은 셈이 된다. 하지만 pipelining 과 더 tight 한 clock pushing 등으로 면적의 증가는 막아낼 수 없는 것으로 판단하였다.

(5) Reference

Verilog HDL -joseph Cavanagh

Verilog HDL 이론 -한양대학교 전자전기공학부

Quora- CPU clock speed vs power vs area

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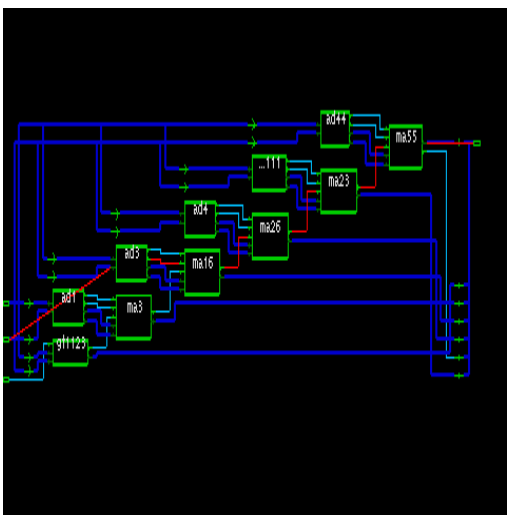
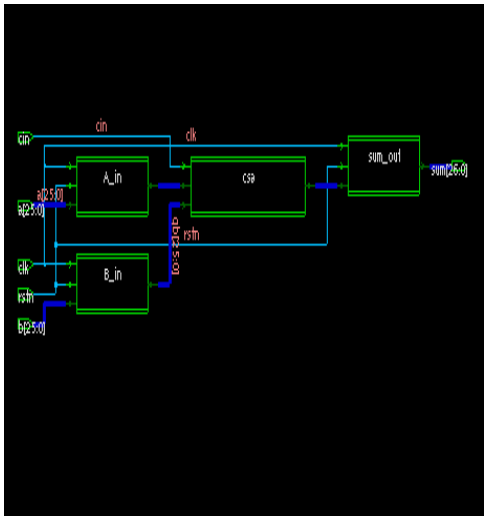
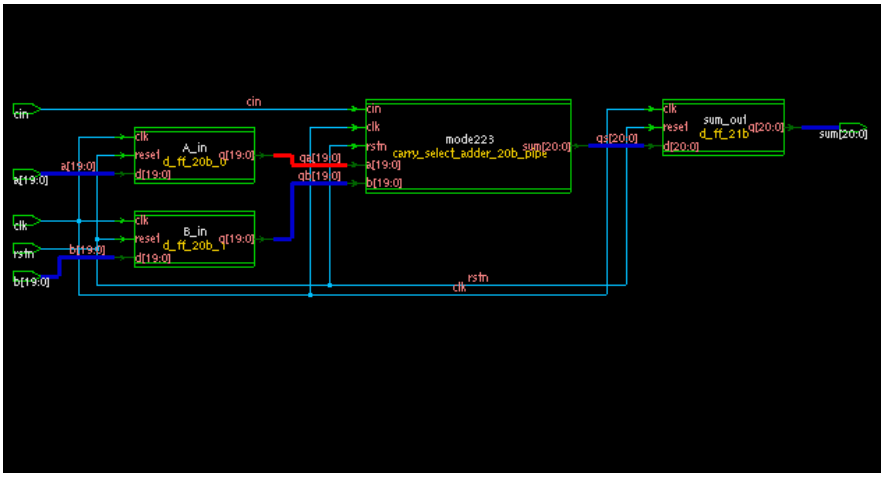
(6) 추가자료-schematics

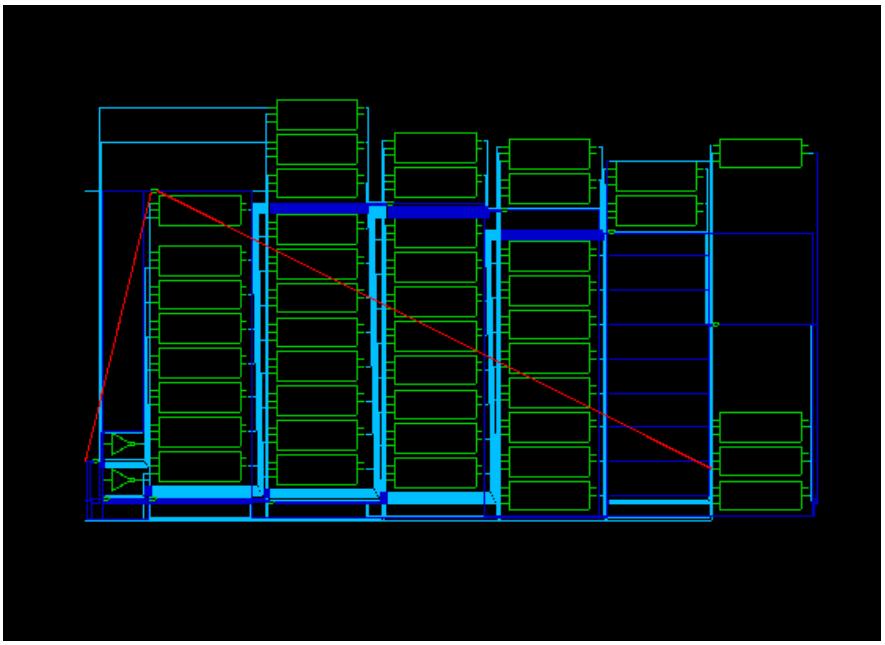
1. 26bit Adder pipelined



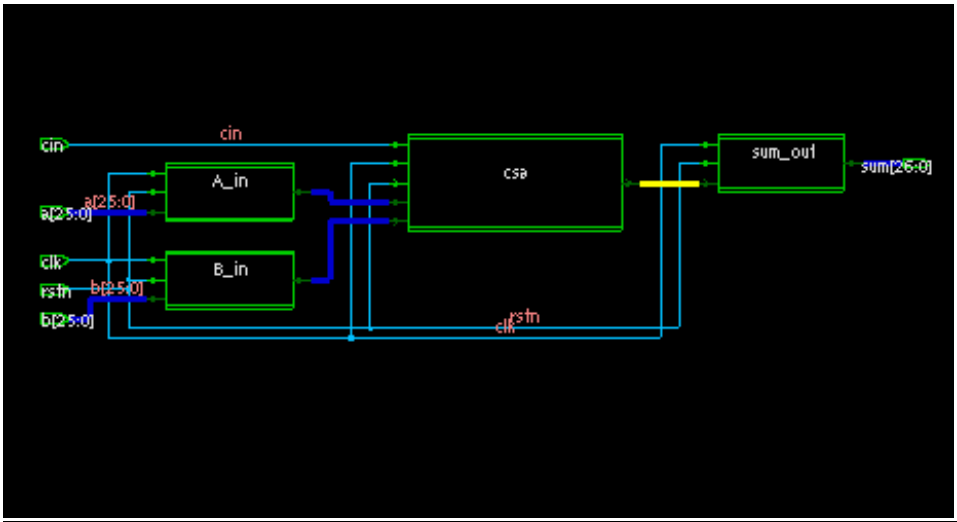


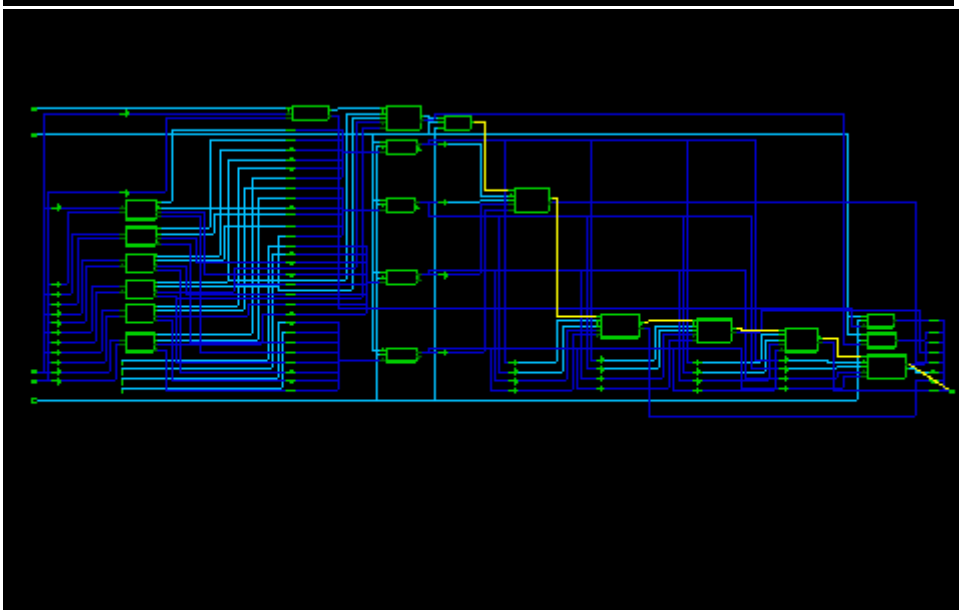
2. 20bit pipelined CSA





3. 26bit piped CSA (2234564)





4. 개선사항

1. D_FF 개선 전

```
        carry_select_adder_26b_44567 csa(qs,qa,qb,cin);

        always @ (negedge clk)
if(reset)
begin
qa <= 26'b00000000000000000000000000; qb<=26'b00000000000000000000000000;
end
else

begin
qa <= a; qb <= b; sum<=qs;
end


endmodule
```

➔ Main circuit 내부에서 별도의 D_FF

2. D_FF 개선 후

```
d_ff_20b A_in(qa,a,clk,rstn);
d_ff_20b B_in(qb,b,clk,rstn);
carry_select_adder_20b_pipe mode223(qs,qa,qb,cin,clk,rstn);
d_ff_21b sum_out(sum,qs,clk,rstn);

endmodule

 module d_ff_20b (
        output reg [19:0] q,
        input  [19:0] d,
        input clk,
        input reset
      );

   always @ (posedge clk)
   begin
     if(reset) q <= d;
     else      q <= 20'b0;
   end

endmodule

module d_ff_21b (
        output reg [20:0] q,
        input  [20:0] d,
        input clk,
        input reset
      );

   always @ (posedge clk)
   begin
     if(reset) q <= d;
     else      q <= 21'b0;
   end

endmodule
```

➔ D_FF module 로 사용

3. MUX 개선 전

```
mux_2to1_1b MUX_C_STAGE_2(.out(c_mux_sel[1]), .in0(p_c_temp_0[0]), .in1(p_c_temp_1[0]), .sel(p_c_mux_sel));
mux_2to1_1b MUX_C_STAGE_3(.out(c_mux_sel[2]), .in0(p_c_temp_0[1]), .in1(p_c_temp_1[1]), .sel(c_mux_sel[1]));
mux_2to1_1b MUX_C_STAGE_4(.out(c_mux_sel[3]), .in0(p_c_temp_0[2]), .in1(p_c_temp_1[2]), .sel(c_mux_sel[2]));
mux_2to1_1b MUX_C_STAGE_5(.out(sum[20]),      .in0(p_c_temp_0[3]), .in1(p_c_temp_1[3]), .sel(c_mux_sel[3]));


mux_2to1_4b MUX_SUM_STAGE_2(.out(sum[7:4]),   .in0(p_sum_temp_0[7:4]),   .in1(p_sum_temp_1[7:4]),   .sel(p_c_mux_s
mux_2to1_4b MUX_SUM_STAGE_3(.out(sum[11:8]),  .in0(p_sum_temp_0[11:8]),  .in1(p_sum_temp_1[11:8]),  .sel(c_mux_sel
mux_2to1_4b MUX_SUM_STAGE_4(.out(sum[15:12]), .in0(p_sum_temp_0[15:12]), .in1(p_sum_temp_1[15:12]), .sel(c_mux_sel
mux_2to1_4b MUX_SUM_STAGE_5(.out(sum[19:16]), .in0(p_sum_temp_0[19:16]), .in1(p_sum_temp_1[19:16]), .sel(c_mux_sel
```

➔ Carry 와 Sum 분리

4. Mux 개선 후

```
        assign sum[3:0] = qs;
        mux_add4to1 ml1(sum[7:4],qsum1[7:4],qsum2[7:4],c[1],qc1[0],qc2[0],qc);
        mux_add4to1 ml2(sum[11:8],qsum1[11:8],qsum2[11:8],c[2],qc1[1],qc2[1],c[1]);
        mux_add4to1 ml3(sum[15:12],qsum1[15:12],qsum2[15:12],c[3],qc1[2],qc2[2],c[2]);
        mux_add4to1 ml4(sum[19:16],qsum1[19:16],qsum2[19:16],sum[20],qc1[3],qc2[3],c[3]);
endmodule
module mux_add4to1(sum,s1,s2,c,c1,c2,s_in);
        output [3:0]sum;
        input [3:0] s1,s2;
        input s_in,c1,c2;
        output c;
        m21 m1(sum[0],s1[0],s2[0],s_in);
        m21 m2(sum[1],s1[1],s2[1],s_in);
        m21 m3(sum[2],s1[2],s2[2],s_in);
        m21 m4(sum[3],s1[3],s2[3],s_in);
        m21 m5(c,c1,c2,s_in);
```

➔ Carry 와 SUM 을 Simultaneous 하게 integrate