

# M2GL/M2S-EVAL-KIT

## DVP-100-000402-002 RevF

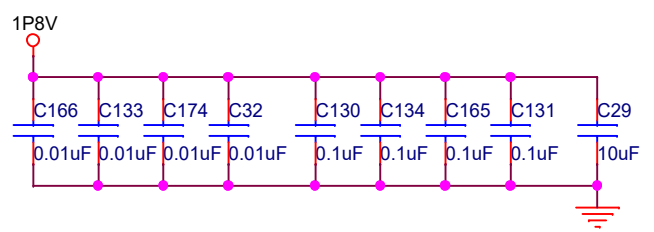
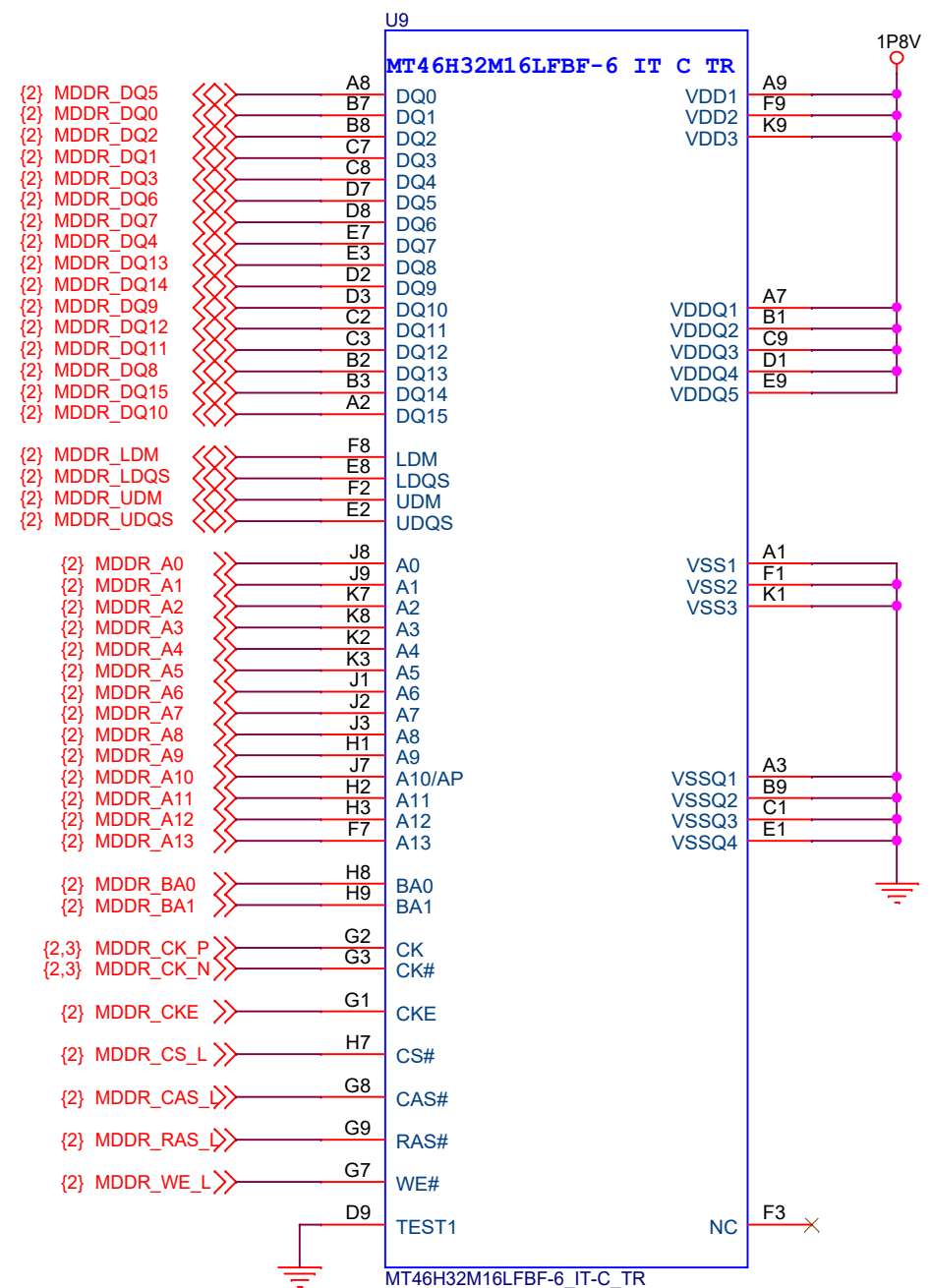
Microsemi Corporation	
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A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.



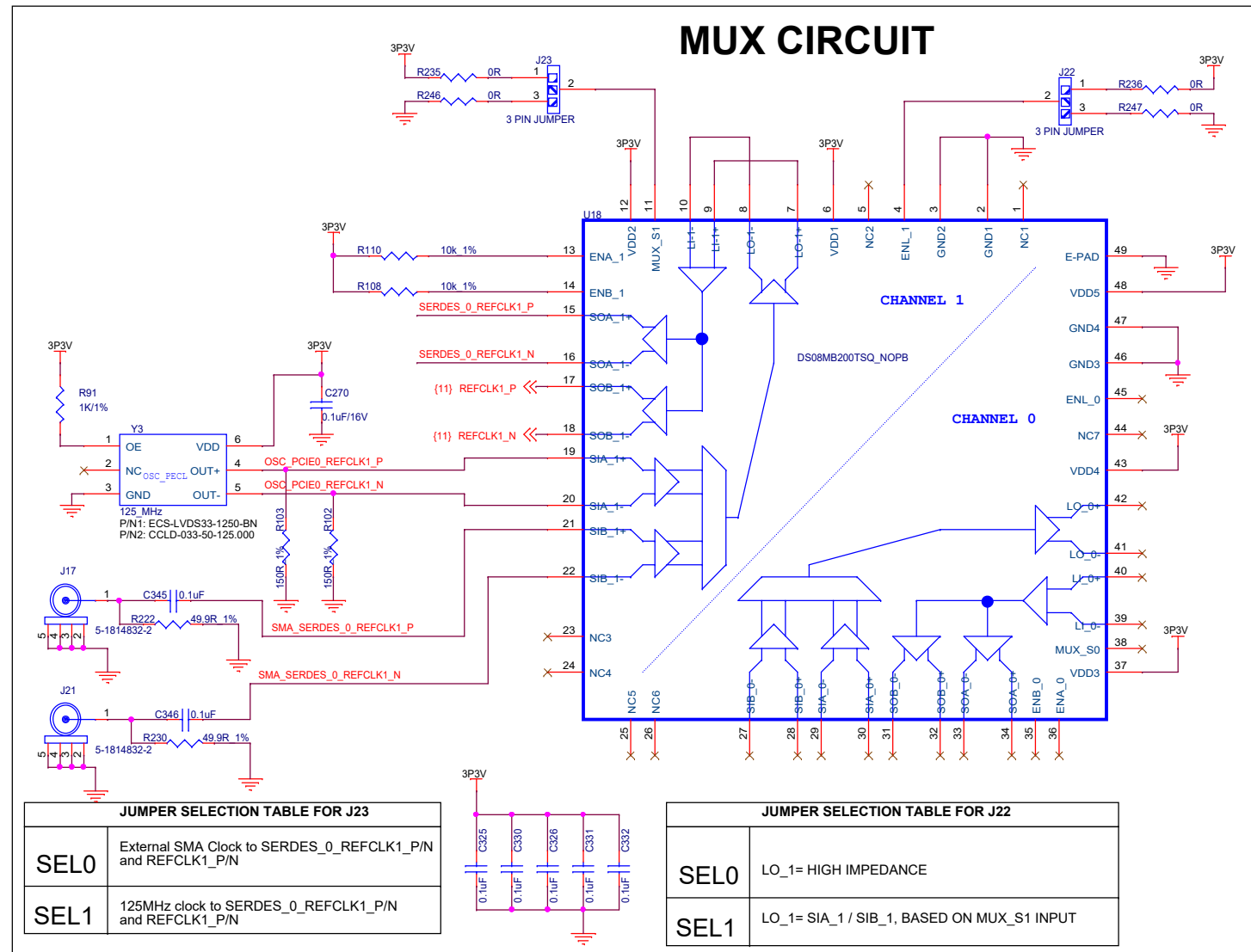
<b>TITLE</b> M2GL/M2S-EVAL-KIT			
<b>Microsemi</b>			
<b>SIZE</b> Custom	<b>DOCUMENT NO.</b>		<b>REV</b> F
<b>DATE:</b> Tuesday, May 09, 2023		<b>SH 2 OF 21</b>	

# LPDDR MEMORY INTERFACE



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# MUX CIRCUIT



JUMPER SELECTION TABLE FOR J22	
SEL0	LO_1= HIGH IMPEDANCE
SEL1	LO_1= SIA_1 / SIB_1, BASED ON MUX_S1 INPUT

# BANK1 & BANK2 CONNECTIONS

## BANK 1

MSIO22NB1/MMUART\_1\_RXD/GPIO\_26\_B/USB\_DATA3\_C  
MSIO21NB1/MMUART\_1\_TXD/GPIO\_24\_B/USB\_DATA2\_C

MSIO21PB1/GB5/USB\_XCLK\_C

MSIO22PB1/GB6/MMUART\_1\_CLK/GPIO\_25\_B/USB\_DATA4\_C  
MSIO23PB1/MMUART\_0\_RTS/GPIO\_17\_B/USB\_DATA5\_C  
MSIO23NB1/MMUART\_0\_DTR/GPIO\_18\_B/USB\_DATA6\_C  
MSIO24PB1/MMUART\_0\_CTS/GPIO\_19\_B/USB\_DATA7\_C  
MSIO24NB1/MMUART\_0\_DSR/GPIO\_20\_B  
MSIO25PB1/MMUART\_0\_RI/GPIO\_21\_B  
MSIO25NB1/MMUART\_0\_DCD/GPIO\_22\_B  
MSIO26NB1/MMUART\_0\_TXD/GPIO\_27\_B/USB\_DIR\_C  
MSIO27PB1/MMUART\_0\_RXD/GPIO\_28\_B/USB\_STP\_C  
MSIO27NB1/MMUART\_0\_CLK/GPIO\_29\_B/USB\_NXT\_C

MSIO28NB1/I2C\_0\_SCL/GPIO\_31\_B/USB\_DATA1\_C  
MSIO28PB1/I2C\_0\_SDA/GPIO\_30\_B/USB\_DATA0\_C

NC\_30  
NC\_31  
NC\_32  
NC\_33  
NC\_34  
NC\_35

M2GL/M2S010T-1FGG484

## BANK 2

{8} SPI\_SCK >> N19  
{8} SPI\_SDI << N20  
{8} SPI\_SDO << N21  
{8} SPI\_SS >> N22  
{8} SPI\_WP >> L16  
{8} SPI\_RESET >> K15  
MSIO7PB3\_K17 >> P16  
MSIO7NB3\_P16 >> N16  
(4) PCIE1\_PERSTn << P18

MSIO12PB2/SPI\_0\_CLK/USB\_XCLK\_A  
MSIO12NB2/SPI\_0\_SDI/GPIO\_5\_A/USB\_DIR\_A  
MSIO13PB2/SPI\_0\_SDO/GPIO\_6\_A/USB\_STP\_A  
MSIO13NB2/SPI\_0\_SS0/GPIO\_7\_A/USB\_NXT\_A  
MSIO18PB2/SPI\_0\_SS1/GPIO\_8\_A/USB\_DATA5\_A  
MSIO18NB2/SPI\_0\_SS2/GPIO\_9\_A/USB\_DATA6\_A  
MSIO19PB2/SPI\_0\_SS3/GPIO\_10\_A/USB\_DATA7\_A  
MSIO7NB2/CAN\_TX/GPIO\_2\_A/USB\_DATA0\_A  
MSIO8PB2/CAN\_RX/GPIO\_3\_A/USB\_DATA1\_A  
MSIO8NB2/CAN\_TX\_EN\_N/GPIO\_4\_A/USB\_DATA2\_A

MSIO6NB2  
MSIO0PB2

NC\_29  
NC\_30  
NC\_31  
NC\_32  
NC\_33  
NC\_34

M2GL/M2S010T-1FGG484

MSIO3PB2/USB\_DATA0\_B  
MSIO3NB2/USB\_DATA1\_B  
MSIO4PB2/USB\_DATA2\_B  
MSIO4NB2/USB\_DATA3\_B  
MSIO5PB2/USB\_DATA4\_B  
MSIO5NB2/USB\_DATA5\_B  
MSIO6PB2/USB\_DATA6\_B  
MSIO0NB2/USB\_DATA7\_B  
MSIO1NB2/USB\_DIR\_B  
MSIO1PB2/USB\_XCLK\_B  
MSIO2NB2/USB\_NXT\_B  
MSIO2PB2/USB\_STP\_B  
MSIO7PB2

V22 >> USB\_DATA0 {10}  
V21 >> USB\_DATA1 {10}  
U22 >> USB\_DATA2 {10}  
U21 >> USB\_DATA3 {10}  
T20 >> USB\_DATA4 {10}  
T21 >> USB\_DATA5 {10}  
P17 >> USB\_DATA6 {10}  
V19 >> USB\_DATA7 {10}  
R18 >> USB\_DIR {10}  
R17 >> USB\_CLKOUT {10}  
T19 >> USB\_NXT {10}  
T18 >> USB\_STP {10}  
R16 >> MSIO7PB3\_R16

R22 >> I2C1\_SCL {8}  
P22 >> I2C1\_SDA {8}

MSIO15NB2/SPI\_1\_SS0/GPIO\_13\_A  
MSIO19NB2/SPI\_1\_SS1/GPIO\_14\_A  
MSIO20PB2/SPI\_1\_SS2/GPIO\_15\_A  
MSIO20NB2/SPI\_1\_SS3/GPIO\_16\_A  
MSIO16PB2/SPI\_1\_SS4/GPIO\_17\_A  
MSIO16NB2/SPI\_1\_SS5/GPIO\_18\_A  
MSIO17PB2/SPI\_1\_SS6/GPIO\_23\_A  
MSIO17NB2/SPI\_1\_SS7/GPIO\_24\_A  
MSIO14NB2/SPI\_1\_SDI/GPIO\_11\_A  
MSIO15PB2/SPI\_1\_SDO/GPIO\_12\_A  
MSIO14PB2/SPI\_1\_CLK

L20 >> SPI\_1\_SS0  
K16 >> SWITCH2 {15}  
K18 >> SWITCH3 {15}  
J18 >> SWITCH4 {15}  
L19 >> DIP1 {15}  
L18 >> DIP2 {15}  
K21 >> DIP3 {15}  
K20 >> DIP4 {15}  
M22 >> SPI\_1\_CLK  
L21 >> SPI\_1\_SDO  
M21 >> SPI\_1\_SDI

Header	Default POS
J37	2-1

SPI\_1\_SS0 1 J37  
MSIO7NB3\_P16 3 2 >> SWITCH1 {15}

3 PIN JUMPER

Place close to FPGA

J38  
HEADER 3

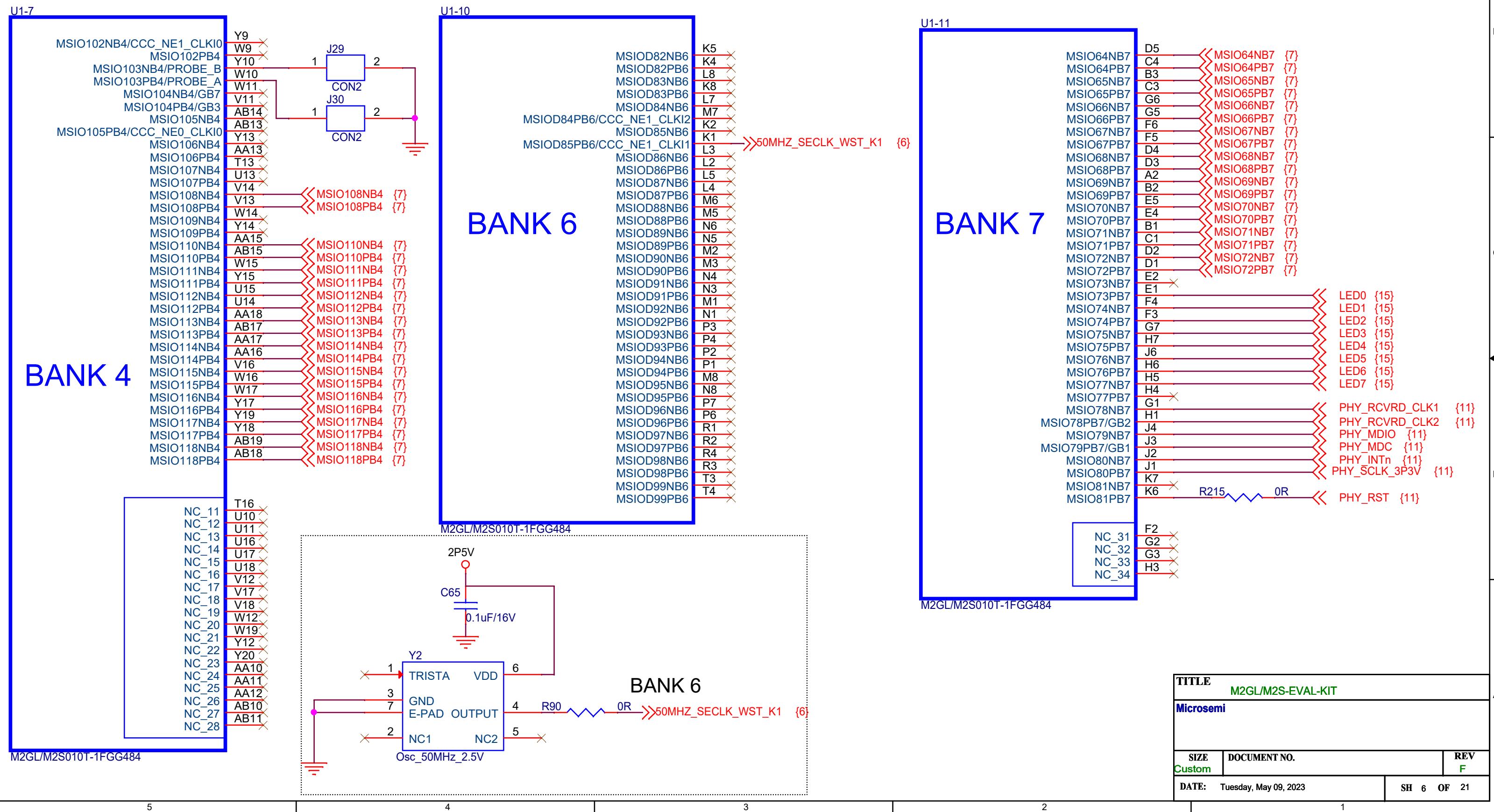
MSIO7PB3\_K17 1 J40  
MSIO7PB3\_R16 3 2 >> USB\_RESET {10}

3 PIN JUMPER

Default Jumper at pin 2 and 3

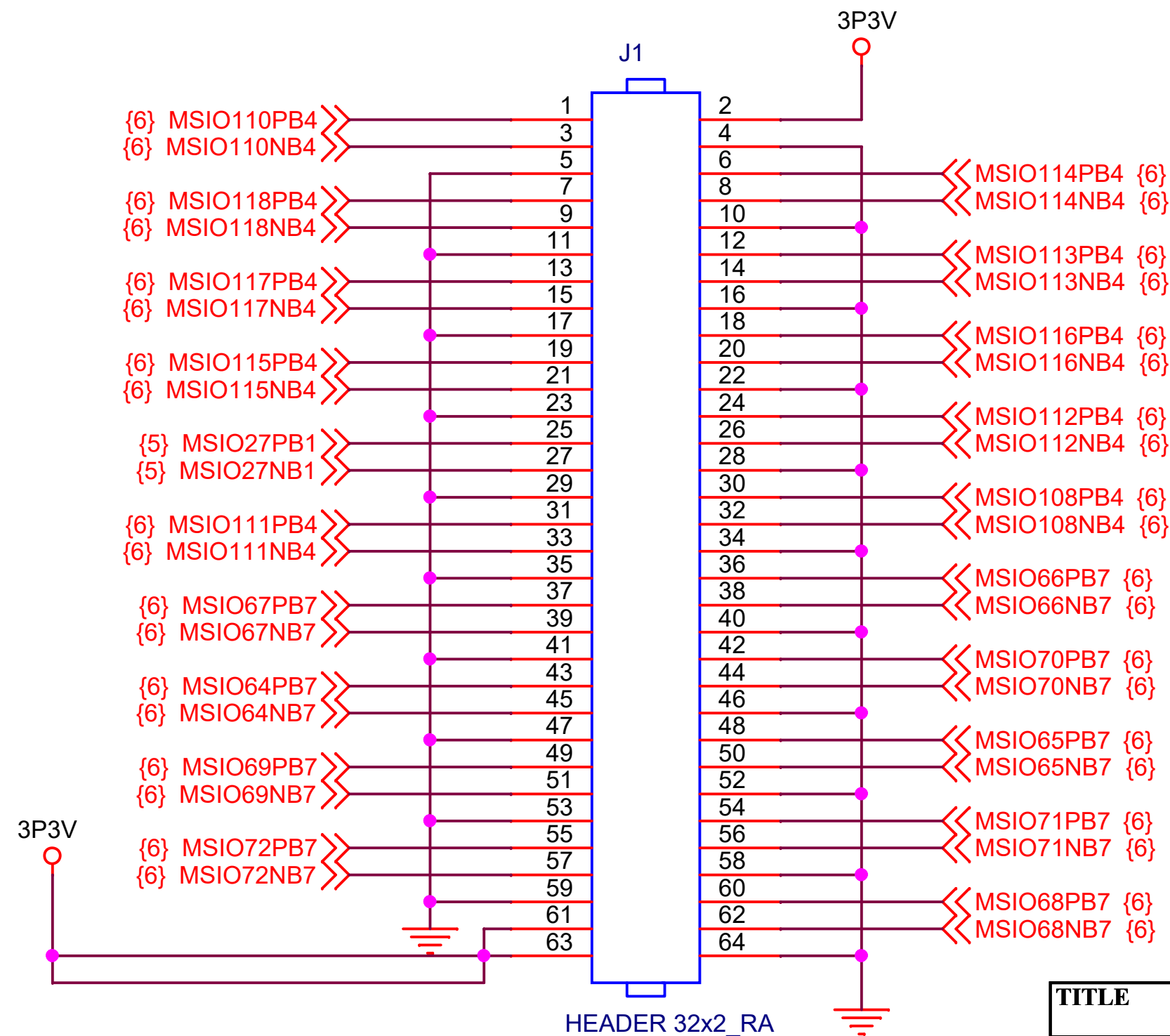
TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		F
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# BANK 4, 6 and 7 CONNECTIONS





# GPIO HEADER

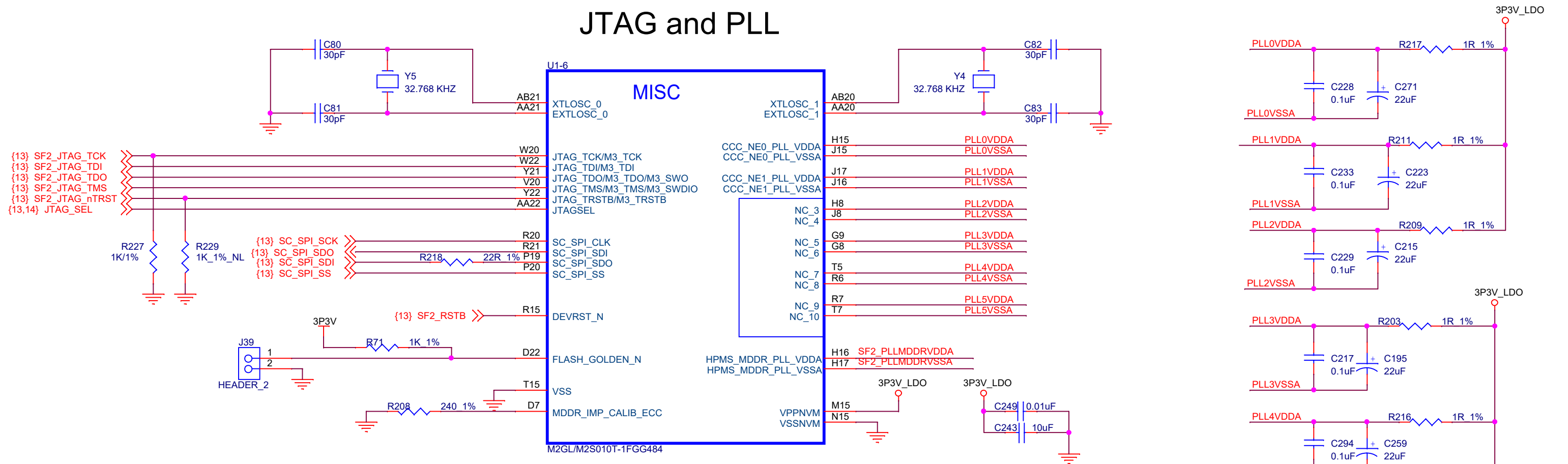


MANUFACTURER P/N = TSW-132-08-T-D-RA  
MANUFACTURER = Samtec

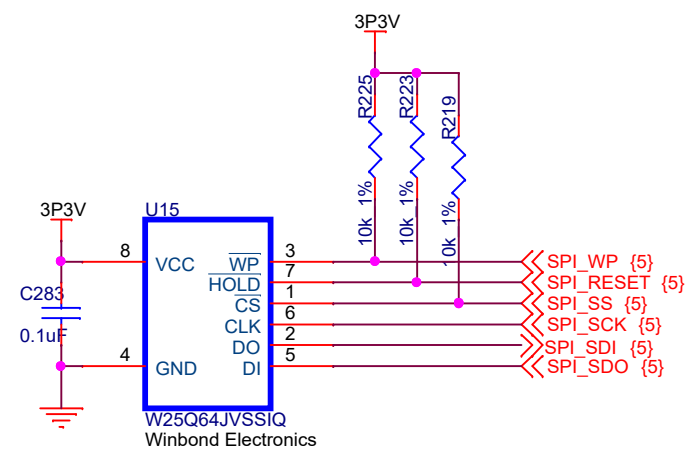
MATING RECEPTACLE P/N: SSW-132-02-S-D-RA  
MANUFACTURER: Samtec

TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
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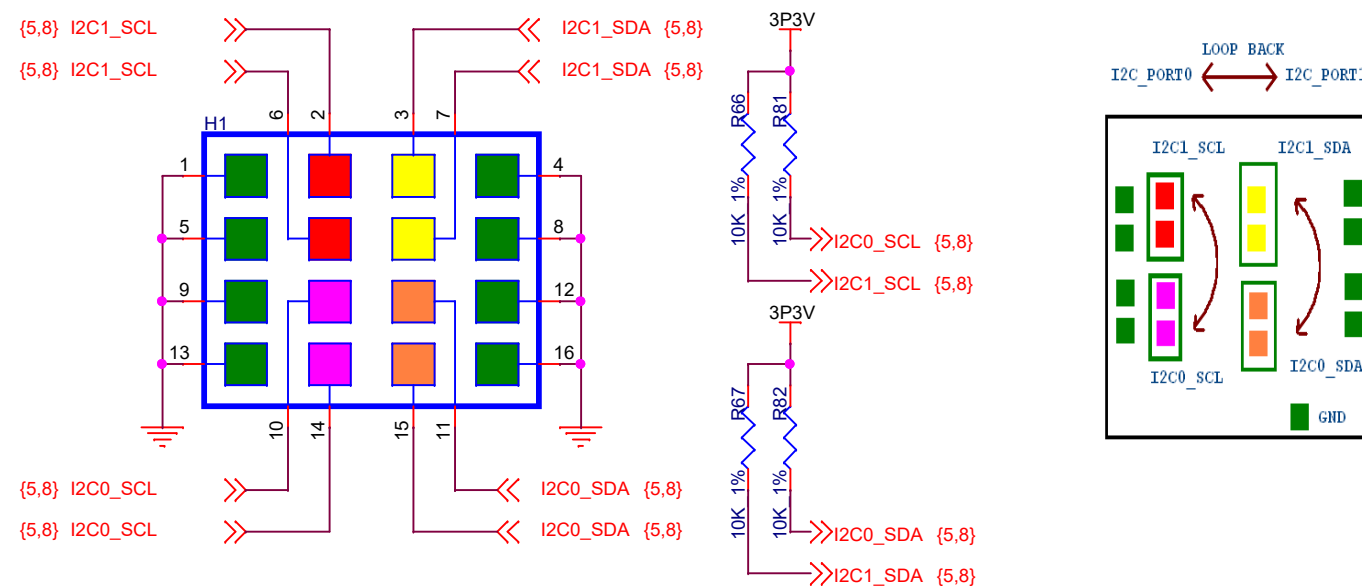
# JTAG and PLL



## SPI FLASH INTERFACE



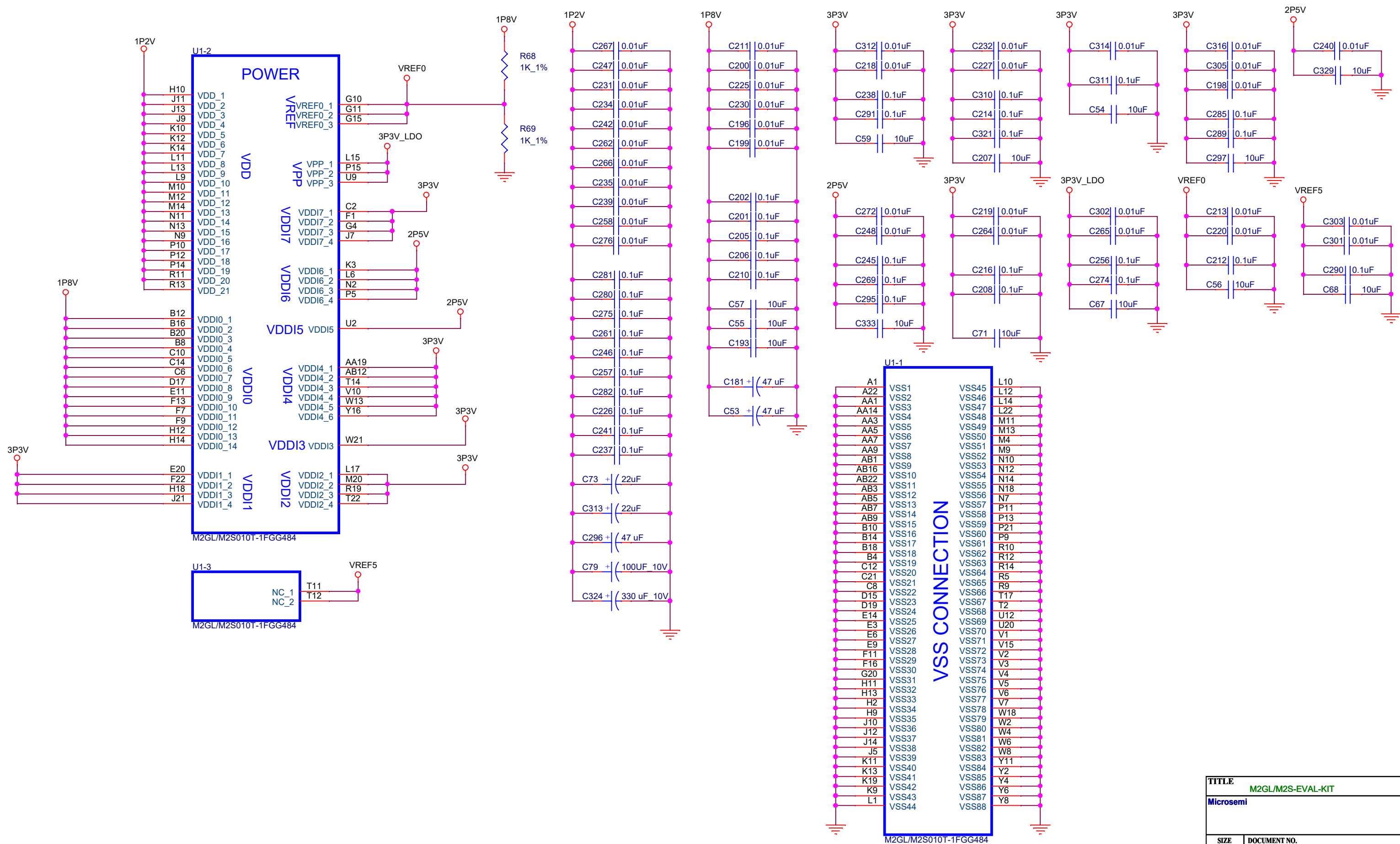
## I2C PORT HEADER



<b>TITLE</b>			
M2GL/M2S-EVAL-KIT			
<b>Microsemi</b>			
<b>SIZE</b>	<b>DOCUMENT NO.</b>		<b>REV</b>
Custom			F
<b>DATE:</b> Tuesday, July 11, 2023		<b>SH</b>	<b>OF</b>
		8	21



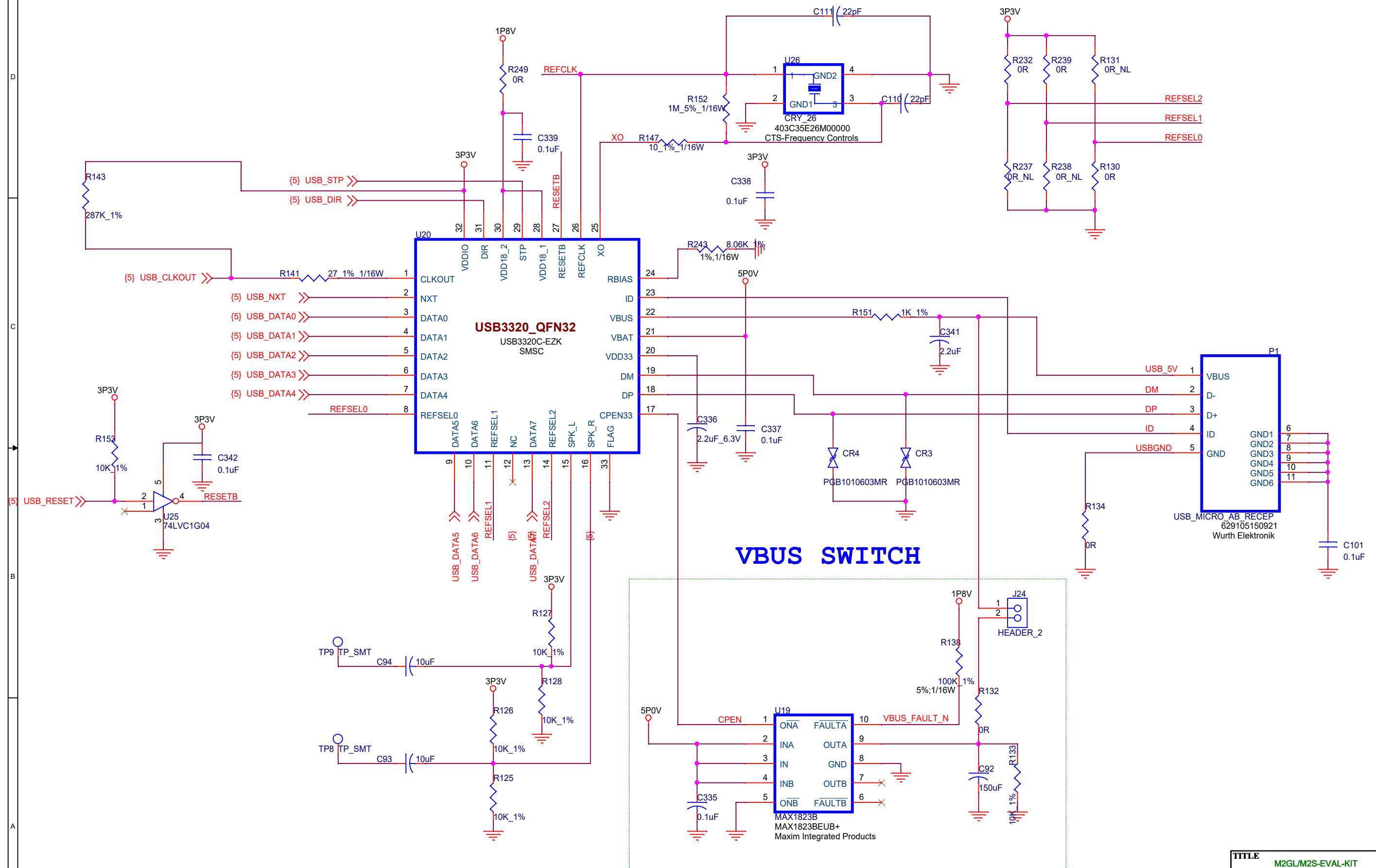
## SF2-POWER, GND AND DECOUPLING CAPACITORS



<b>TITLE</b>			
M2GL/M2S-EVAL-KIT			
<b>Microsemi</b>			
<b>SIZE</b>	<b>DOCUMENT NO.</b>		<b>REV</b>
B			F
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# USB Interface

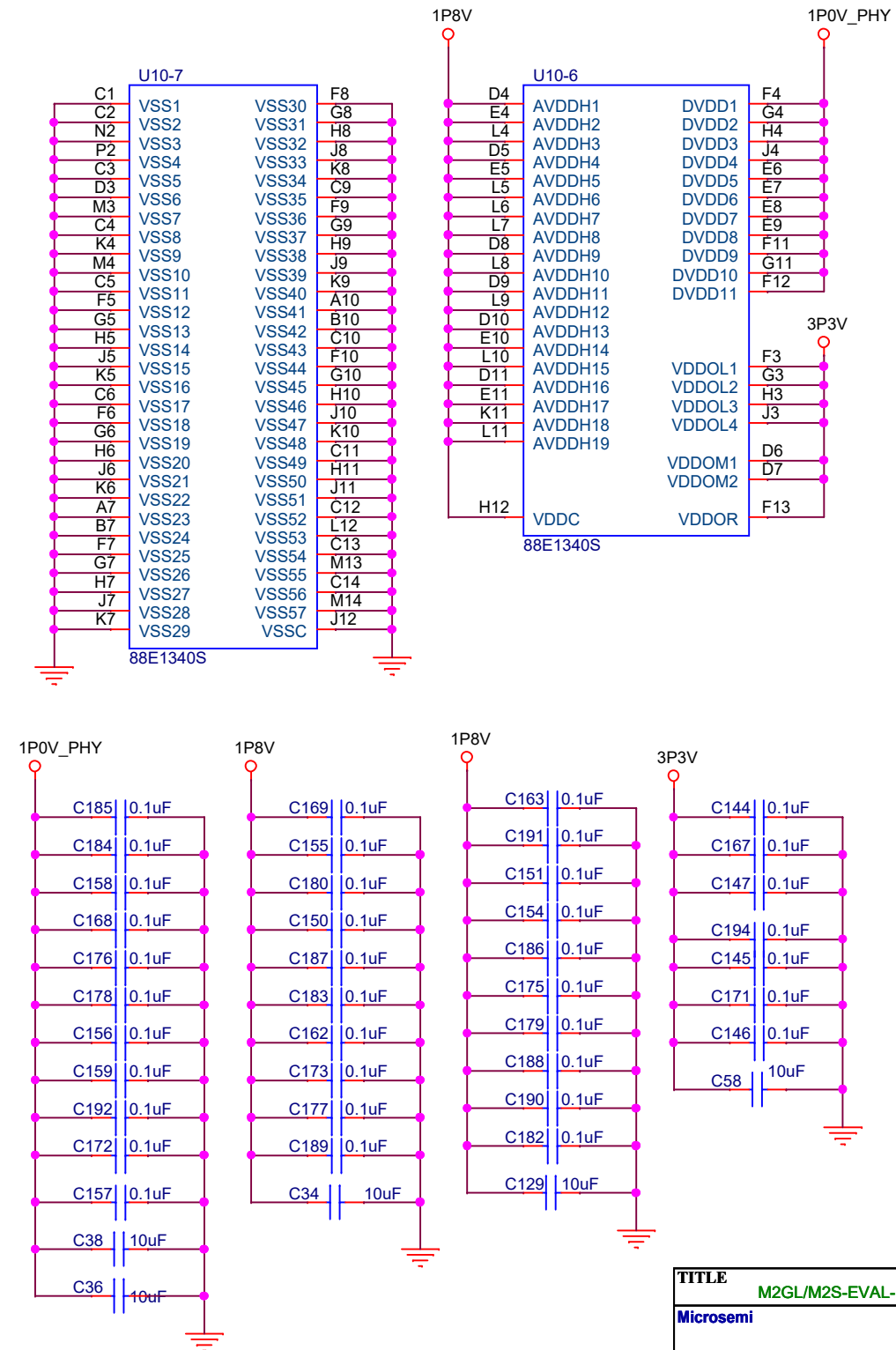
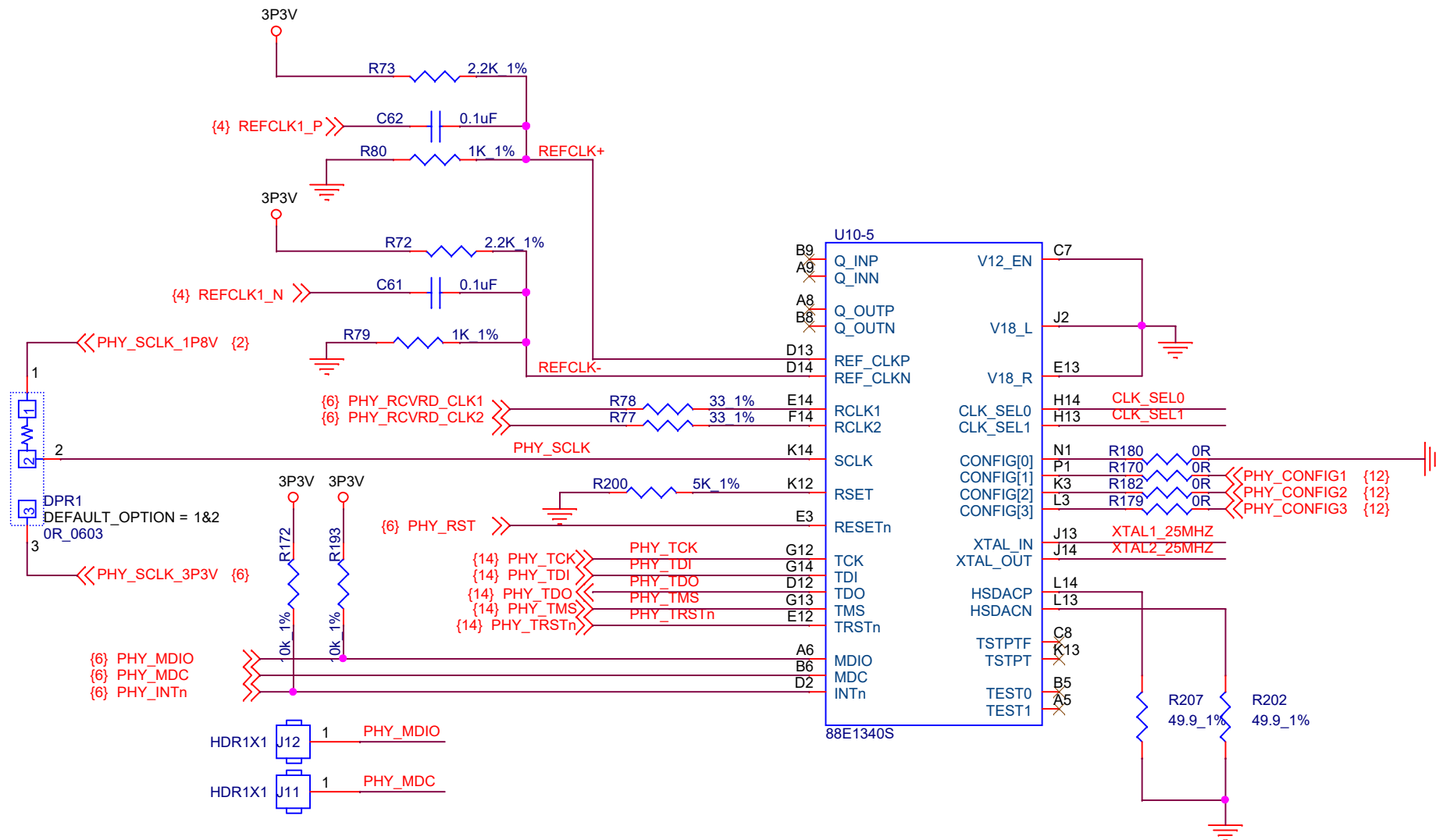
Schematic shows 26.0 MHz Configuration.  
REFCLK[2:0] = 110



TITLE				M2GL/M2S-EVAL-KIT			
Microsemi							
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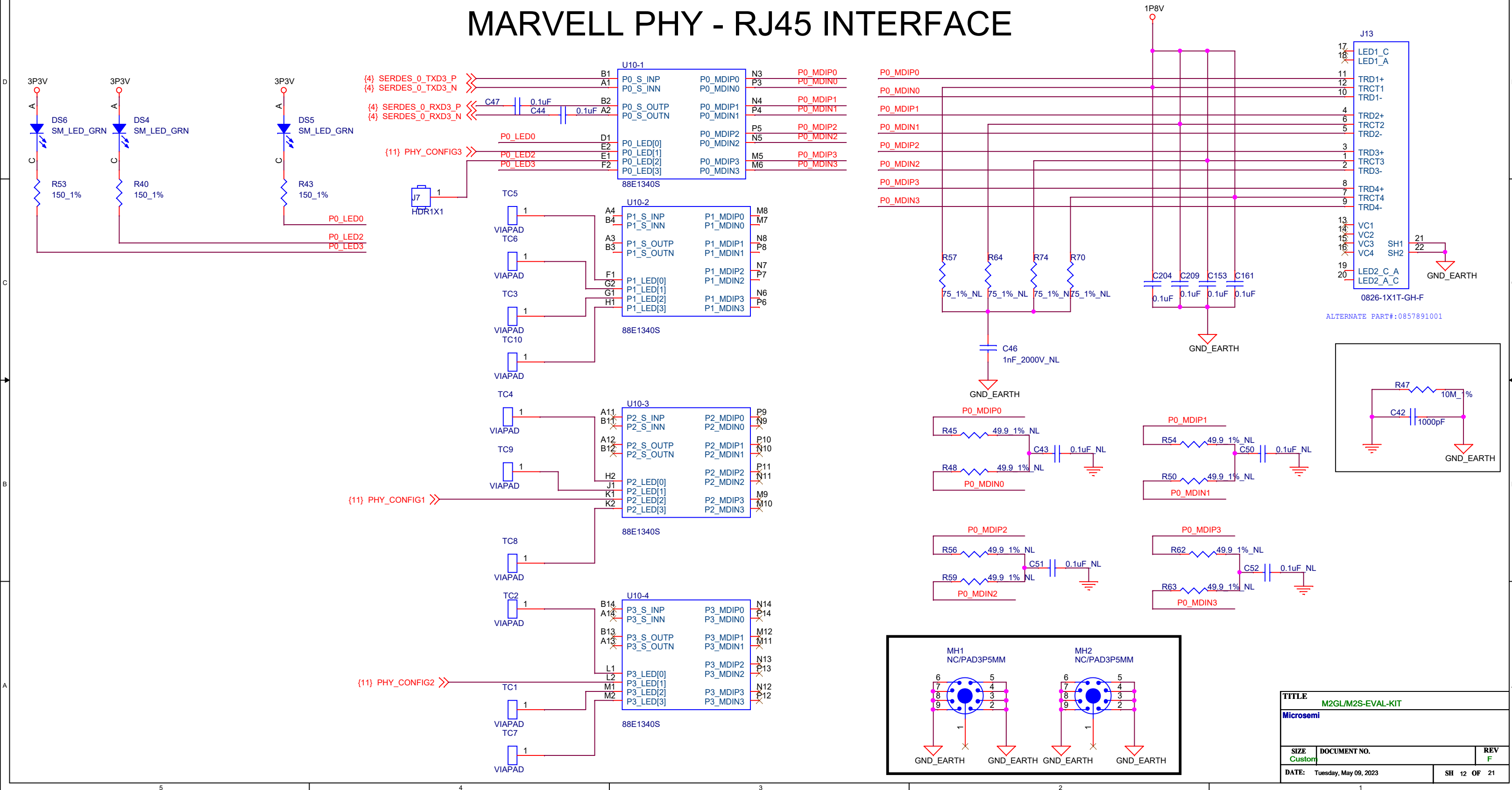
# MARVELL PHY INTERFACE

need to check voltage swing level



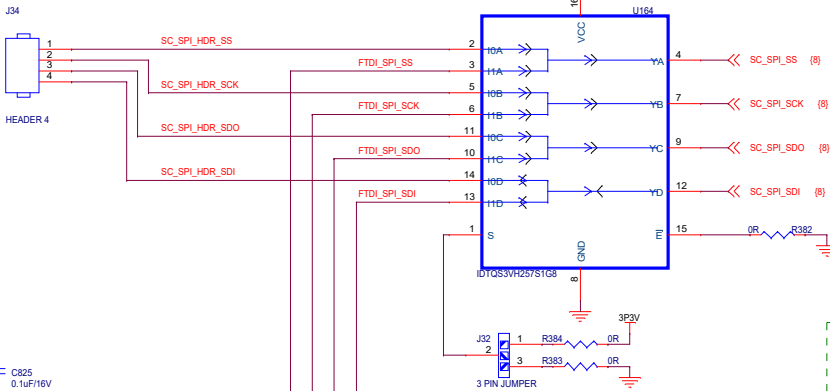
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Microsemi			
<b>SIZE</b> B	<b>DOCUMENT NO.</b>		<b>REV</b> F
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# MARVELL PHY - RJ45 INTERFACE

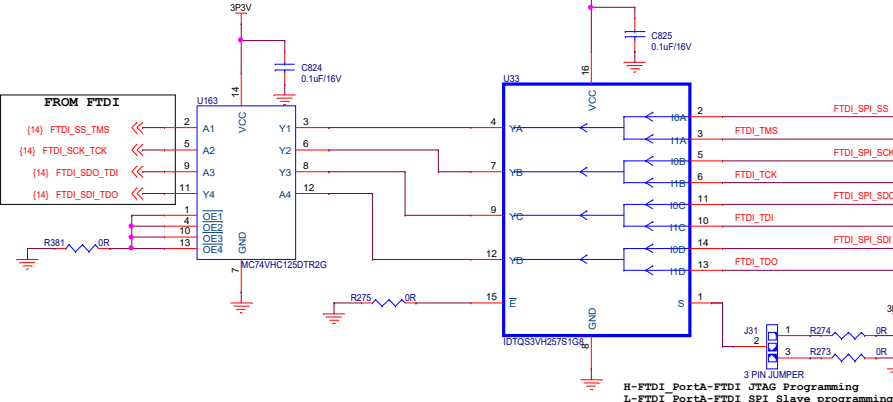


PROGRAMMING CIRCUITRY

SC SPI Header

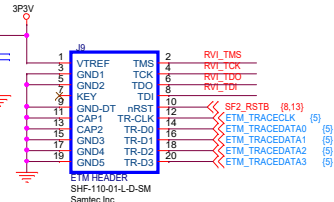


TO FPGA SC\_SPI

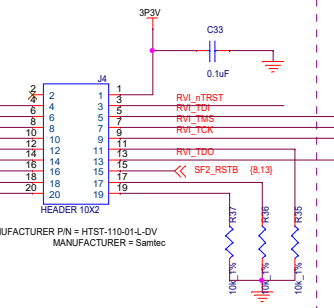


H-FTDI\_PortA-FTDI JTAG Programming  
L-FTDI\_PortA-FTDI SPI slave programming

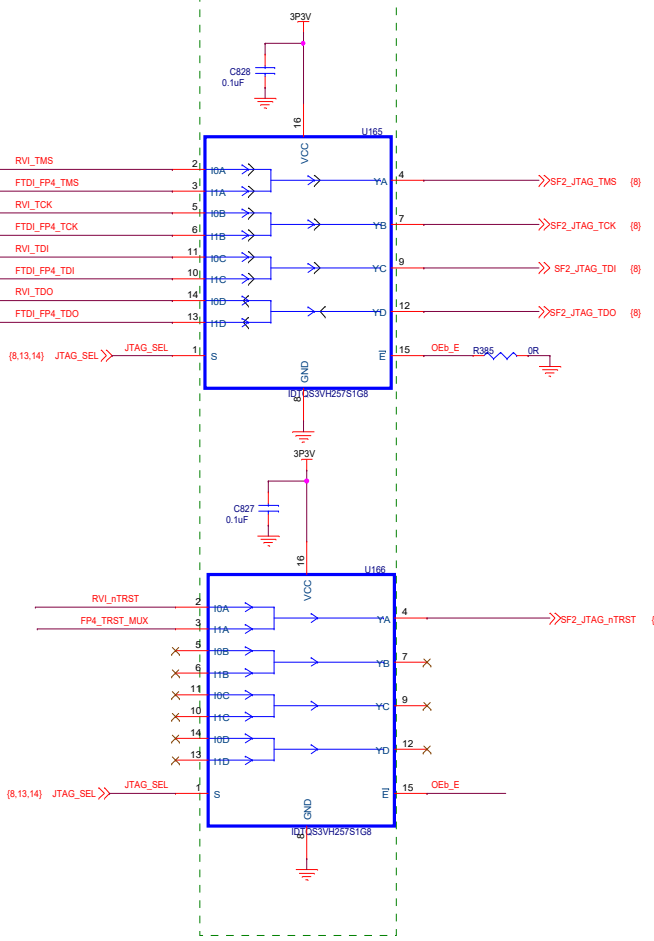
TRACE ETM HEADER



RVI HEADER

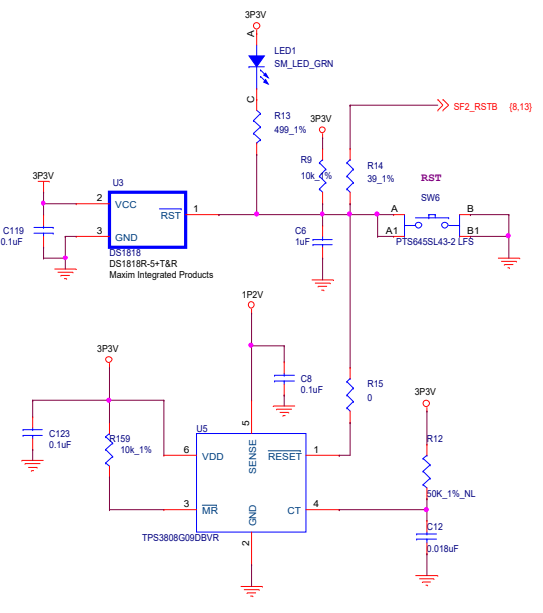


MUX D

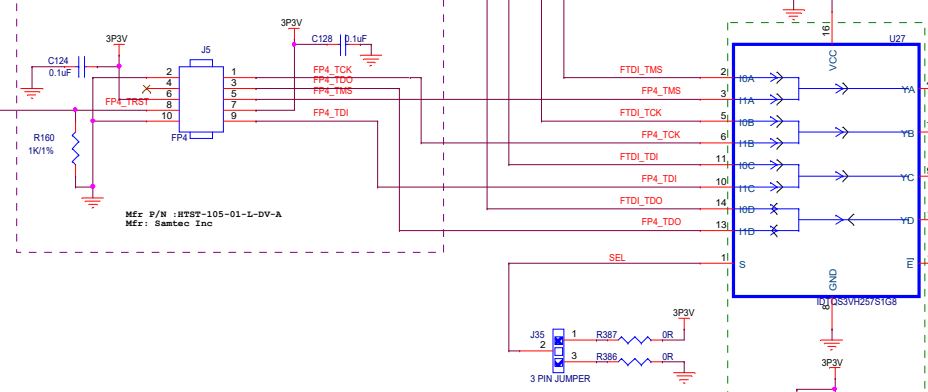


TO FPGA JTAG

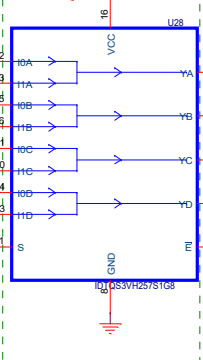
RESET



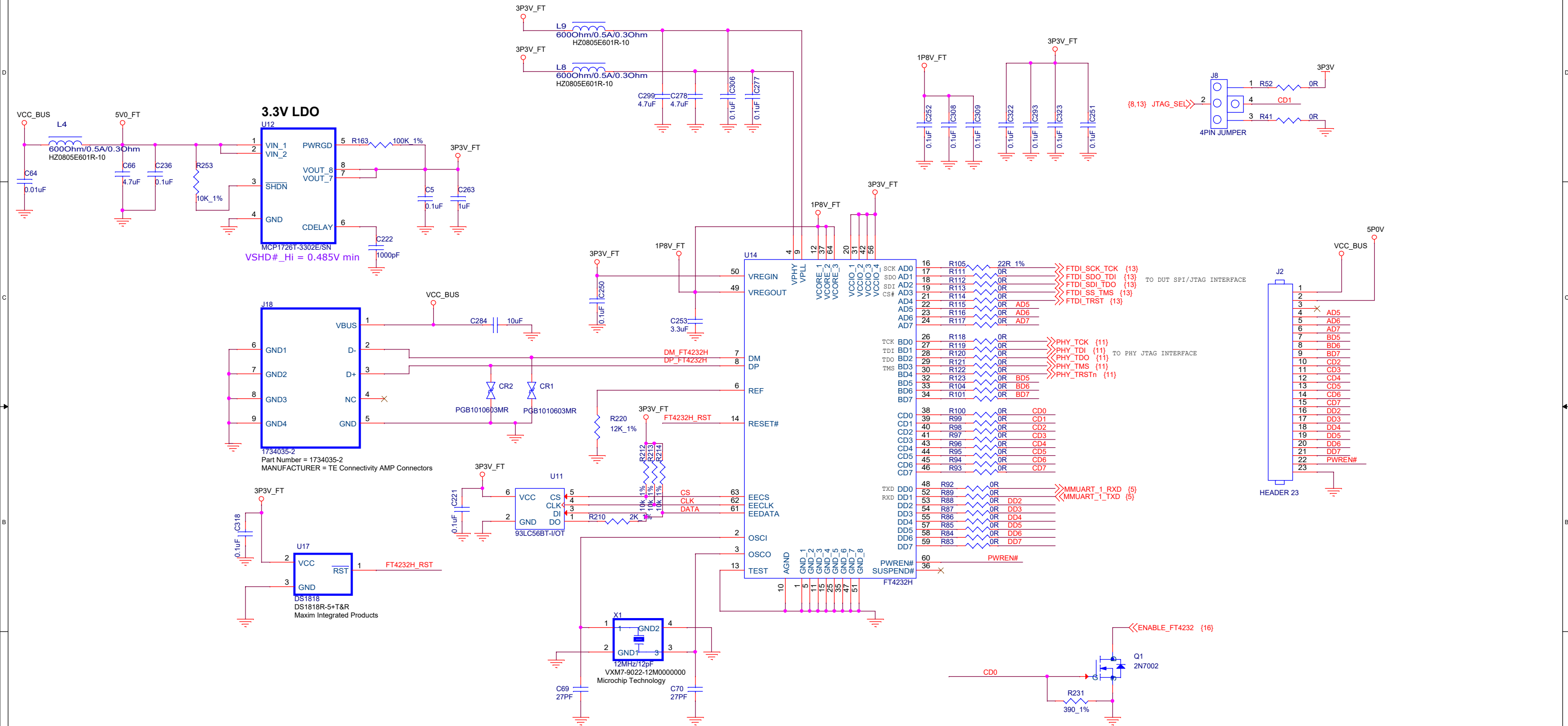
FP4 HEADER



H PATH 1 - Programming Through FP4 HEADER  
L- PATH 0 - Programming Through FTDI JTAG



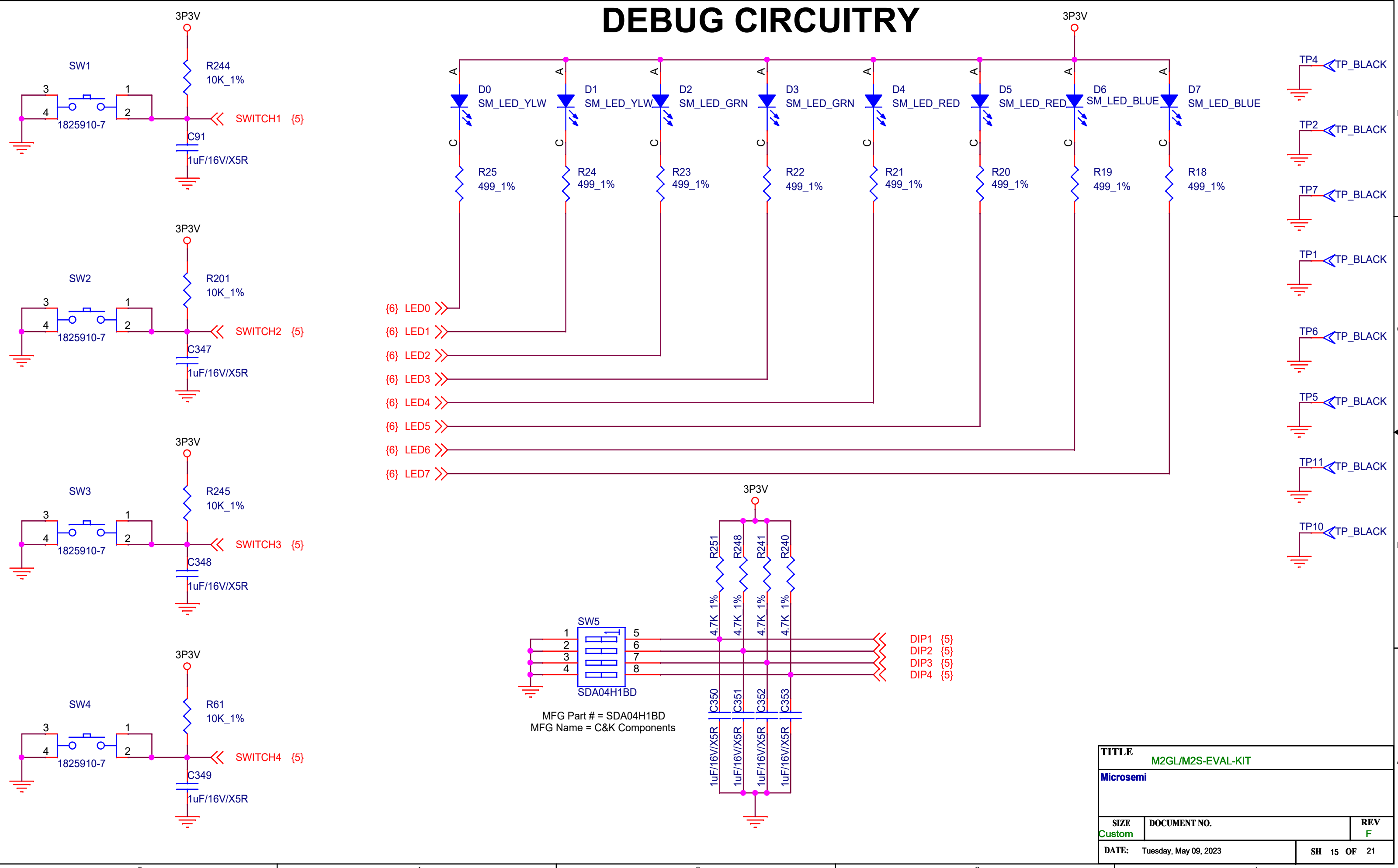
# FT4232H CIRCUITRY



TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
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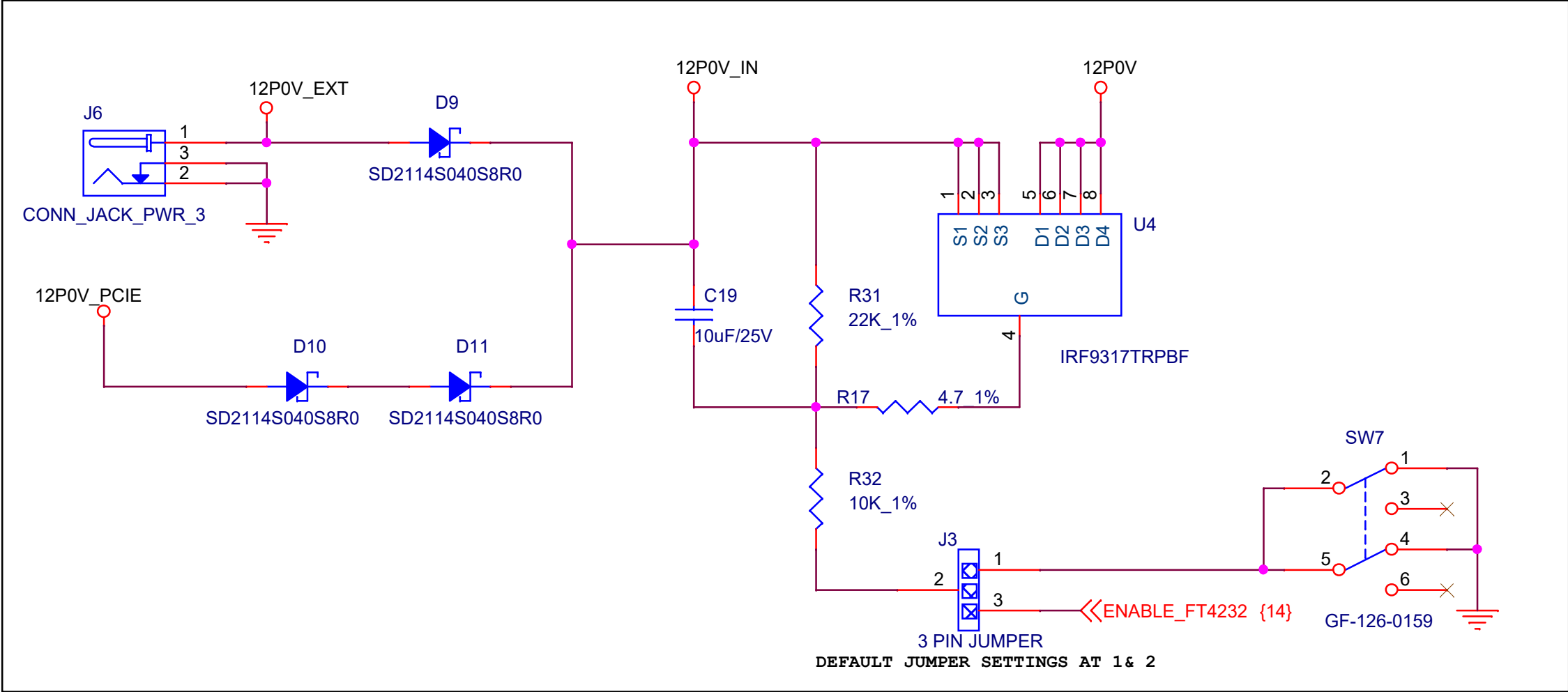


# DEBUG CIRCUITRY



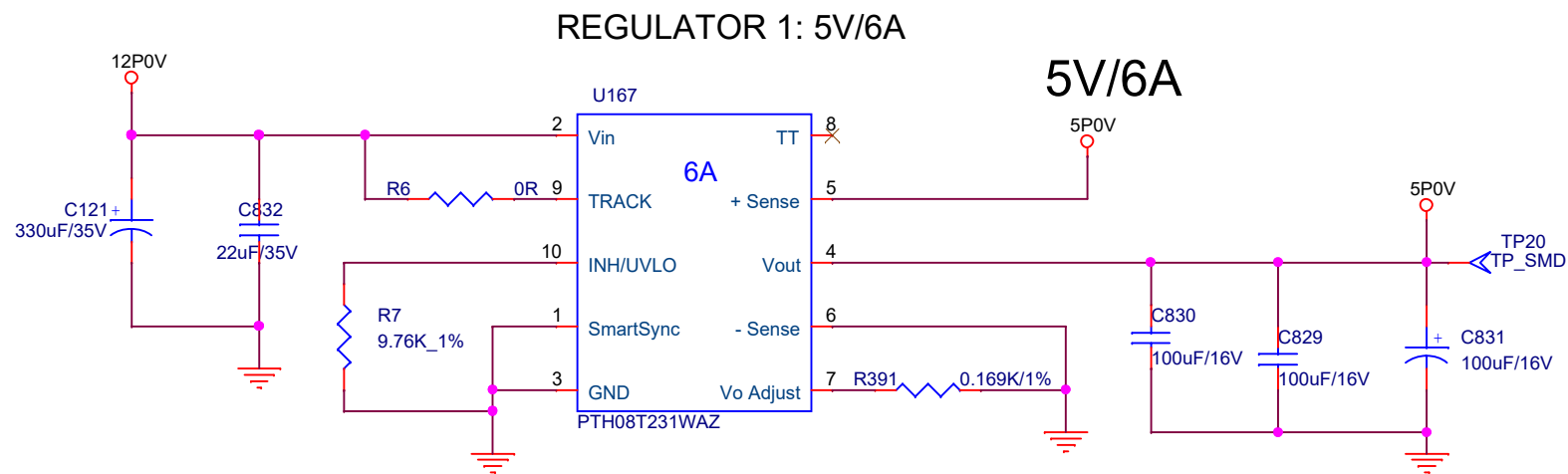
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M2GL/M2S-EVAL-KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		F
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# POWER SUPPLY 1



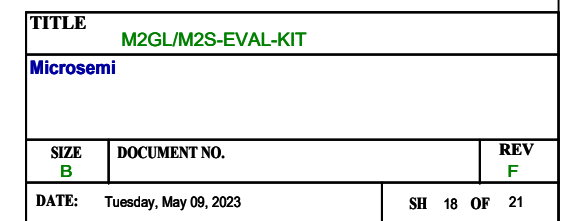
TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		F
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# POWER SUPPLY 2



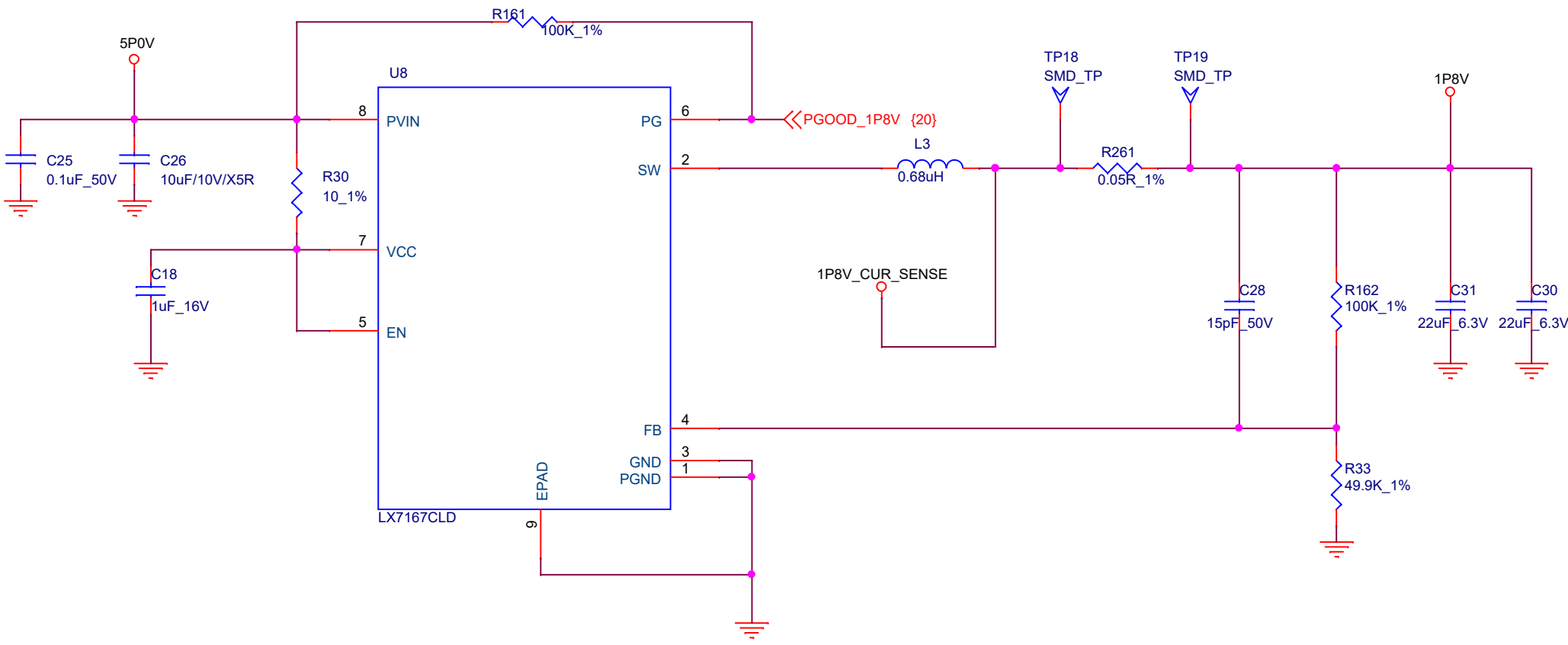
TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
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## 1.2V REGULATOR

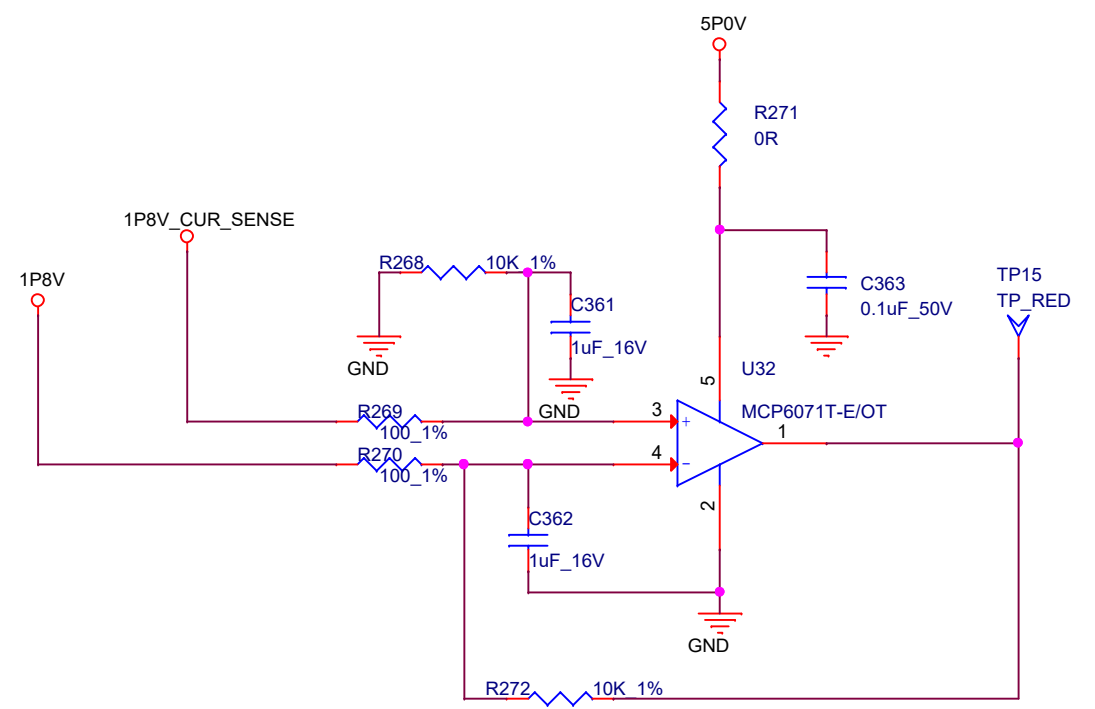


# POWER SUPPLY 4

## 1.8V REGULATOR

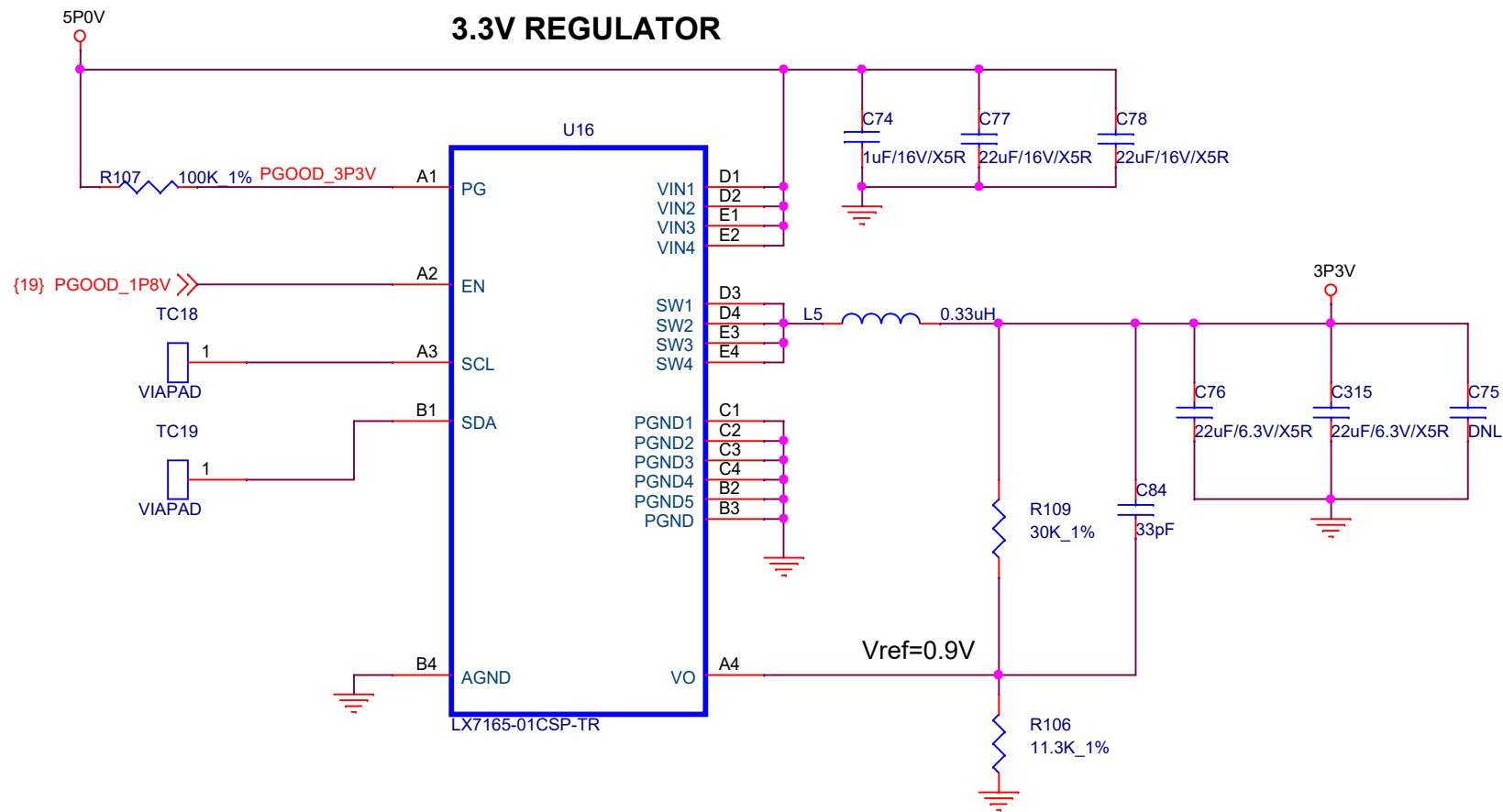
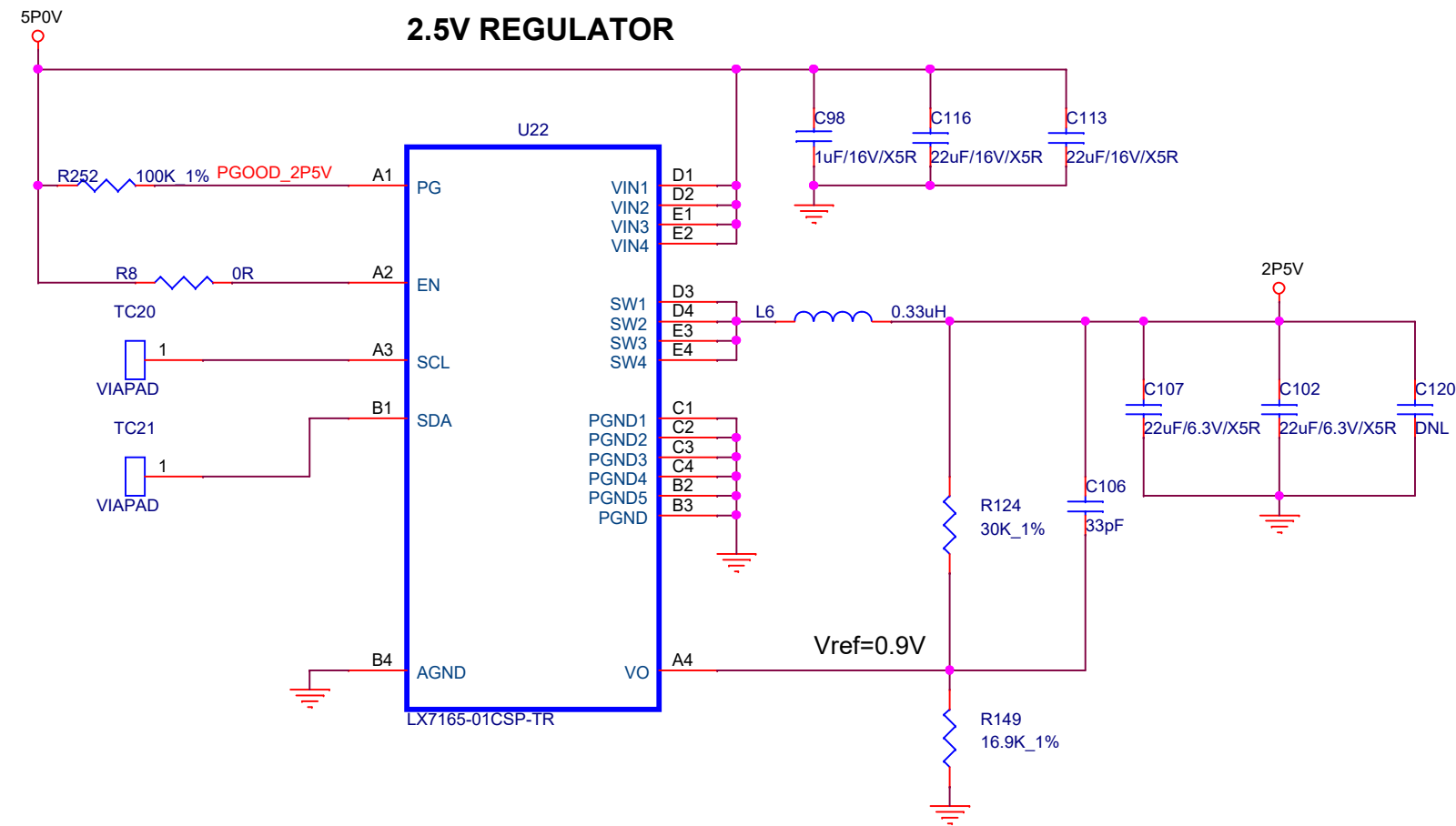


## 1.8V CURRENT SENSING CIRCUIT



TITLE		
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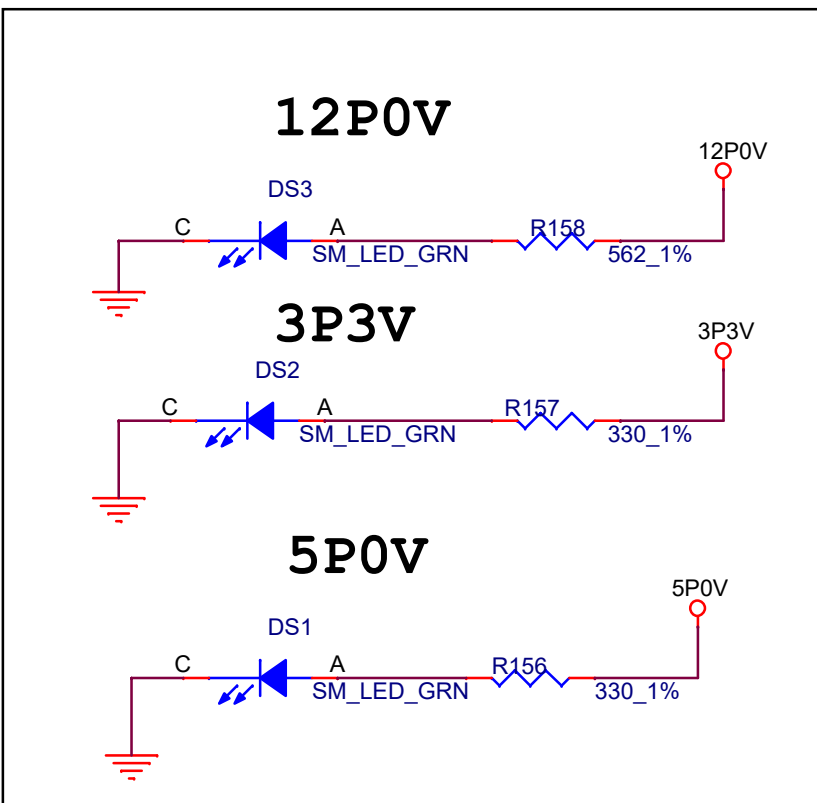
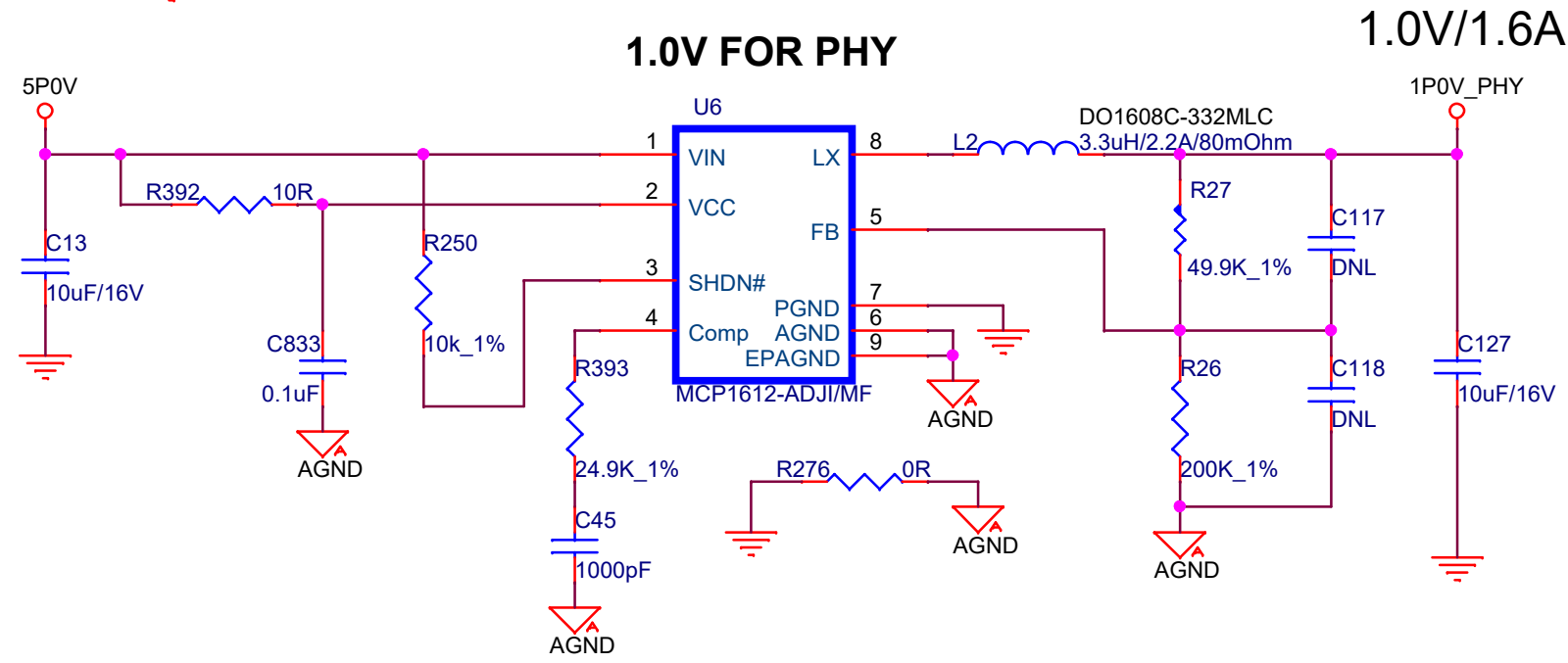
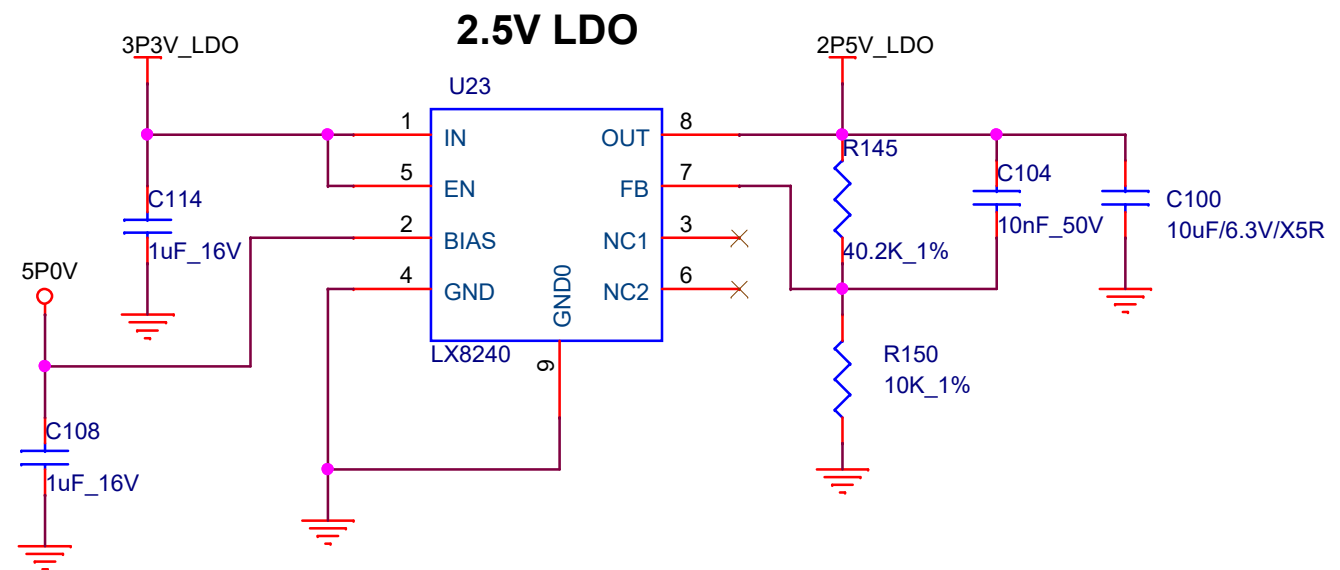
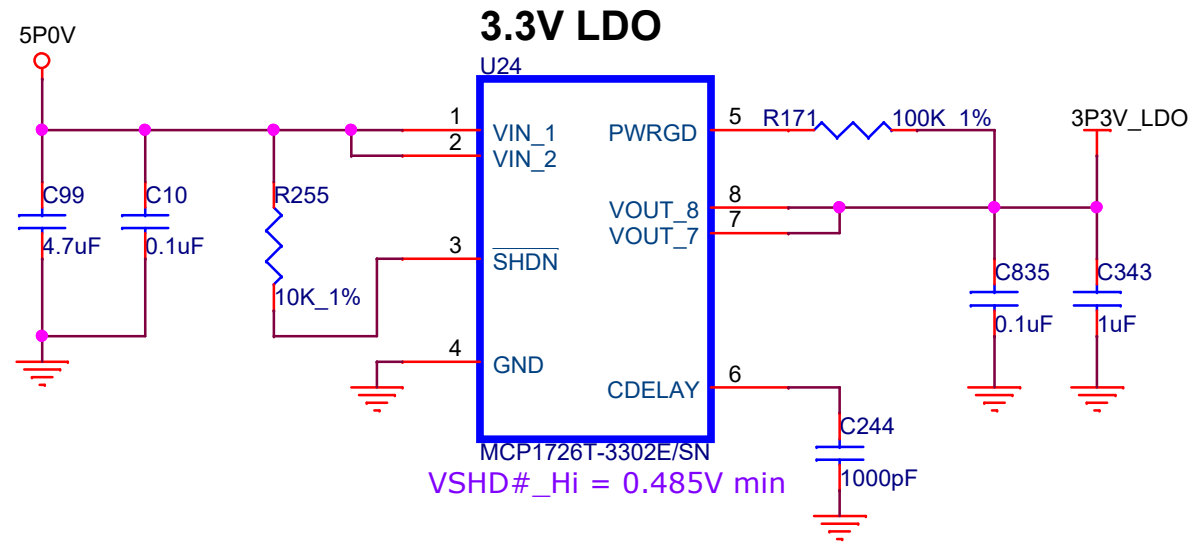
POWER SUPPLY 5



TITLE		
M2GL/M2S-EVAL-KIT		
Microsemi		
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# POWER SUPPLY 6 & LED



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