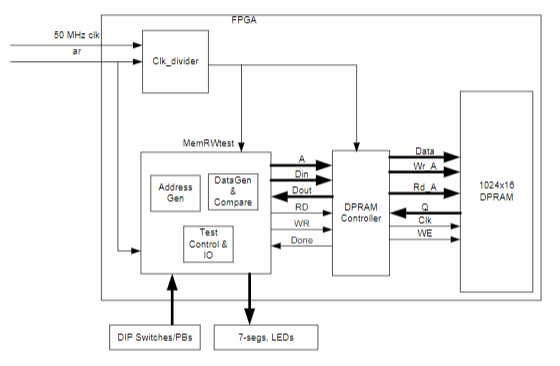
**Project 3 – DE2-115 Internal Memory Controller**

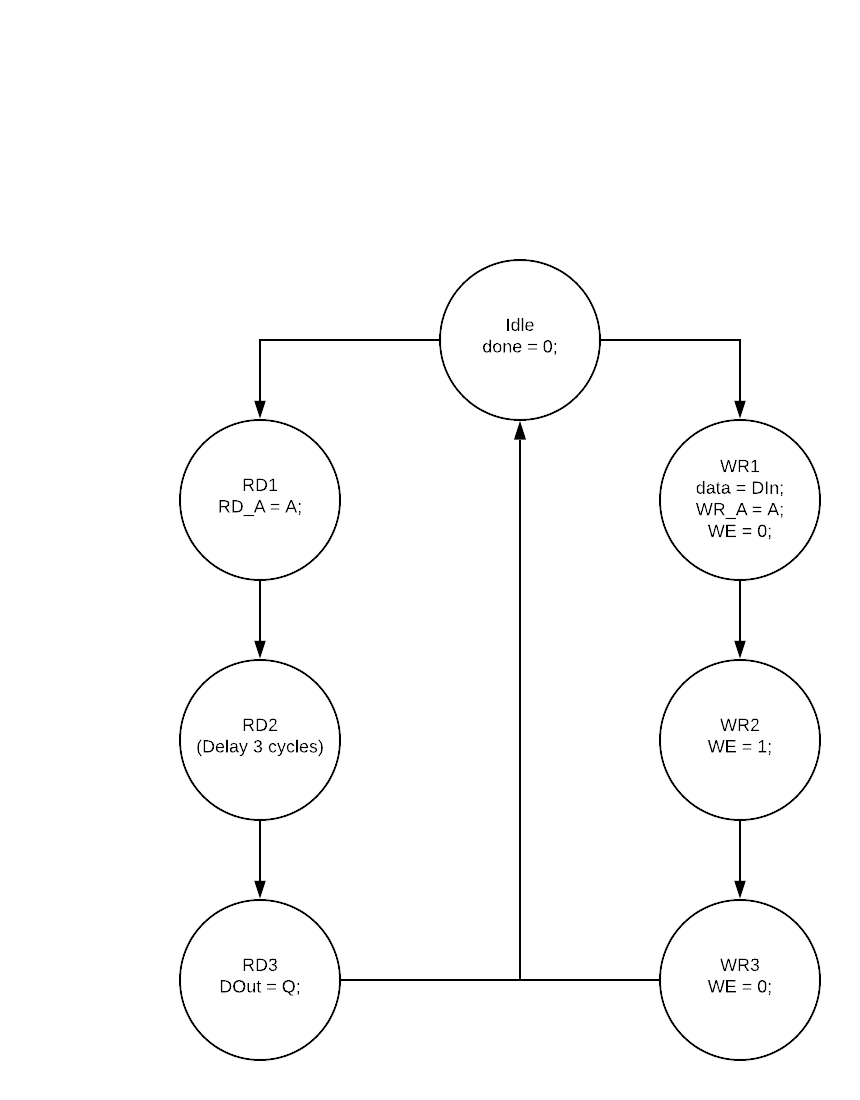
**Scope:**

The goal of this project was to design, implement, and test a memory controller for an internal DPRAM. The project contained 3 modules, the DPRAM, controller, and a test module. The goal of the test module was to perform an internal test and also offer the user I/O to load and read data from any of the memory locations.

**Design Strategy:**

The Project was built to the specifications in the diagram below excluding the clock divider which was not needed.

The DPRAM module was created in Quartus through the IP setup wizard. The controller was implemented following the state machine design we went over in class. State diagram shown below. The MemRWtest module implemented two similar state machines, one for the internal test, and one for the I/O read and write. The active state machine is controlled by a switch on the board. When in the internal test mode, the button on the far left is pushed to start the test, at the end of the test the green LED will light up if the test passes or the red LED will light up if the test fails. In use I/O mode the buttons from left to right are address, read, write, and reset. The address button will take in the 10 rightmost switches as the address and the write uses the 16 rightmost to take in the data to be written.

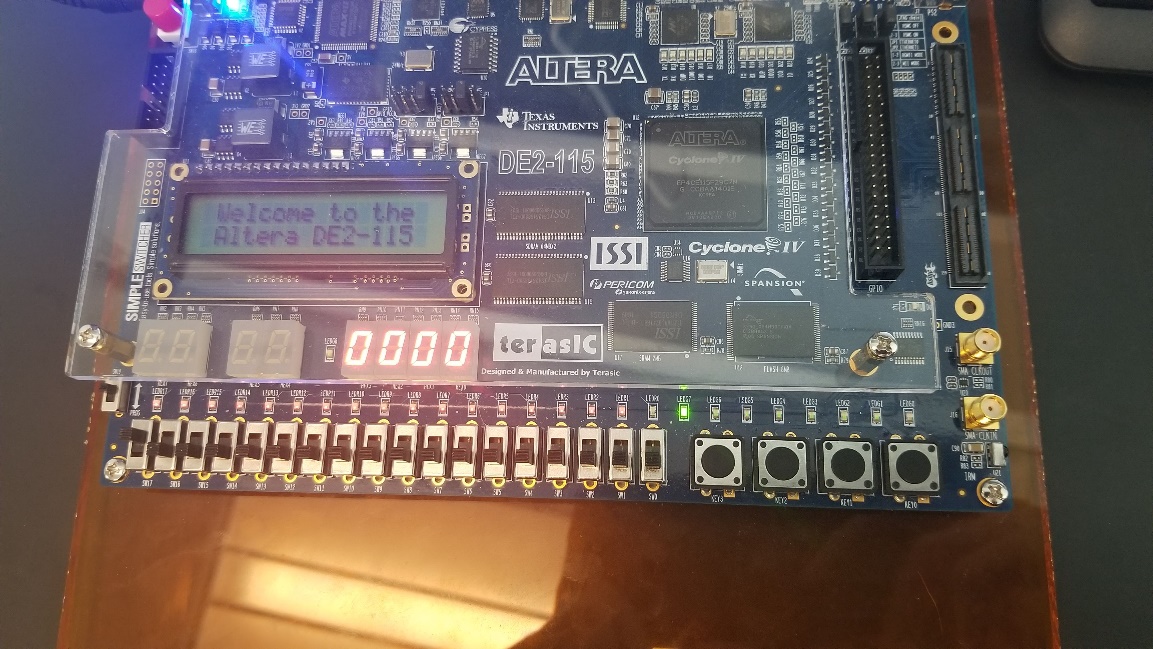


**Results:**

The following link contains video showing the I/O working as expected. The hex value F is stored in memory location 1 and the hex value E is store in location 2.

<https://photos.app.goo.gl/BiKGWyWHXTih5EFc8>

The picture below shows the board in internal test mode with the green LED on showing it has passed the test.



From Quartus the Fmax is 99.39 MHz and the board uses 232 logic elements which is <1%. The DPRAM module is clearly seen as implemented with Quartus showing 16,384 bits which is equivalent to 1024 X 16.

**What I Learned:**

**Conclusions:**

**Appendix:**