PIC32CX-BZ2

PIC32CX-BZ2 Hardware Design Guidelines User's Guide

Introduction

This user guide describes the hardware design guidelines for integrating the PIC32CX1012BZ25048 System-on-Chip (SoC) in a custom design.

This document describes the following recommended guidelines to achieve the optimized RF performance and to reduce the time to market:

- Reference design and certain key aspects to be considered in the design for achieving optimized performance using the PIC32CX1012BZ25048 device
- Comprehensive design checklist that can be used for self-review of the PIC32CX1012BZ25048-based design
- Schematic and layout considerations for different sections of a reference design based on the PIC32CX1012BZ25048 device

Note: The snippets of schematics and layouts are provided from the reference design, unless otherwise specified. Schematic and layout snippets from the WBZ451 Curiosity Board were added for reference in the description of the corresponding figure.

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1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth® Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Data Sheet* (DS70005504)
- *PIC32CX-BZ2 Family Silicon Errata Sheet* (DS80001043)
- *WBZ451 Curiosity Board User's Guide* (DS50003367)

1.2 Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms and Abbreviations	Description
CLDO	Core Low-Dropout
GND	Ground
LDO	Low-Dropout
LPA	Linear Power Amplifier
LPF	Low-Pass Filter
MLDO	Main Low-Dropout
MPA	Medium Power Amplifier
PCB	Printed Circuit Board
RX	Receiver
SoC	System-on-Chip
SOSC	Secondary Oscillator
SWD	Serial Wire Debug
SWO	Serial Wire Output
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
VDD	Voltage Drain Drain

2. Schematic Guidelines

2.1 Power Supply

The VDD_M power rail is the main power supply voltage rail connected to Pin 39 (VDD33), Pin 2 (PMU_VDDIO/ VPMU_VDDC) and Pin 48 (VPMU_VDDP). AVDD power rail is an analog power supply voltage rail connected to Pin 36 (AVDD).

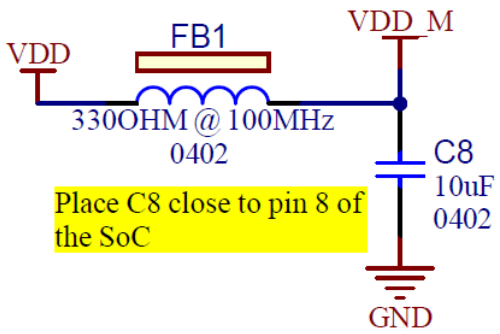
Notes:

1. The same voltage level must be applied to VDD_M and VDD_A.
2. Matching the ramp rate to the ramp requirement of the device is recommended.

2.1.1 VDD_M Input Filter

The following figure illustrates the schematic snippet, highlighting the filtering requirement for VDD_M from the main power supply rail, VDD.

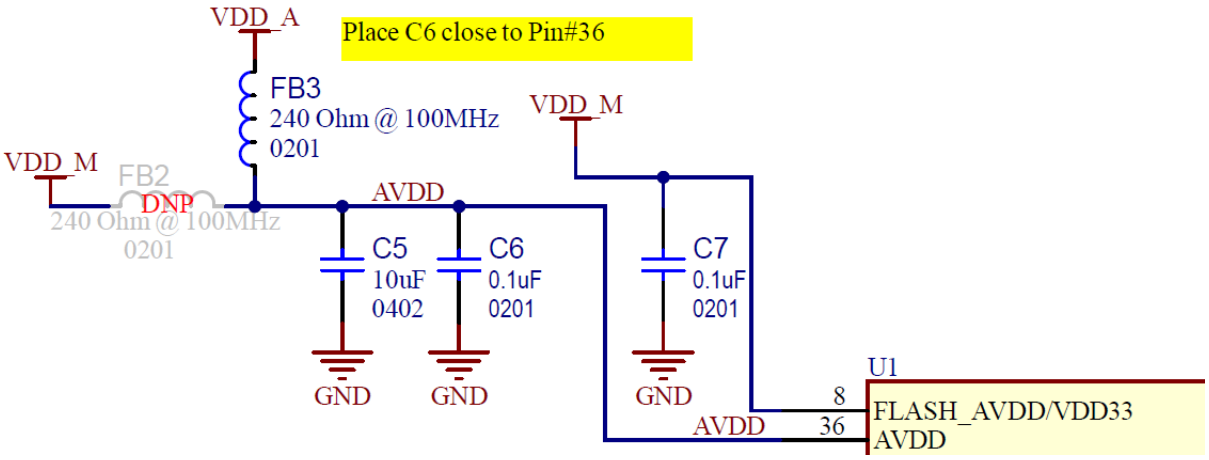
Figure 2-1. Filtering for Power Supply



2.1.2 AVDD Input Filter

The following figure illustrates the schematic snippet, highlighting the filtering requirement for AVDD. It can be either connected to the main power supply rail VDD_M or to a separate analog power supply VDD_A. By default, the FB3 ferried bead is shown mounted on the reference design, assuming that a separate analog supply will be fed to the device. If a separate analog supply is not available on a specific custom design case, then connect AVDD to a main power supply rail VDD_M through the FB2 ferrite bead.

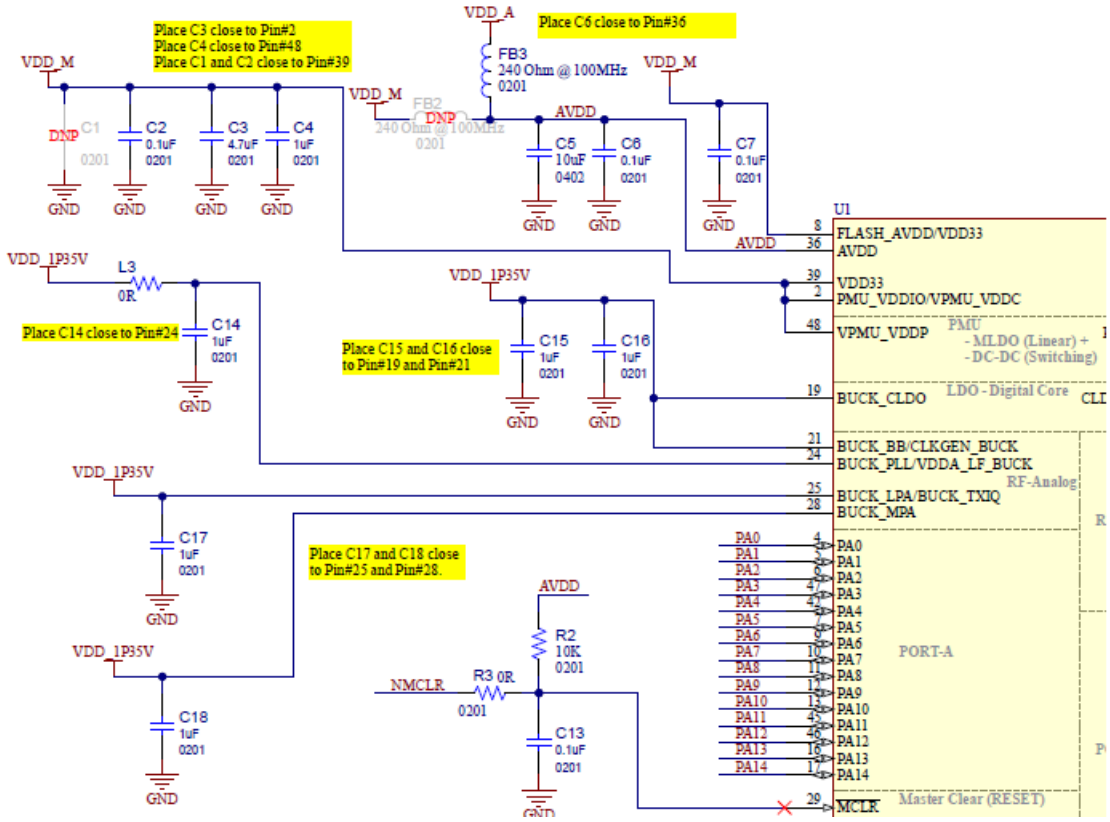
Figure 2-2. AVDD Input Filter



2.1.3 Input Decoupling Capacitor

The following figure focuses on the decoupling requirements for the power supply pins of the PIC32CX1012BZ25048 device. Place all the decaps closer to the power pins.

Figure 2-3. Input Decoupling Capacitor



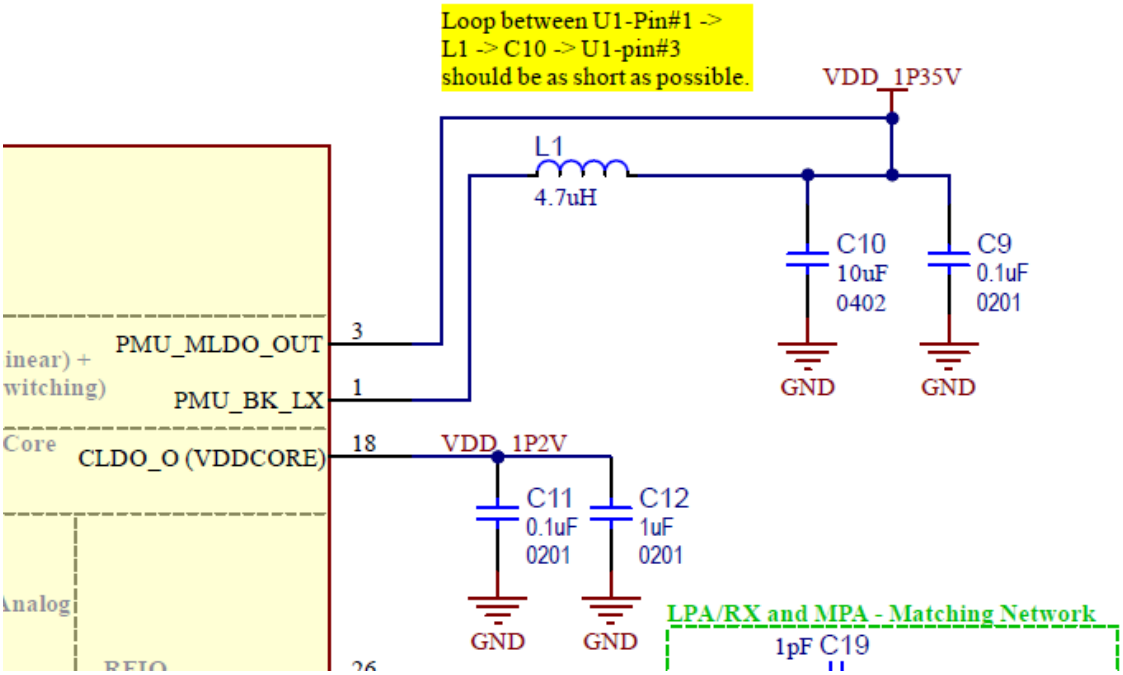
2.1.4 Power Management Unit (PMU)

The PIC32CX1012BZ25048 device's PMU section has both a DC-DC converter and a Main Low-Dropout (MLDO). The following figure shows the external components required for the internal buck regulator (DC-DC section). Using

the same value of switching inductor (L1) and switching capacitor (C10) is recommended to get the same buck output performance.

The output of the DC-DC converter (buck) and MLDO is typically 1.35V and it is named “VDD_1P35V” power rail. The VDD_1P35V power rail is used to power the pins BUCK_CLDO (Pin 19), BUCK_BB (Pin 21), BUCK_PLL (Pin 24), BUCK_LPA (Pin 25) and BUCK_MPA (Pin 28).

Figure 2-4. Decoupling for DC-DC Section and VDDCORE



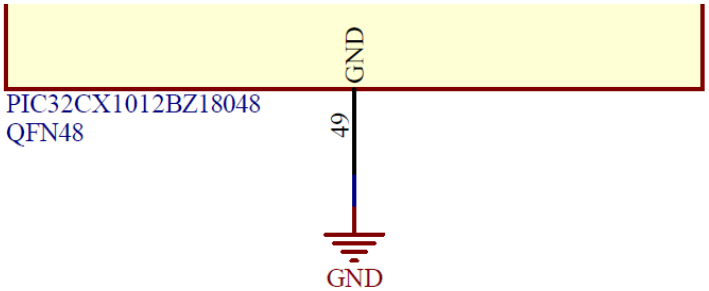
2.1.5 Core LDO (CLDO)

The device has an internal core LDO, and its output is connected to pin 18 (CLDO_O) to add an external decoupling capacitor. The output of the core LDO regulator is 1.2V, and it is named “VDD_1P2V”. Do not use this VDD_1P2V to power any other external circuitry. C11, referred to in Figure 2-4, must be placed closer to the pin followed by C12 in the Printed Circuit Board (PCB) layout.

2.1.6 Ground Paddle (GND)

The GND paddle of the PIC32CX1012BZ25048 device must be connected to the board GND.

Figure 2-5. GND Paddle Schematic Connection



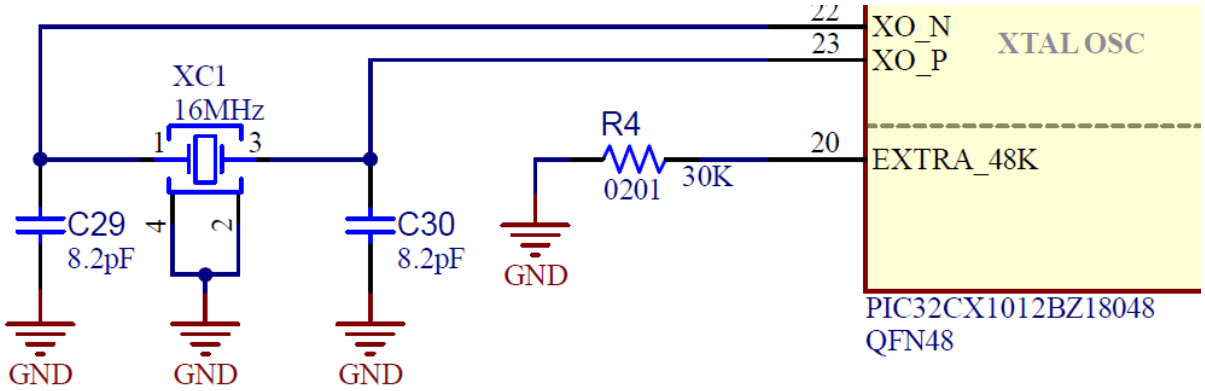
2.2 External Clock Sources (Crystal)

This section details the schematic connection for the external clock sources of the PIC32CX1012BZ25048 device.

2.2.1 16 MHz Crystal

The 16 MHz crystal is the most critical part as this is the clock source for the RF section.

Figure 2-6. 16 MHz Crystal Schematic Connection

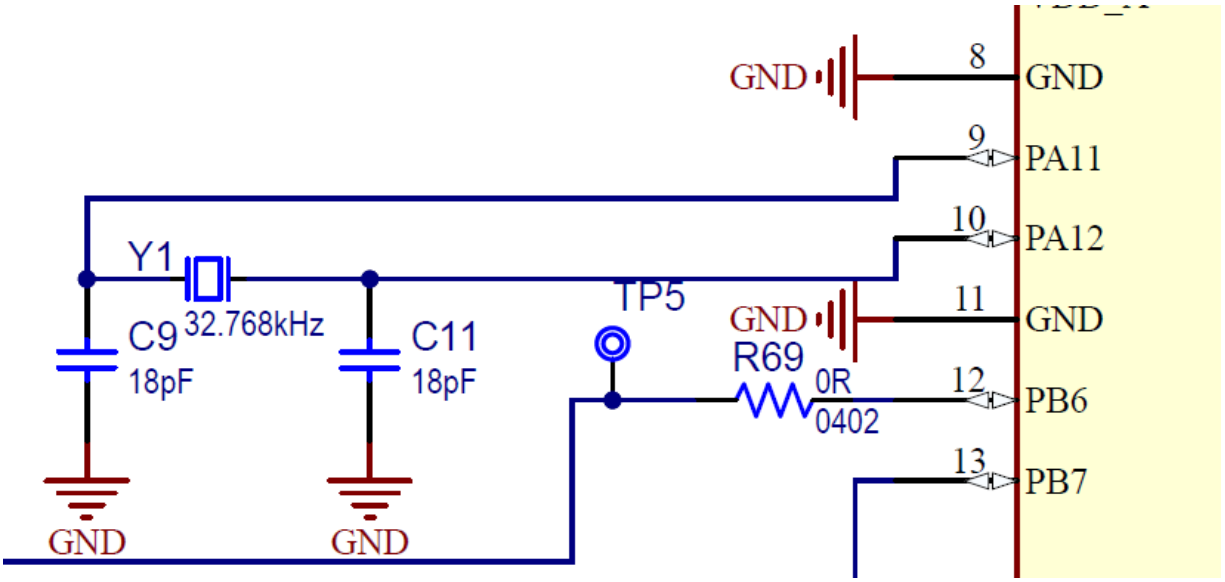


Note: The crystal load caps help to coarse tune the RF center frequency. The “Frequency Offset Calibration” process helps to further fine tune the center frequency to keep it within the required tolerance and, ideally, closer to 0.

2.2.2 Secondary Oscillator (SOSC) (32.768KHz) Crystal

The SOSC crystal circuit is not part of the reference design. For more details, refer to the *WBZ451 Curiosity Board User's Guide* design files. PA11 (Pin 45) and PA12 (Pin 46) on the PIC32CX1012BZ25048 device are SOSC pins.

Figure 2-7. SOSC (32.768 kHz) Crystal Schematic Connection



Note: For tuning the SOSC crystal frequency, the SOSC clock can be enabled and output on an I/O pin. For more details, refer to the *High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Data Sheet*.

2.3 RF Front-end

The following schematic snapshots show the reference schematic design for the RF front-end with the Linear Power Amplifier (LPA) and Medium Power Amplifier (MPA) path shorted after the matching capacitors (C19 and C27). This is followed by a discrete Low-pass Filter (LPF) section, designed for filtering the harmonic frequencies. The RF test point (TP3) is recommended to add in the design for verifying the performance of the device in both the prototype and production stage.

Two separate reference designs are provided, one with a PCB antenna variant and another with a U.FL connector for connecting an external antenna. Each variant has its own network impedance-matching components.

Figure 2-8. PCB Antenna Reference Design – RF Front-end Schematic Connection

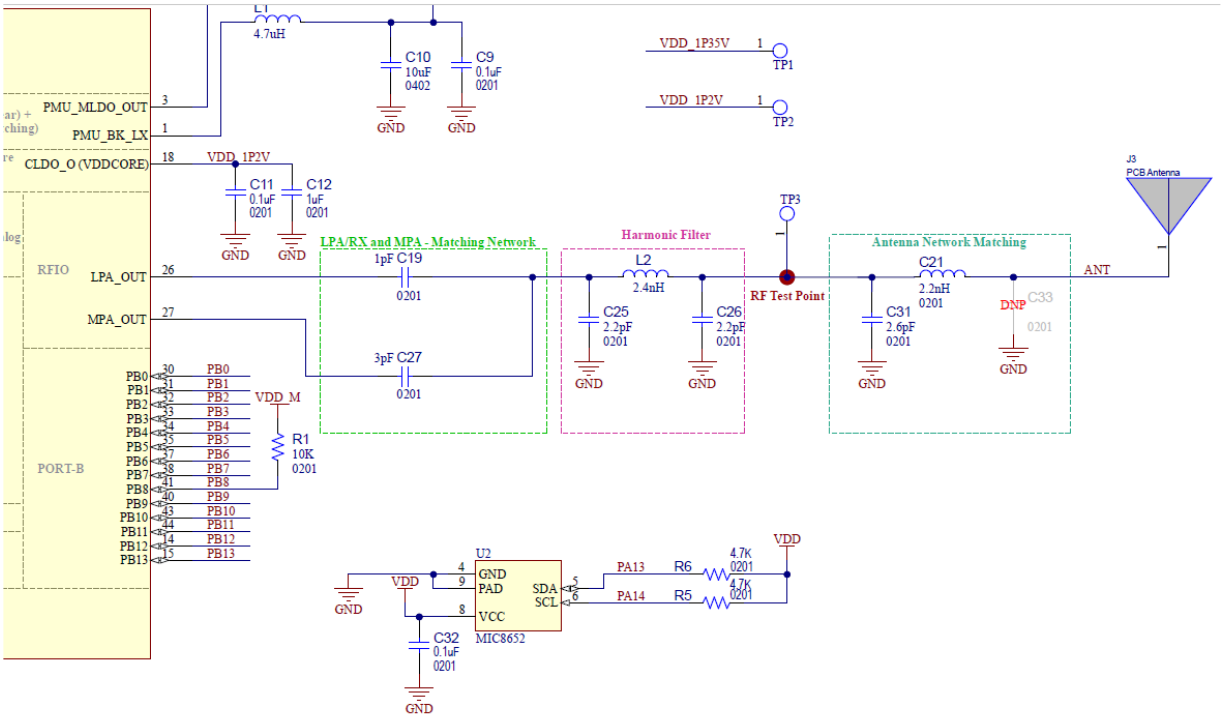
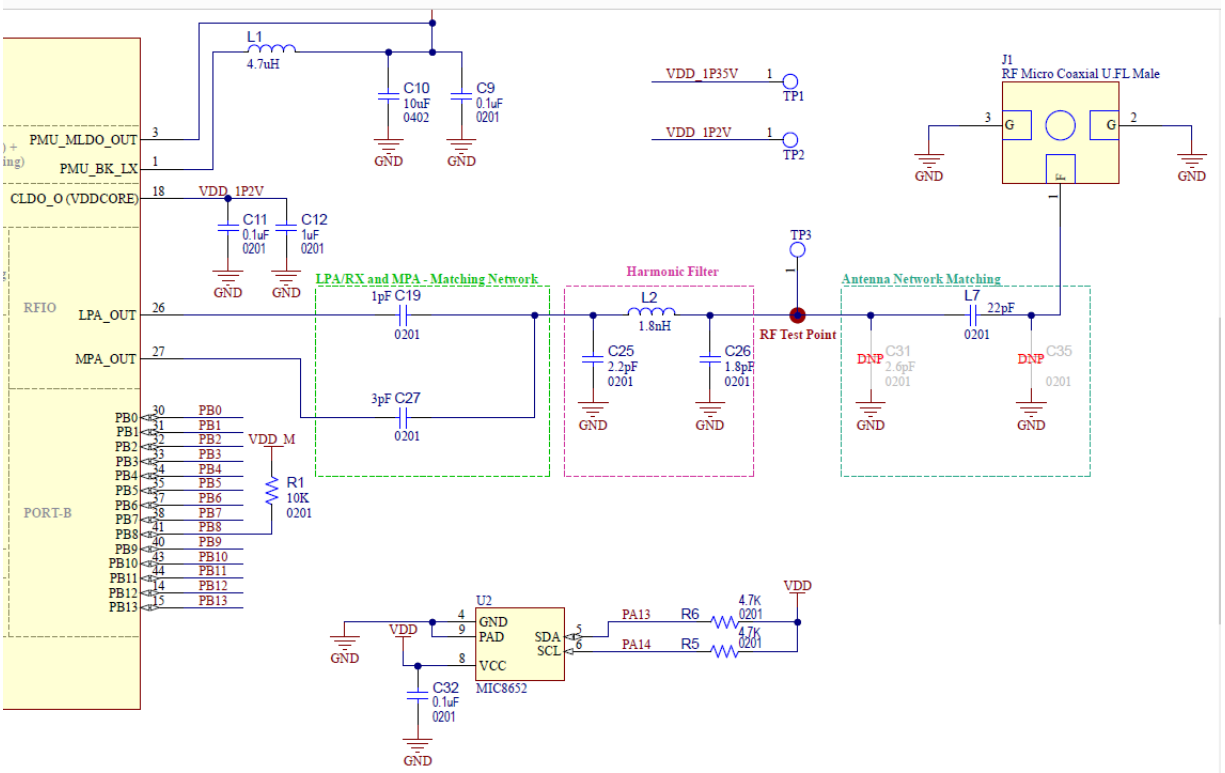


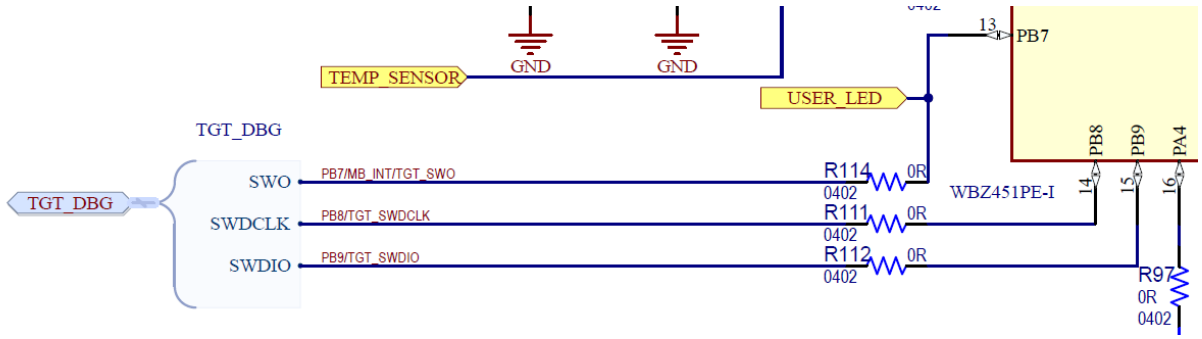
Figure 2-9. U.FL Connector Reference Design – RF Front-end Schematic Connection



2.4 Programming Interface

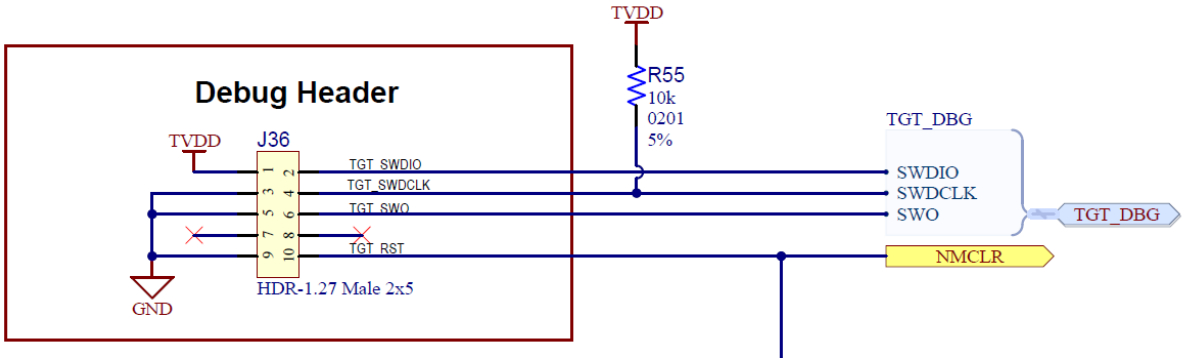
This section describes the programming and debugging interface of the PIC32CX1012BZ25048 device. This specific snapshot is taken from the WBZ451 Curiosity Board design. The pin Serial Wire Output (SWO) might not be required for general programming and debugging unless the program trace debugging is a requirement.

Figure 2-10. Programming Interface Schematic Connection



The following figure illustrates the pin-out of the Serial Wire Debug (SWD) interface required for interfacing with debuggers and/or programmers.

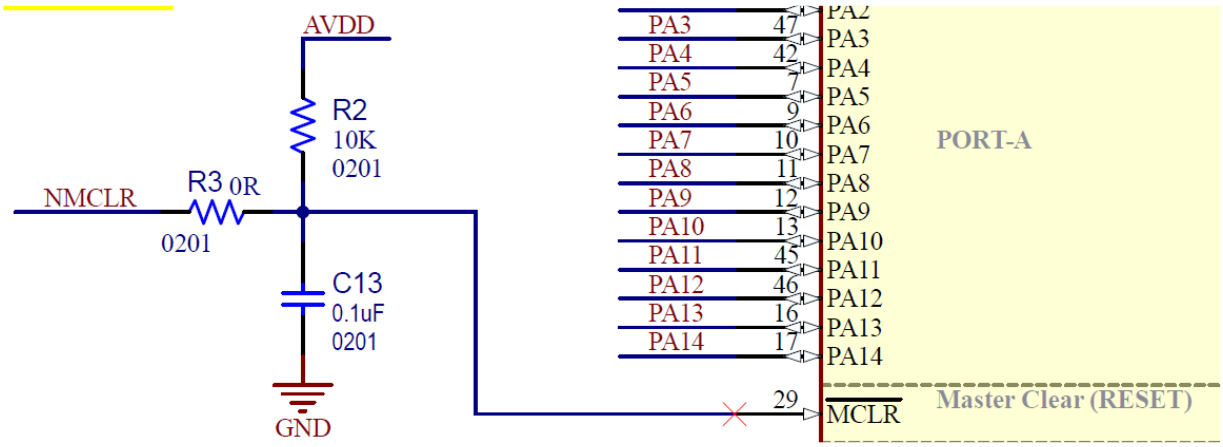
Figure 2-11. Programming Pin-out Schematic Connection



Note: For a reliable operation in a noisy environment, adding a pull-up resistor of value 10 kΩ to the SWDCLK pin (PB8) is recommended. In addition, the RC filter on the NMCLR line must be placed very close to the MCLR pin of the PIC32CX1012BZ25048 device.

The following figure illustrates the schematic connections for the RC filter to be added on the NMCLR pin.

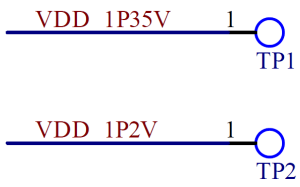
Figure 2-12. NMCLR Schematic Connection



2.5 Required Test Points

This section describes the required test points for the PIC32CX1012BZ25048 SoC-based design. Adding test points for all power rails, including VDD_1P35V and VDD_1P2V, is recommended. This is required for debugging purposes.

Figure 2-13. Power Supply Test Point



In addition, adding pins for the Universal Asynchronous Receiver-Transmitter (UART) interface, such as PA5 (TxD) and PA6 (RxD), as test points is recommended. Interface to these UART pins is required for accessing the test

mode interface using the MCHPRT3 Radio Test Tool during validation, regulatory and production testing of the PIC32CX1012BZ25048 design.

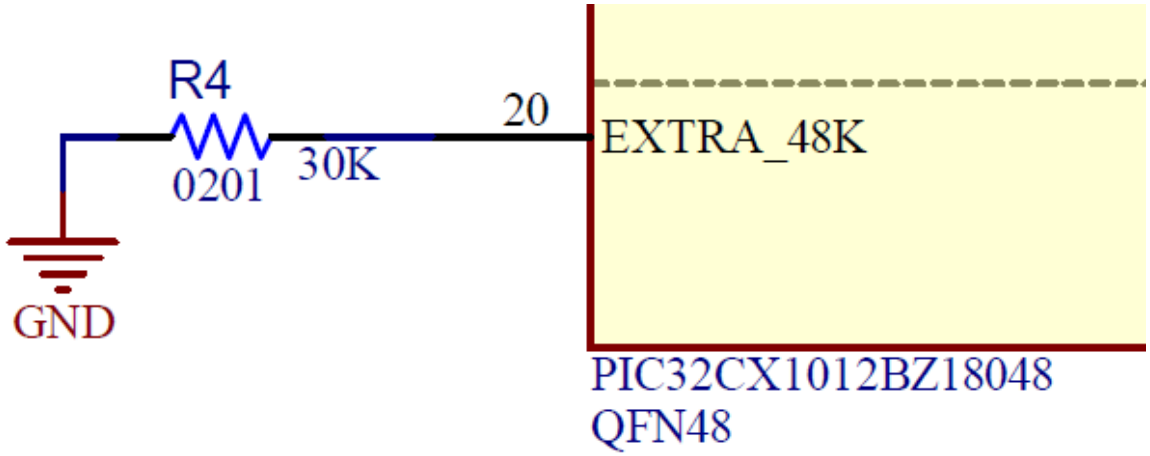
For meeting programming requirements, test points for programming interface pins (SWDIO, SWDCLK, NMCLR, VDD, GND) must be added in design.

For verifying the RF performance of the design in the production and prototype stages, adding an RF test point in the RF trace between the LPF section and the antenna network matching section is required.

2.6 Miscellaneous

- All unused or unconnected pins must be left floating with the pin configured as Input with Pull-up. This helps to ensure the design achieves the lowest power consumption.
- It is required to add a resistor of value 30 kΩ ±1% to the EXTRA_48K pin 20 of the PIC32CX1012BZ25048 device. This is required to set the internal bias voltage.

Figure 2-14. Schematic Connection for EXTRA_48K



- The peripheral functionality on the WBZ451 Curiosity Board design is only for reference purposes. The user is free to choose the peripheral functionality based on their design needs. Refer to the PPS functionality described in the *High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Data Sheet*.
- Add a placeholder for the RF shield in the schematic and the layout. This allows the RF shield to be added if required at a later stage of evaluation.

3. Layout Guidelines

3.1 Reference PCB Stack-Up

This section provides the reference PCB stack-up for a 4-layer design with 0.8 mm as PCB thickness. The reference design provided is based on the module design.

Note: If a different PCB stack-up with a different PCB thickness is required to meet the end design constraints, be sure to meet the required controlled impedance for the RF trace by maintaining the same height between layer-1 (Top layer) and layer-2 (Inner layer 1) to maintain the same trace width and spacing requirements.

Following the guidelines below is recommended for achieving the best performance:

- Top layer – Used for RF traces and signal routing
- Inner layer 1 – Used for ground plane. Ensure this ground plane is not broken by any signal traces. This ground layer must be selected immediately below the layer containing the RF traces routed from the PIC32CX1012BZ25048 device to the antenna.
- Inner layer 2 – Used for routing power traces and signal traces. Instead of using the entire plane, power traces must be routed as thick trace sufficient (around 20 mil) to minimize IR drop. The remaining part of the plane must be filled with ground polygon pour.
- Bottom layer – Used for power and signal traces

Table 3-1. Recommended PCB Stack-up

Layer Name	Layer Type	Stack-Up Details			
		Materials (um)	Finished (um)	Tolerance (um)	DK
S/M	Solder mask	—	10	—	—
TOP signal	Copper(T oz+plating)	12	35.00	±15	—
—	2116 RC55	120	220.00	±22	4.3
—	2116 RC55	120			
L2 gnd	Copper(1 oz)	35	30.00	±10	—
—	Core 130 mm	130	130.00	±10	4.3
—	Copper(1 oz)	35	30.00	±10	—
—	2116 RC55	120	220.00	±22	4.3
—	2116 RC55	120			
Bottom signal	Copper(T oz+plating)	12	35.00	±15	—
S/M	Solder mask	—	10	—	—
Laminated thickness	—	—	700	±10%	—
Overall thickness	—	—	800	±100	—

3.2 Sensitive Traces

Traces connecting to the following pins are sensitive to noise and must be isolated from signal traces/noise source with guard GND vias/GND polygon pour.

- BUCK_PLL

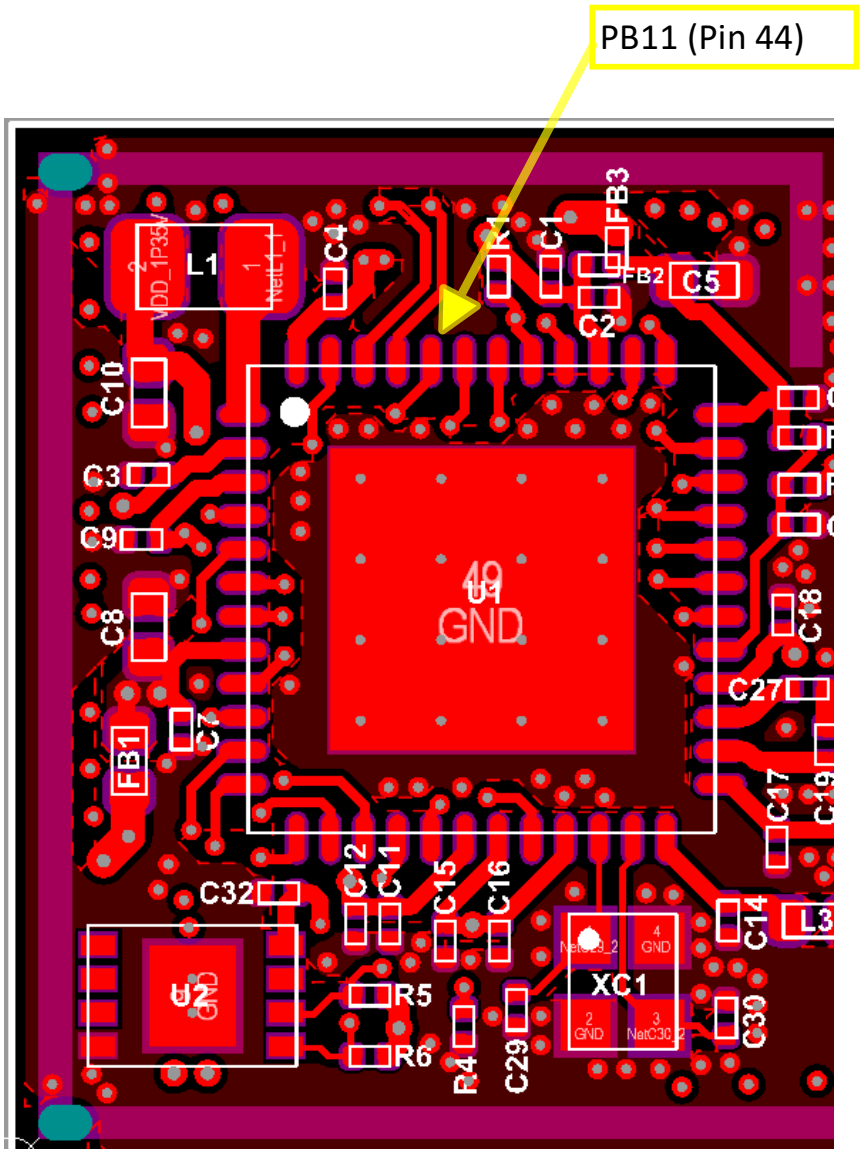
- BUCK_LPA, BUCK_BB, BUCK_CLDO
- BUCK_MPA
- AVDD
- EXTRA_48K
- XO_P/XO_N
- LPA_OUT
- MPA_OUT
- PMU_VDDIO, VPMU_VDDP
- NMCLR
- CLDO_O

3.3 Power Supply

This section describes the recommended layout guidelines with respect to power supply.

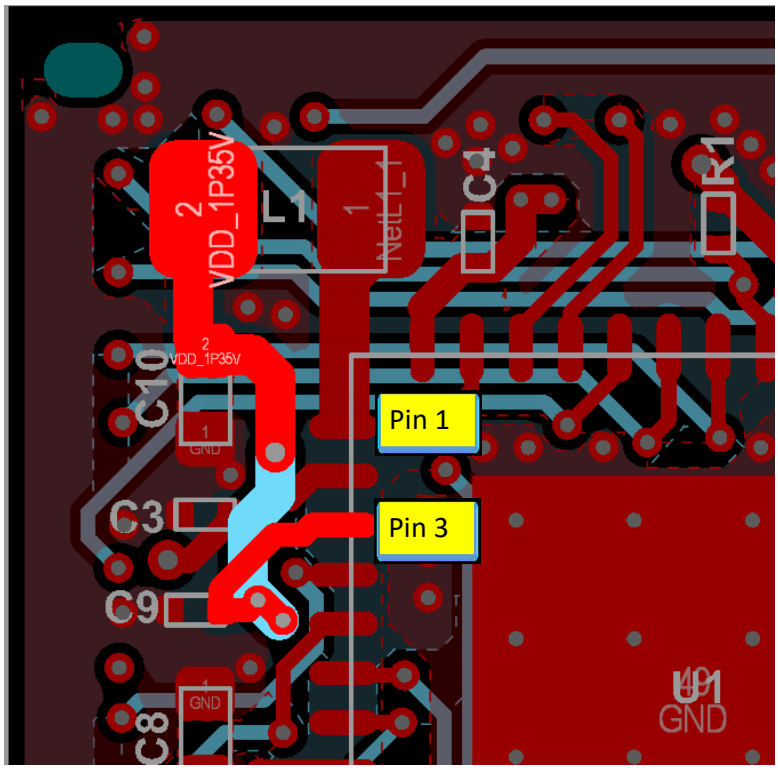
1. Place the decoupling capacitors as close to the device pin as possible. The following figure illustrates the best possible placement of all the decoupling capacitors for the PIC32CX1012BZ25048 design. To achieve this, fanning out of certain GPIOs are done with the help of traces routed towards the GND paddle followed by a via to other layers. For example, refer to pin PB11 (pin 44) in the following figure.

Figure 3-1. Top Layer Overlayed with Top Assembly



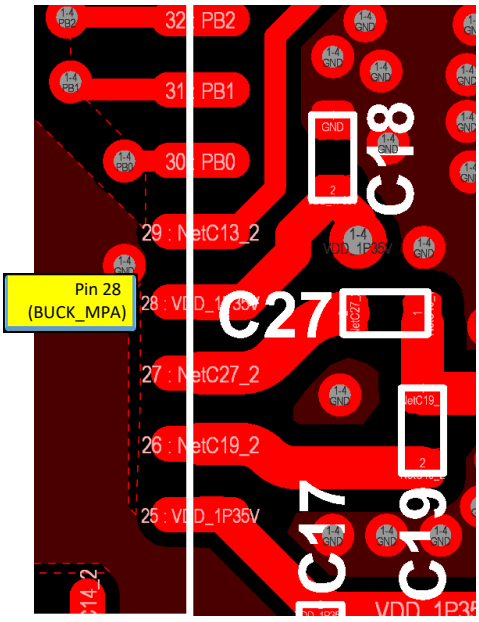
2. Ensure the loop formed by the trace from pin 1 (PMU_BK), PMU switching inductor (L1), decoupling capacitor (C10), pin 3 (PMU_MLDO) and decoupling capacitor (C9) is as short as possible. The following figure shows the best placement for these components. It is recommended to replicate this placement in the design. Ensure the trace from C10 to pin 3 (PMU_MLDO) is routed through a via to inner layer 3.
   Note: The trace is intentionally routed such that the trace after via might pass through C9 before routing to pin 3. This allows for better filtering.

Figure 3-2. PMU Output Loop



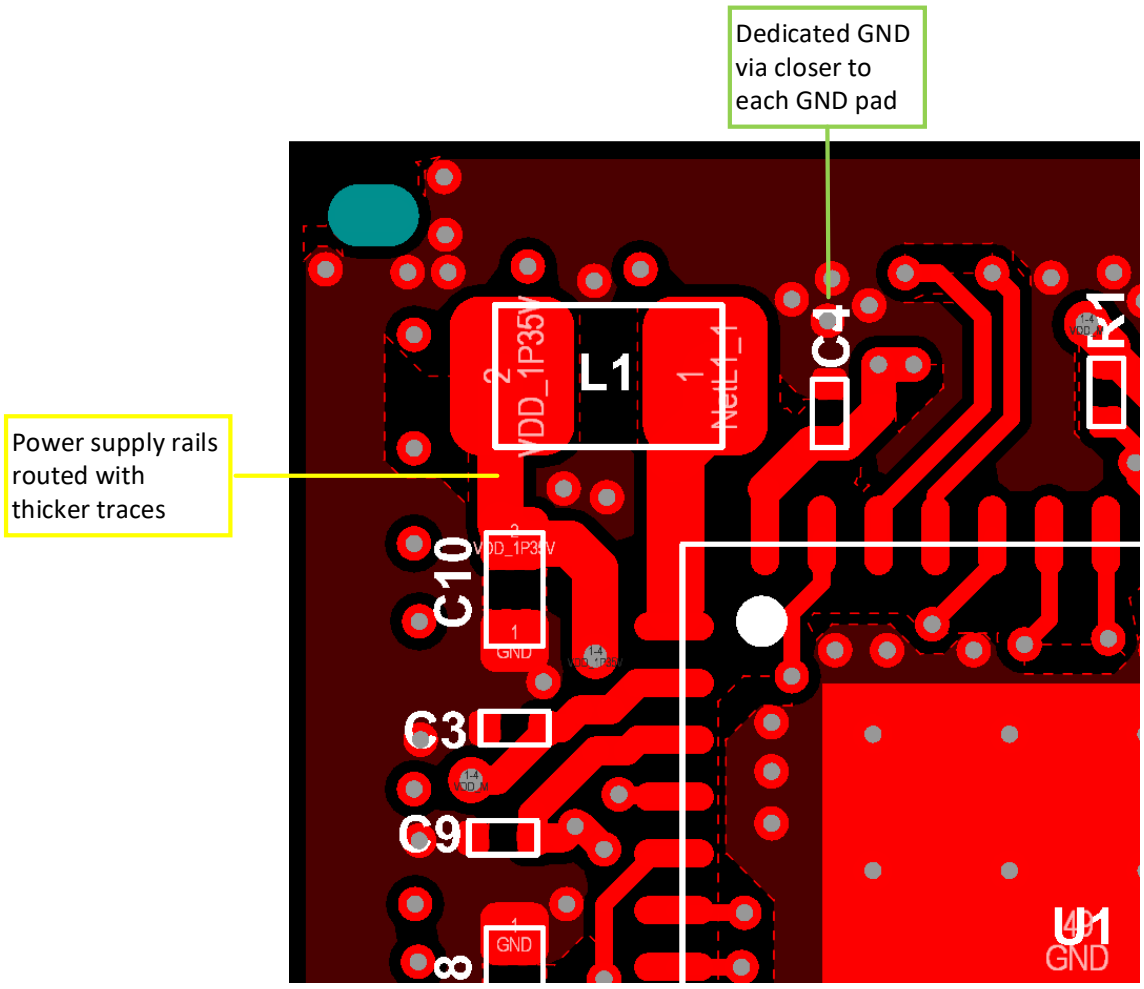
3. Ensure the decoupling capacitor to pin 28 (BUCK_MPA) is placed closer to the device pin, and, also, route the trace, such that the trace after via might pass through the decoupling capacitor (C18) before routing to pin 28.

Figure 3-3. BUCK_MPA



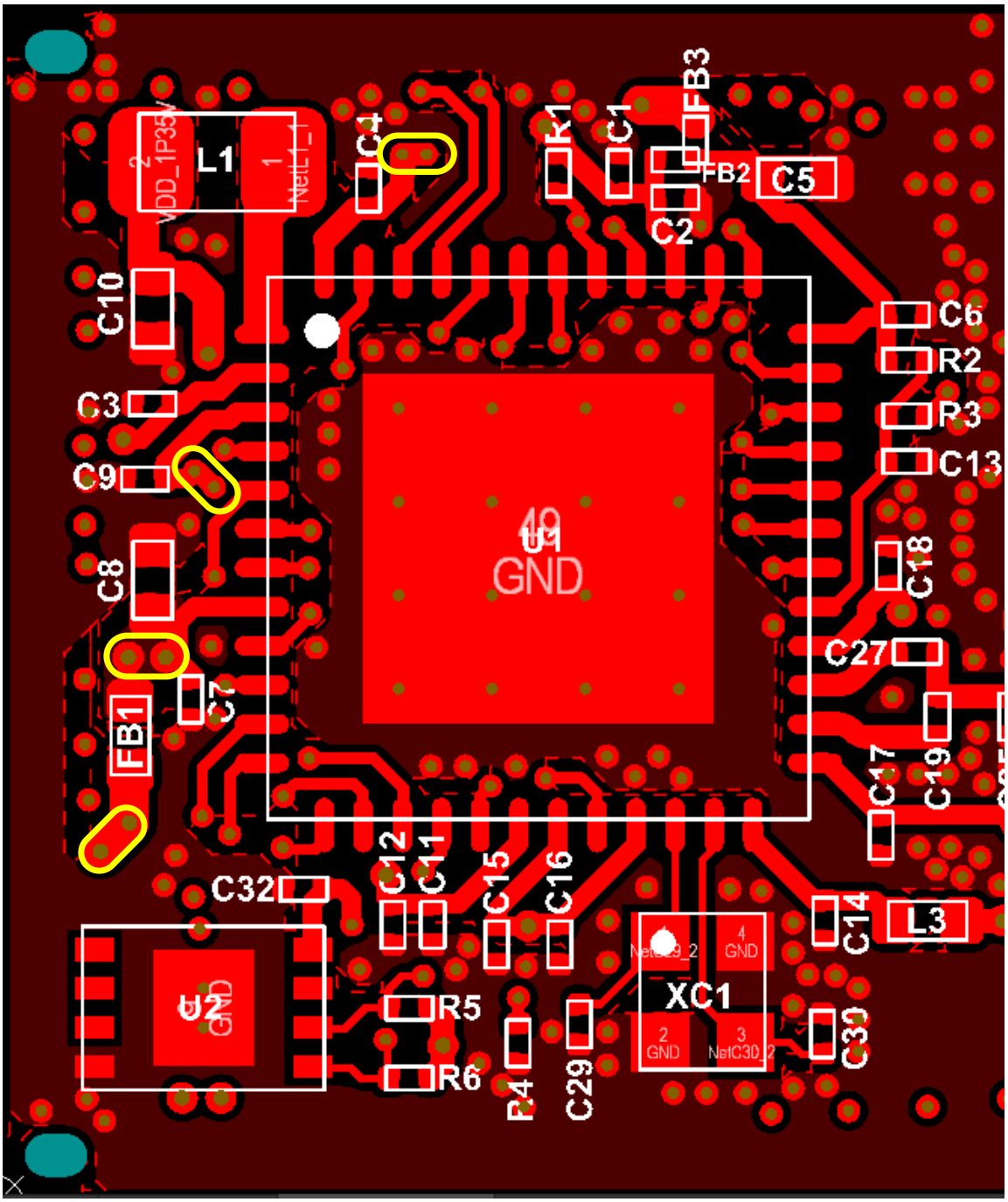
4. All power supply traces must have heavy copper fill planes to ensure the lowest possible resistance.
5. All decoupling capacitors must have a dedicated ground via placed next to the GND pad of the capacitor.

Figure 3-4. Power Traces and GND Via



6. For the connection from the primary supply trace VDD and VDD_M, use redundant vias for connecting between layers as highlighted (in Yellow) in the following figure. Also, it is recommended that large vias be used for the power supply trace to lower the inductance. The recommended via size might be 8/16 mil (hole size/diameter).

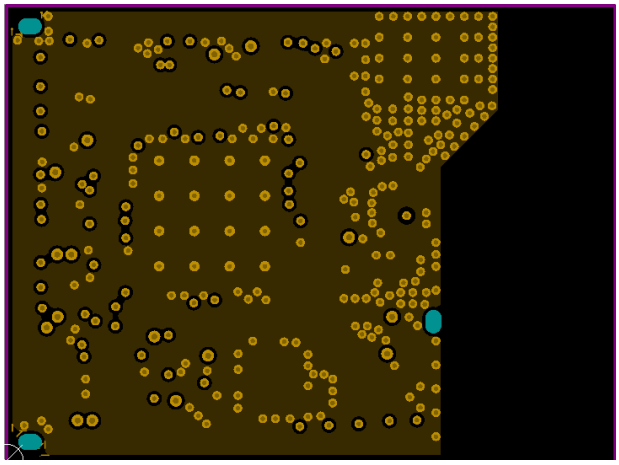
Figure 3-5. Power Supply Routing Vias



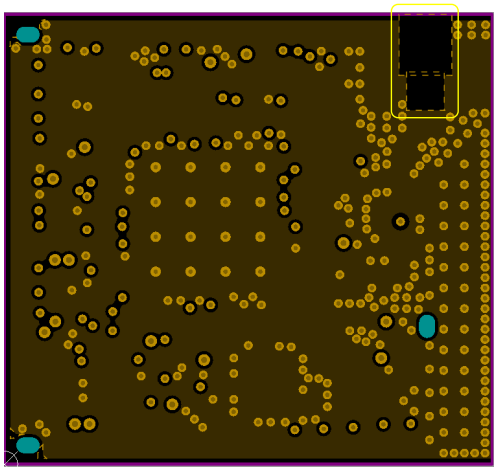
7. Inner layer 1 must be fully dedicated to GND and must not be used for routing signal/power traces. The bottom side of the PCB antenna must be free from copper. Keep enough clearance on all the layers as per the antenna recommendation. Also, the U.FL connector area must not have any conductive traces; therefore, keep the polygon cutout on this area, otherwise it impacts the impedance matching for the U.FL antenna.

Figure 3-6. Inner Layer 1(GND)

Reference Design with PCB Antenna



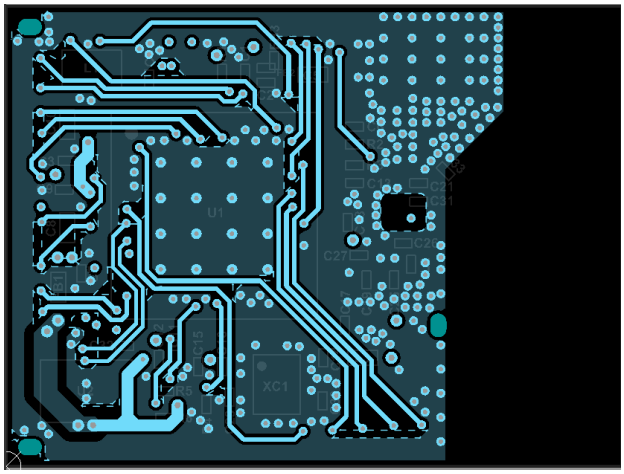
Reference Design with U.FL Connector



8. Use inner layer 2 for power and signal routing. Fill the unused areas with the GND copper pour.

Figure 3-7. Inner Layer 2

Reference Design with PCB Antenna



Reference Design with U.FL Connector

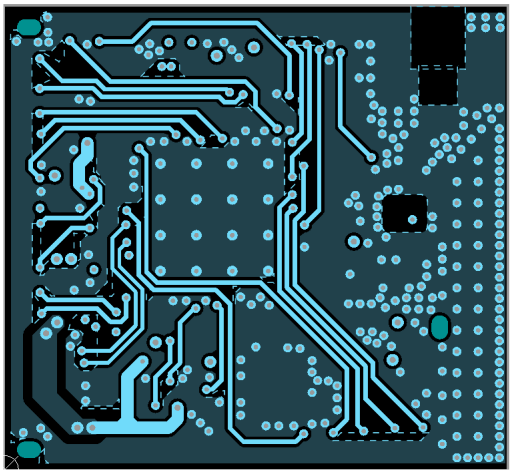
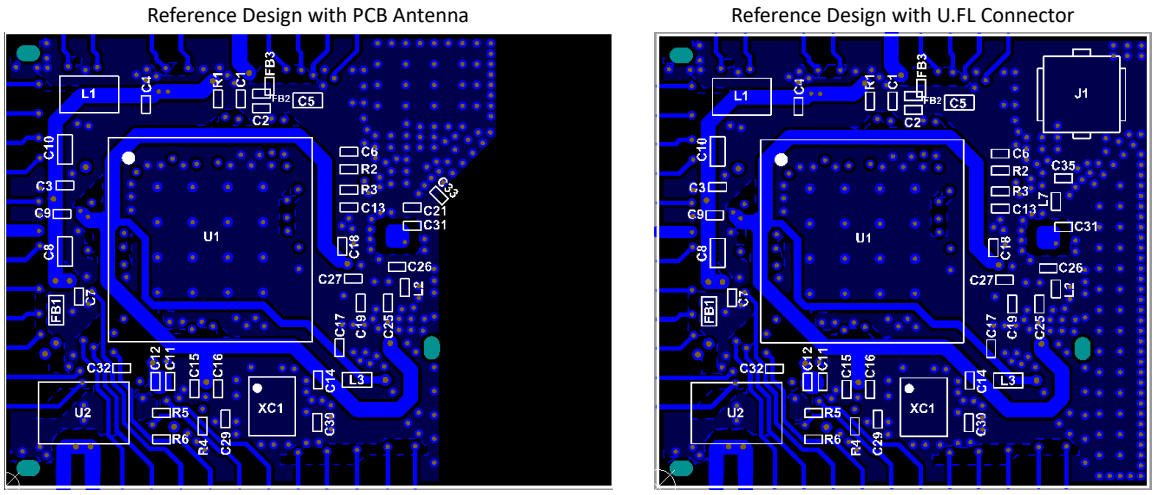
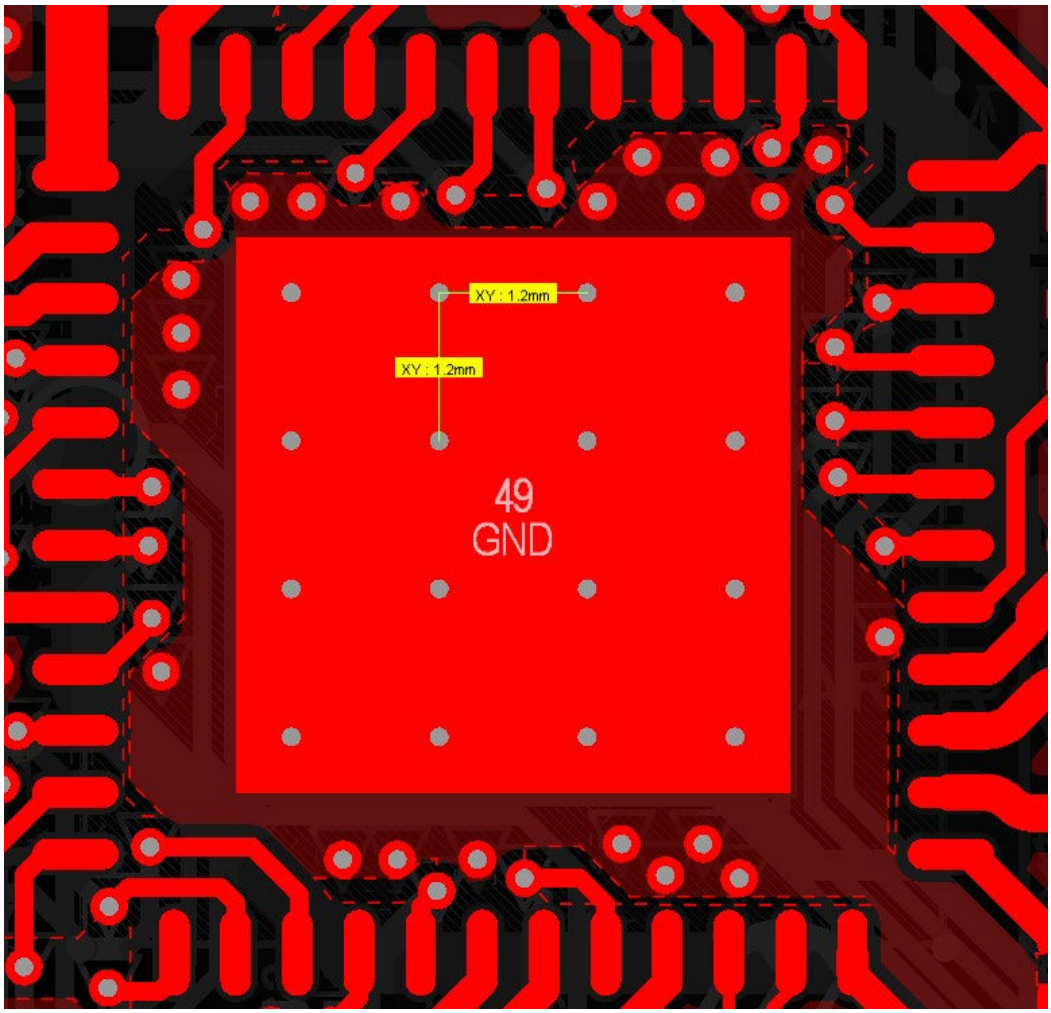


Figure 3-8. Bottom Layer Overlaid with Top Assembly



9. Figure 3-8 shows the routing of the VDD_M and VDD_1P35V traces in the bottom layer with the top assembly overlaid. Ensure the routing topology for VDD_1P35V as in the reference design with a star topology ensuring the lowest IR drop for the power rail routed to the power supply pins. Routing the VDD_1P35V trace to the following pins with isolated traces is recommended as follows:
   a. Pin 19 (BUCK_CLDO), pin 21 (BUCK_BB) and pin 25 (BUCK_LPA)
   b. Pin 24 (BUCK_PLL)
   c. Pin 25 (BUCK_MPA)
10. The VDD_1P35V trace of pin 24 (BUCK_PLL) is intentionally separated from trace to pin 19 (BUCK_CLDO), pin 21 (BUCK_BB) and pin 25 (BUCK_LPA). This is done to avoid coupling of any noise onto BUCK_PLL. Also, wherever possible, these two adjacent VDD_1P35V traces in the bottom layer were isolated with GND polygon pour and vias.
11. The GND paddle of the device must be connected to the GND of the host board through a grid of 4x4 vias with a minimum via size of 6/14 mil (hole size/diameter). The same is shown in the following figure. The vias are to be evenly spread out by about 1.2 mm from each other. This allows for a better GND connection and helps with improved thermal performance.

Figure 3-9. Recommended GND via Placement for GND Paddle



12. Place sufficient GND vias throughout the board in feasible areas to ensure the least possible inductance to the ground path.
13. Place GND vias at the edge of the design to improve the ESD/EMC performance.

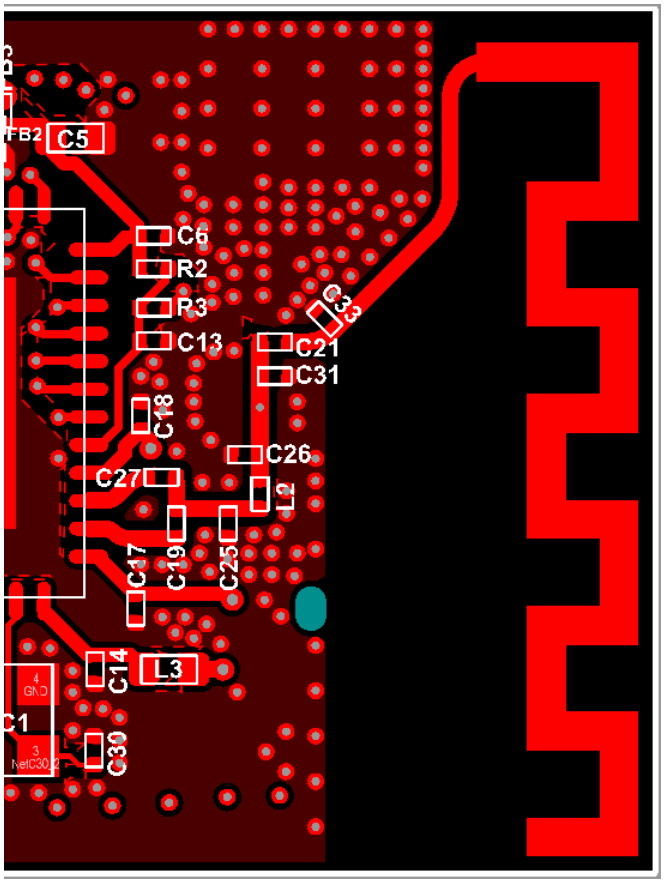
3.4 RF Traces and Components

This section describes the recommended layout guidelines with respect to RF trace routing:

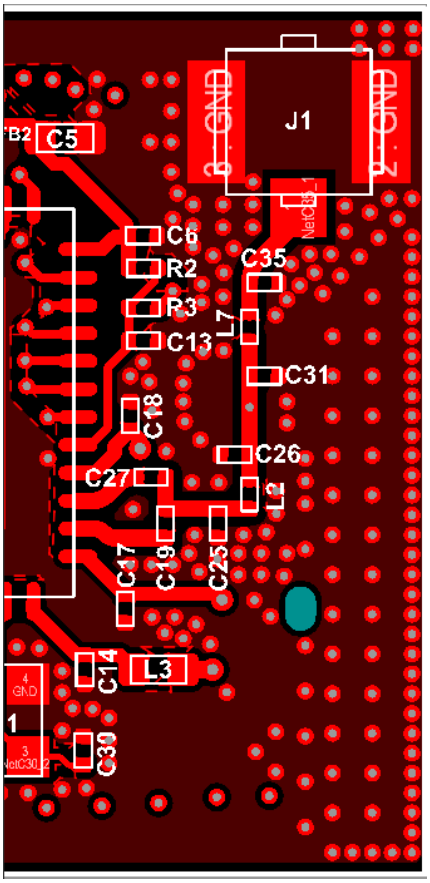
1. The RF trace routed from pins LPA_OUT (26) and MPA_OUT (27) of the PIC32CX1012BZ25048 device must be designed for a 50Ω impedance-controlled trace.
2. Be sure to isolate the RF trace from LPA_OUT and MPA_OUT until the junction of series-matching components are as they are in the reference layout design shown in Figure 3-10. A GND polygon pour with a GND via must be added in between the RF traces from LPA_OUT and MPA_OUT.
3. In this specific reference layout, RF traces are routed with a thickness of 0.302 mm with spacing to GND polygon pour at 0.158 mm. The following figure illustrates the recommended PCB stack-up details.

Figure 3-10. RF Front-end Trace Routing Overlaid with Top Assembly

Reference Design with PCB Antenna



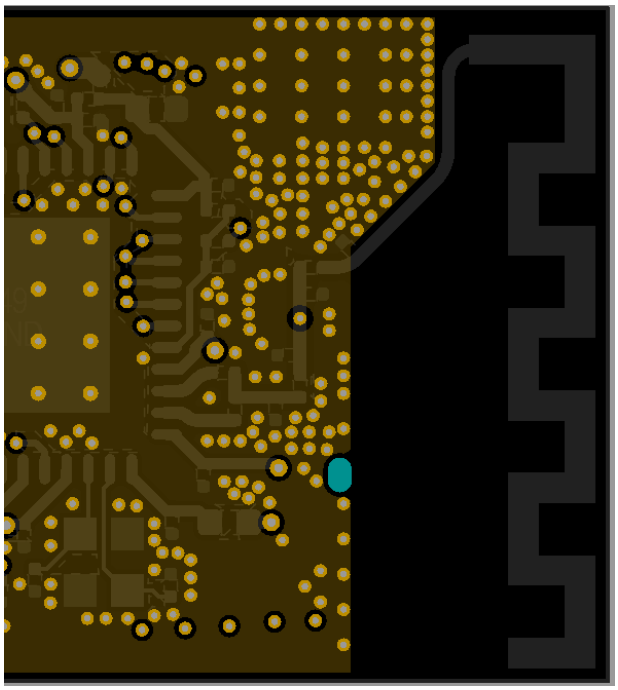
Reference Design with U.FL Connector



4. Place guard ground vias along the RF trace on either side of the trace. The PCB layer directly below the RF trace must have a ground polygon pour.
5. Do not route any signal traces below the RF trace on all the other layers. Also, do not route any signal traces adjacent to the RF trace. The following figure illustrates the locations within inner layer 2 and all the signal traces that are routed away from the RF traces.

Figure 3-11. Inner Layer 1 – RF Section

Reference Design with PCB Antenna



Reference Design with U.FL Connector

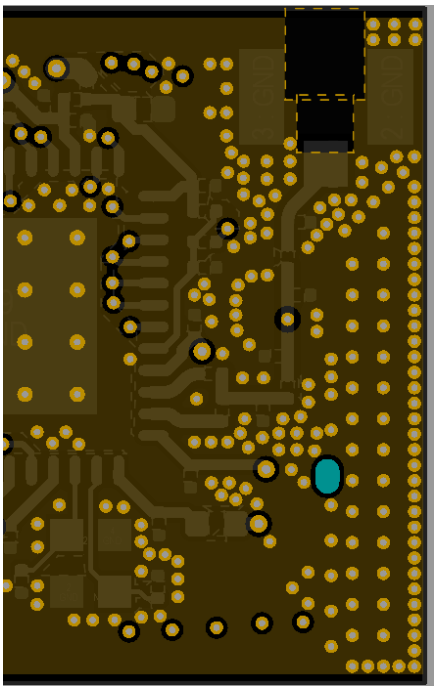
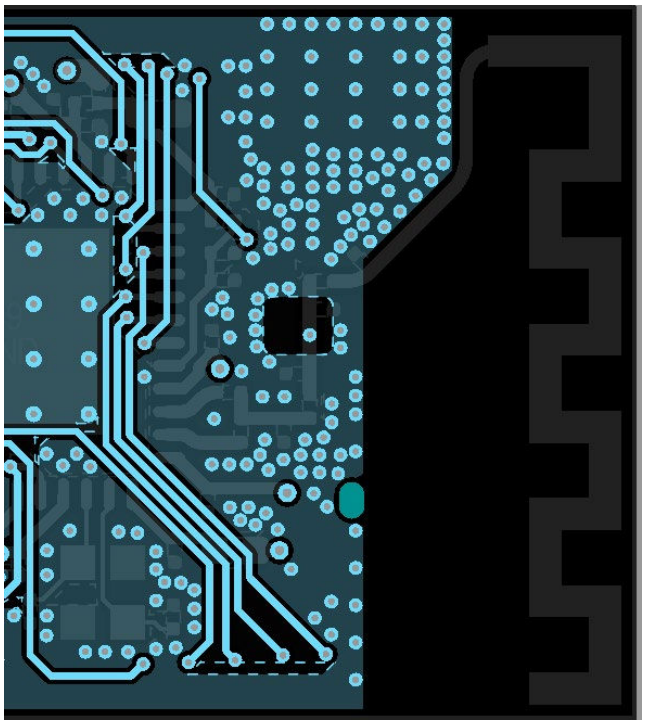


Figure 3-12. Inner Layer 2 – RF Section

Reference Design with PCB Antenna



Reference Design with U.FL Connector

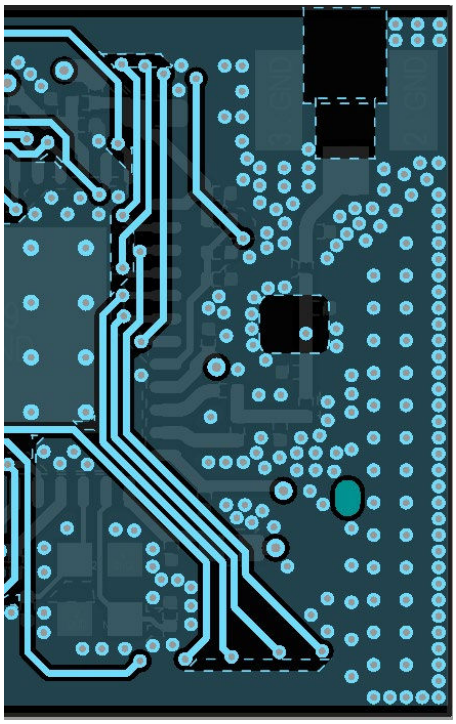
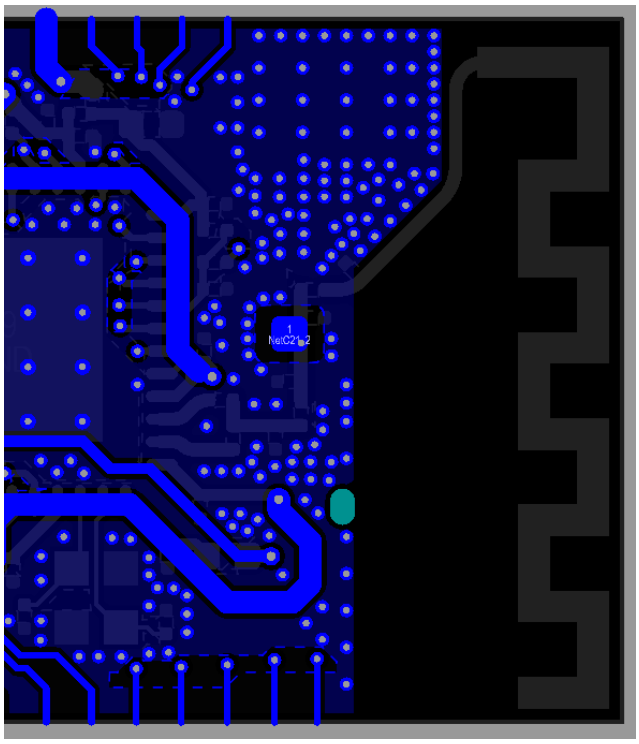
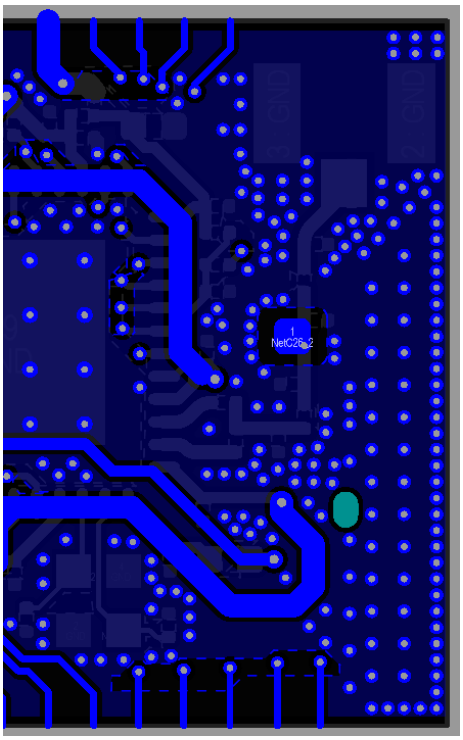


Figure 3-13. Bottom Layer – RF Section

Reference Design with PCB Antenna

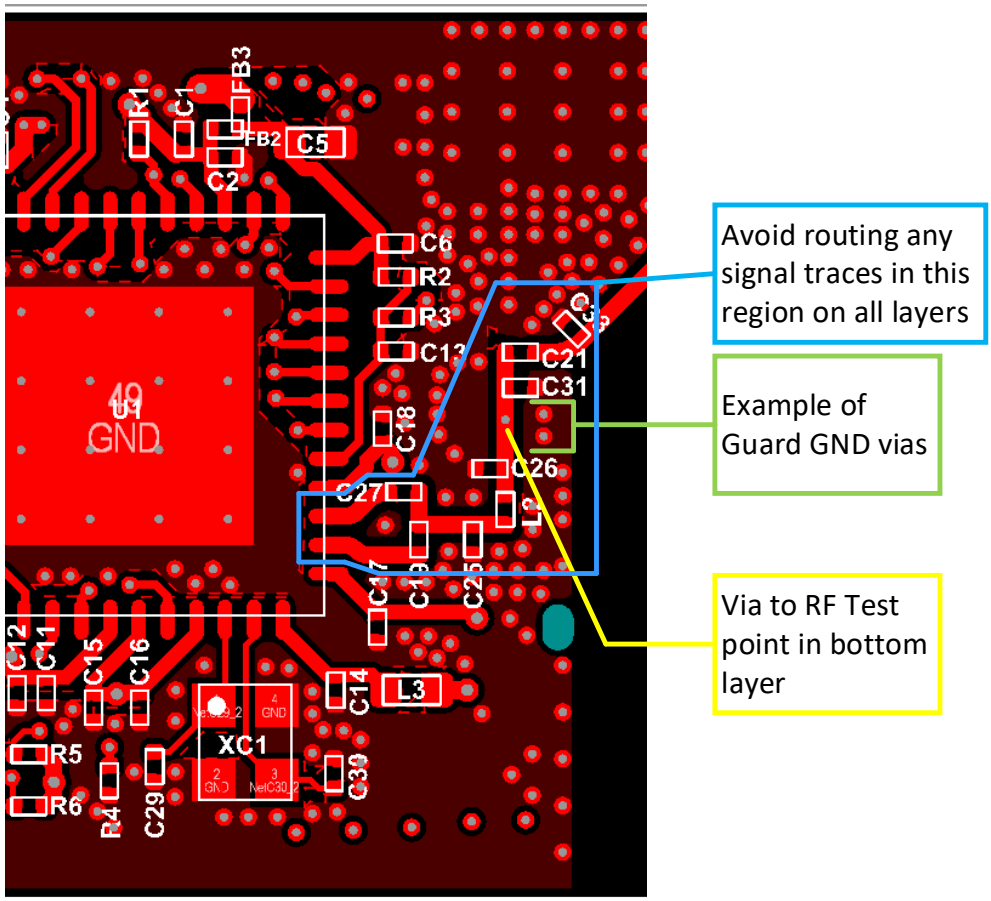


Reference Design with U.FL Connector



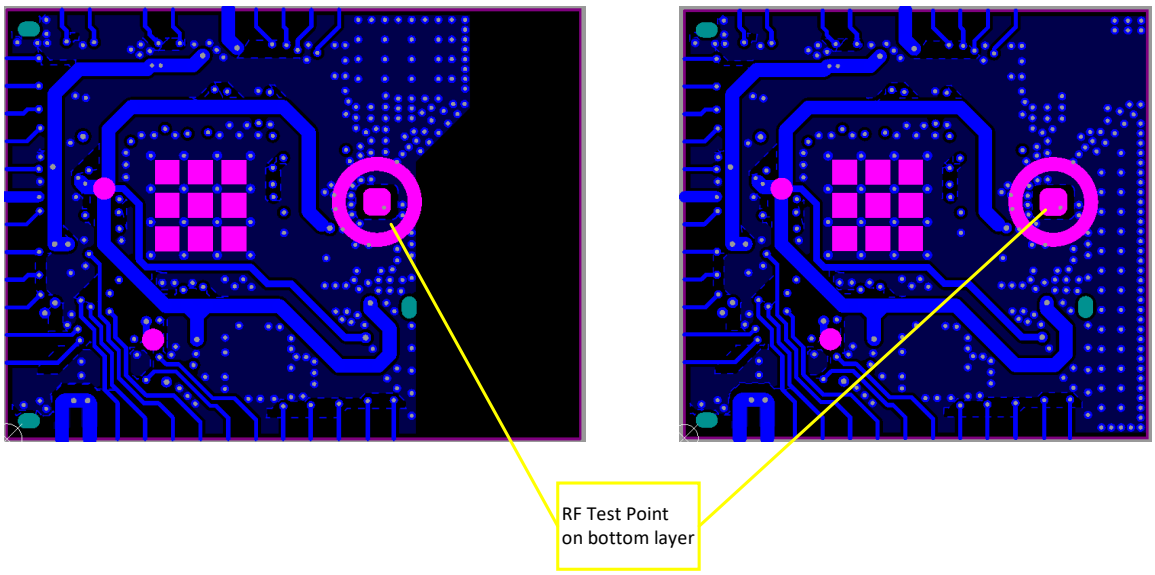
6. Do not use thermal relief pads for the ground pads of all components in the RF front-end. These pads must be completely connected to the ground copper polygon pour using the direct connect style. Place dedicated vias to ground for all these individual shunt components.

Figure 3-14. Reference Placement of Guard Ground Vias



7. Keep any components that may radiate noise or signals within the 2.4 to 2.5 GHz frequency band away from the antenna and the RF traces, and, if possible, shield these components. Any noise radiated from the board in this frequency band degrades the RF performance of the module.
8. Adding the RF test point as shown in the following figure is recommended. The circular ring around the RF test point is for the GND contact for the probe from the socket. This test point must be designed based on the recommendation of the probe structure in the test socket design. The purpose of this test point is for the measurement of RF parameters in the production test. In the production test fixture, ensure the antenna is detuned sufficiently so that the maximum RF power is coupled to the RF test point instead of the antenna.

Figure 3-15. RF Test Point in Bottom Layer with Bottom Solder Mask and Top Assembly Overlaid

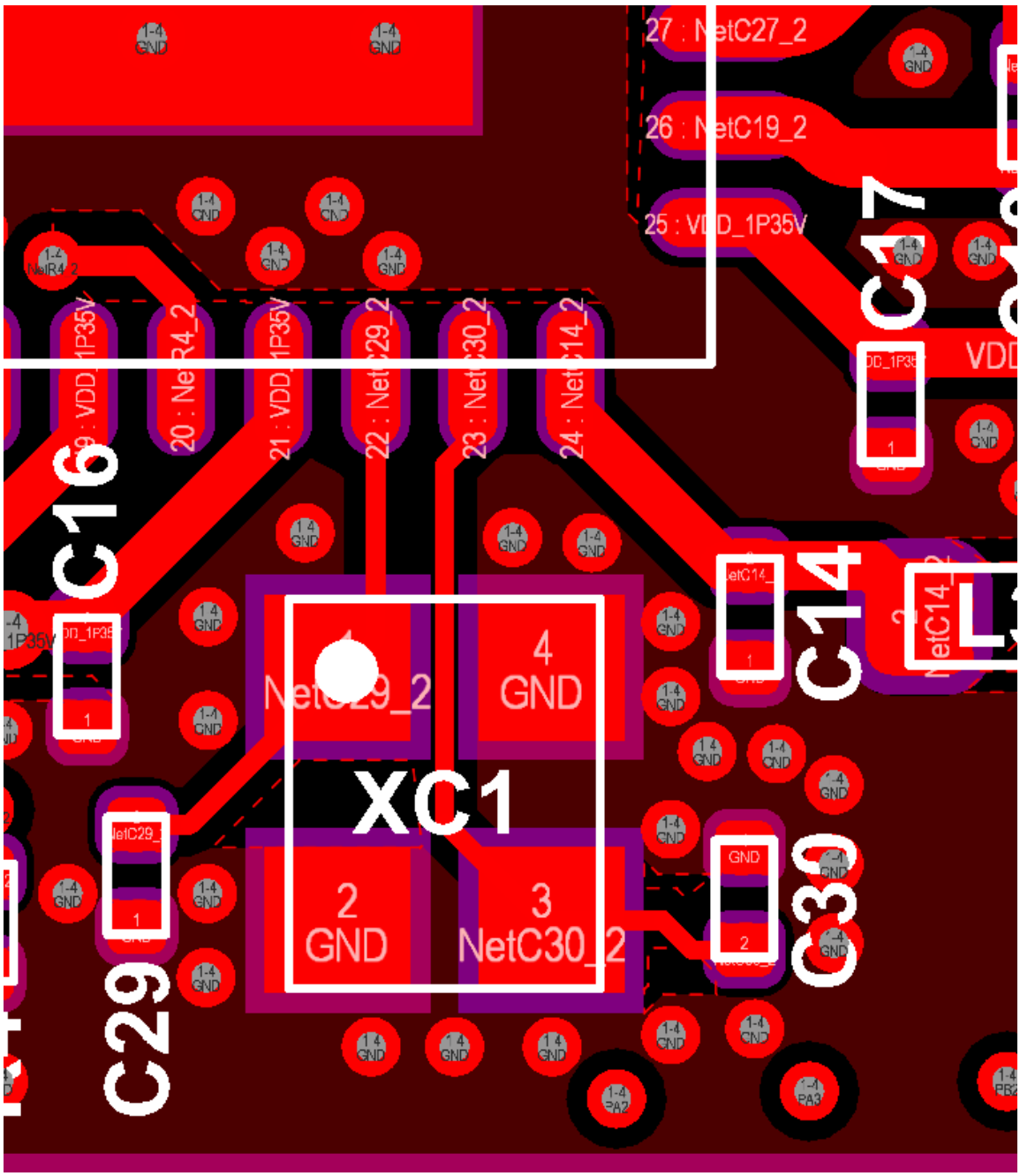


3.5 Crystal Routing

This section describes the recommended layout guidelines with respect to crystal routing:

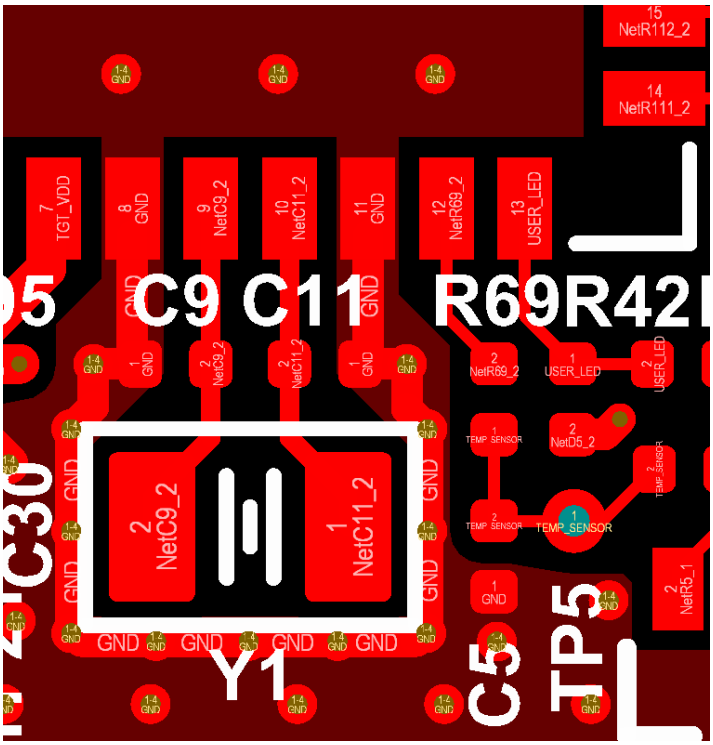
1. Keep the traces from the device pads to the crystal as short as possible.
2. Place the guard ground vias all along the trace routed to crystal. See Figure 3-16 for the entire area around the trace to pin 22 (XO_N) and pin 23 (XO_P).
3. Surround the area around the crystal with ground polygon pour, and place sufficient ground vias in this polygon pour.
4. Do not route any signal traces below the crystal area in all the other layers. Also, do not route any signal traces adjacent to the crystal trace. Specific care must be taken to isolate any known noisy signal traces, such as GPIOs intended to be fast toggling, from crystal traces with proper polygon ground pour and sufficient GND vias.

Figure 3-16. Recommended 16 MHz Crystal Placement



5. Like Figure 3-16, SOSC (32.768 kHz) crystal is to be placed as shown in the following figure. This is a layout snippet from the WBZ451 Curiosity Board.

Figure 3-17. Recommended 32.768 kHz Crystal Placement



3.6 Miscellaneous

This section describes the general layout guidelines.

1. Keep any large metal objects as far away from the antenna as possible to avoid electromagnetic field blocking.
2. Avoid enclosing the antenna in a metal shield.
3. Keep any components that may radiate noise or signals within the 2.4 GHz to 2.5 GHz frequency band away from the antenna and, if possible, shield those components. Any noise radiated by the Host board in this frequency band reduces the device's sensitivity.
4. Ensure that the traces route directly through the pads of the filter capacitors and not by a stub route. The following figure illustrates the correct way to route through a capacitor pad.

Figure 3-18. Correct Routing Through Filtering Capacitor Pad

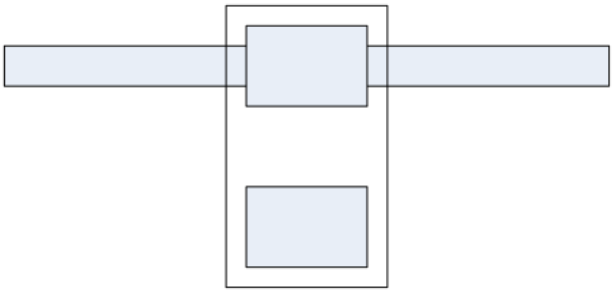
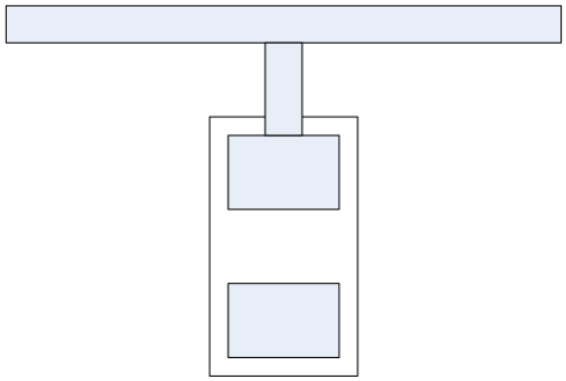


Figure 3-19. Incorrect Stub Routing to Filtering Capacitor Pad



4. Antenna Guidelines

1. External antenna certified with the WBZ451 module based on the PIC32CX1012BZ25048 device are listed on the WBZ451 Data Sheet. Refer to the *High-performance 2.4 GHz Multi-protocol Wireless MCUs and Modules, supporting Bluetooth Low Energy and 802.15.4 protocols with 32-bit ARM® Cortex®-M4F, 2 Msps 12-bit ADC Data Sheet* for more information. If any other antenna is chosen because of some end-product constraints, ensure that the antenna covers the desired frequency band, from 2.4 to 2.5 GHz.
2. If any other antenna (PCB antenna or Chip antenna) is chosen, follow the footprint and other layout recommendations as per the antenna data sheet/guidelines.
3. Ensure the dimension of the ground plane in the board meets the dimension requirement specified in the antenna data sheet. A reduced ground plane dimension might reduce the efficiency achieved with the same antenna.
4. Place the antenna impedance-matching components as close to the antenna pad as possible.

5. Design Checklist

This section is intended to be used by a designer for self-review of their PIC32CX designs. This section is a consolidation of all the guidelines recommended for a PIC32CX design.

5.1 Schematic Checklist

Table 5-1. Schematic Checklist

S.No	Item Description	Verified (Yes/No)	Remarks
1	Verify the decoupling capacitor requirements are met for all power supply pins (VDD, VPMU_VDD, VPMU_VDD, AVDD).		
2	Verify the decoupling capacitor requirements are met for all the BUCK power supply pins (BUCK_CLDO, BUCK_BB, BUCK_PLL, BUCK_MPA and BUCK_LPA).		
3	Verify the decoupling capacitor requirements are met for all the CLDO_O pins.		
4	Verify the filtering requirement (Ferrite beads) for AVDD and power rail.		
5	Verify the LC circuit components for DC-DC section is as per the recommendation, and verify that the same part numbers are being used.		
6	Is GND paddle connected to GND?		
7	Is power budgeting performed to ensure the power source is capable to supply the required current to the circuit in all functional conditions? It might be required to choose a power supply with maximum current handling at 125-130% of the estimated power budget.		
8	Verify whether the chosen 16 MHz RF crystal meets the following requirements: 1. Frequency 2. Frequency tolerance including temperature and aging 3. Load capacitance requirements of both crystal and device		
9	Verify the addition of the 32.768 kHz crystal to the design.		
10	Verify that the design replicates the reference design for the RF section with same components and schematic.		
11	Verify the addition of test points for the programming interface (SWDIO, SWDCLK, NMCLR, VDD, GND), critical power rails (VDD_1P35V and VDD_1P2V), RF and UART interface for regulatory testing (such as PA5 (TxD) and PA6 (RxD)).		
12	Verify the addition of pull-up resistor of value 10 kΩ to the SWDCLK.		
13	Verify the addition of recommended bias resistor to pin 20 (EXTR).		
14	Verify the addition of current limiting resistors for I/O pins interfaced to LED, buttons and so on.		
15	Verify the addition of an RF shield placeholder in design.		

.....continued			
S.No	**Item Description**	**Verified (Yes/No)**	**Remarks**
16	For unused pins, review the recommendation and handle the pin status accordingly.		

5.2 PCB Layout Checklist

Table 5-2. PCB Layout Checklist

S.No	Item Description	Verified (Yes/No)	Remarks
1	Verify whether the PCB stack-up matches with the reference design for achieving the best performance.		
2	Verify that the decoupling capacitors for all power supply pins (VDD, VPMU_VDD, VPMU_VDD, AVDD), BUCK power supply pins (BUCK_CLDO, BUCK_BB, BUCK_PLL, BUCK_MPA and BUCK_LPA) and CLDO_O are placed closest possible to the IC pin.		
3	Verify the PCB trace thickness for power rail is adequate for the estimated current consumption.		
4	Verify that all the decoupling capacitors have a dedicated GND via placed adjacent to the GND pad. Avoid sharing the GND via for different components.		
5	Verify the loop formed PMU_BK, PMU switching inductor, decoupling capacitor and PMU_MLDO is as short as possible. Replicate this section of design as it is in the reference design.		
6	Verify the addition of redundant vias for power rails and GND, wherever possible.		
7	Verify that there are no signal or power traces routed in the Inner layer 1(Layer immediately below the device/RF traces). Dedicating this layer for GND is recommended.		
8	Ensure the PCB routing topology for the 1P35V trace is as per the reference layout for achieving the best performance with least IR voltage drop.		
9	Verify the addition of grid of 4x4 vias with the recommended via size and spacing.		
10	Verify with the PCB vendor and confirm that the single-ended impedance of RF trace is 50Ω.		
11	Verify the placement of guard GND vias all around the RF trace.		
12	Verify that there are no traces routed and no polygon pour split (such as, reference plane split) in all the layers under the RF routing area.		
13	Verify that all the shunt components in the RF section use direct connect polygon style instead of the usual thermal relief polygon connect style.		

.....continued

S.No	Item Description	Verified (Yes/No)	Remarks
14	Verify that the trace to crystal from device pins is as short as possible and also covered with guard GND vias and polygon pour on either side to improve isolation.		
15	Ensure the test points of critical power rails are sufficiently isolated from noise sources.		
16	Verify the addition of placeholder RF shield footprint in the PCB layout.		
17	Verify the addition of RF test point in the RF trace for production test.		
18	Verify the addition of GND stitching vias in the entire board area wherever possible and at the PCB edges.		
19	Verify there are no errors by running a Design Rule Checking (DRC) check provided by the CAD tool.		

6. Document Revision History

Revision	Date	Section	Description
A	10/2022	Document	Initial revision

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