DATA_ADDR_sample_mode process

sig_ADC_ADDR = 0x0000
sig_ADC_DATA = 0x0000
sig_ADC_CLK_to_mem_dist = 0
sig_RnW_to_mem_dist_out = 1 (Read mode)

← 1 (done)

i_ADC_DnB?

0 (busy) →

sig_ADC_ADDR = Currnet write address
sig_ADC_DATA = input ADC data
sig_ADC_CLK_to_mem_dist = i_ADC_DATA_RDY
sig_RnW_to_mem_dist_out = 0 (Write mode)
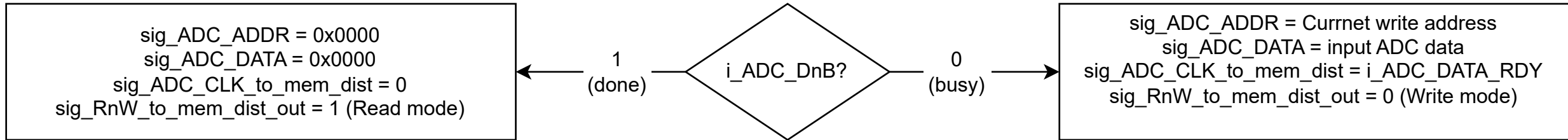
DATA_ADDR_read_mode process

sig_int_mem_data = i_DATA_MDIST
sig_int_mem_ADDR = Current read address
sig_CLK_from_int_mem = i_CLK_IXMUX
sign_RnW_to_mem_dist_out_nB = 1

← 1 (done)

i_ADC_DnB?

0 (busy) →

sig_int_mem_data = 0x0000
sig_int_mem_ADDR = 0x0000
sig_CLK_from_int_mem = 0
sign_RnW_to_mem_dist_out_nB = 0