

TLV906xS 10-MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems

1 Features

- Rail-to-rail input and output
- Low input offset voltage: ± 0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: $10 \text{ nV}/\sqrt{\text{Hz}}$
- Low input bias current: 0.5 pA
- Low quiescent current: 538 μA
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version: TLV906xS
- Extended temperature range: -40°C to 125°C

2 Applications

- E-bikes
- Smoke detectors
- HVAC: heating, ventilating, and air conditioning
- Motor control: AC induction
- Refrigerators
- Wearable devices
- Laptop computers
- Washing machines
- Sensor signal conditioning
- Power modules
- Barcode scanners
- Active filters
- Low-side current sensing

3 Description

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) are single-, dual-, and quad- low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the OPAx316 and TLVx316 devices.

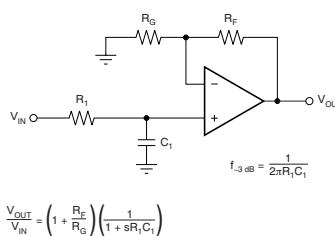
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|---------------------------|-------------------|
| TLV9061 | SOT-23 (5) | 1.60 mm x 2.90 mm |
| | SC70 (5) | 1.25 mm x 2.00 mm |
| | SOT553 (5) ⁽²⁾ | 1.65 mm x 1.20 mm |
| | X2SON (5) | 0.80 mm x 0.80 mm |
| TLV9061S | SOT-23 (6) | 1.60 mm x 2.90 mm |
| TLV9062 | SOIC (8) | 3.91 mm x 4.90 mm |
| | TSSOP (8) | 3.00 mm x 4.40 mm |
| | VSSOP (8) | 3.00 mm x 3.00 mm |
| | SOT-23 (8) | 1.60 mm x 2.90 mm |
| | WSON (8) | 2.00 mm x 2.00 mm |
| TLV9062S | VSSOP (10) | 3.00 mm x 3.00 mm |
| | X2QFN (10) | 1.50 mm x 2.00 mm |
| TLV9064 | SOIC (14) | 8.65 mm x 3.91 mm |
| | TSSOP (14) | 4.40 mm x 5.00 mm |
| | WQFN (16) | 3.00 mm x 3.00 mm |
| | X2QFN (14) | 2.00 mm x 2.00 mm |
| TLV9064S | WQFN (16) | 3.00 mm x 3.00 mm |

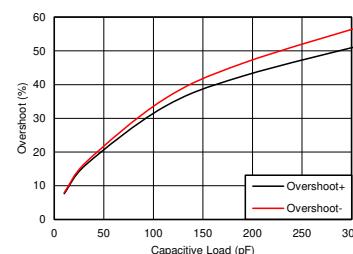
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is for preview only.

Single-Pole, Low-Pass Filter



Small-Signal Overshoot vs Load Capacitance



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (May 2019) to Revision J

| | Page |
|--|------|
| • Deleted TLV9062IDDFR (SOT-23 (8)) package preview notations throughout data sheet..... | 1 |
| • Added industry standard package names to <i>Device Comparison Table</i> | 5 |
| • Added note to packages with thermal pads, specifying that the thermal pads need to be connected to V–..... | 7 |
| • Added link to <i>Shutdown Function</i> section in <u>SHDN</u> pin function rows | 11 |
| • Added <i>EMI Rejection</i> section to the <i>Feature Description</i> section | 24 |
| • Changed <i>Shutdown Function</i> section to add more clarification | 25 |

Changes from Revision H (April 2019) to Revision I

| | Page |
|--|------|
| • Added DDF (SOT-23) thermal information to replace TBDs | 13 |

Changes from Revision G (December 2018) to Revision H

| | Page |
|---|------|
| • Added SOT-23 (8) information to <i>Device Information</i> | 1 |
| • Added DDF package column to <i>Device Comparison Table</i> | 5 |
| • Added DDF (SOT-23) package to <i>Pin Functions</i> | 7 |
| • Added DDF (SOT-23) package to <i>Thermal Information</i> | 13 |
| • Added TLV9062 RUG (X2QFN) thermal information to replace TBDs | 14 |

Changes from Revision F (September 2018) to Revision G
Page

| | |
|--|----|
| • Changed TLV9064 RUC package name From WQFN (14) : To X2QFN (14) in <i>Device Information</i> table | 1 |
| • Added TLV9064 RUC (X2QFN) pinout drawing to <i>Pin Configuration and Functions</i> section..... | 9 |
| • Added RUC (X2QFN) package pinout information to Pin Functions: TLV9064 table | 9 |
| • Added RUC (X2QFN) to Thermal Information: TLV9064 table | 14 |

Changes from Revision E (July 2018) to Revision F
Page

| | |
|--|----|
| • Deleted Shutdown part numbers from datasheet header | 1 |
| • Deleted X2QFN (10) package from TLV9062 Device Information table | 1 |
| • Added references to shutdown part numbers in Description section | 5 |
| • Changed TLV906xS series to TLV906xS family throughout datasheet | 5 |
| • Added Shutdown devices to Device Comparison Table | 5 |
| • Changed pin namings for all pinout drawings to reflect updated nomenclature | 6 |
| • Added TLV9061S Thermal Information Table..... | 13 |
| • Added TLV9064S Thermal Information Table..... | 14 |
| • Deleted Partial Shutdown Amplifier Enable Time | 16 |
| • Added clarification on selecting resistors for a current sensing application in the Typical Applications Section | 27 |
| • Changed wording of third bullet in Layout Guidelines..... | 29 |

Changes from Revision D (June 2018) to Revision E
Page

| | |
|---|----|
| • Added TLV9061S device to <i>Device Information</i> table..... | 1 |
| • Added TLV9064S device to <i>Device Information</i> table..... | 1 |
| • Added RUC and RUG packages to the <i>Device Comparison</i> table | 5 |
| • Added TLV9061S DBV (SOT-23) pinout drawing to <i>Pin Configuration and Functions</i> section | 7 |
| • Added TLV9061S DBV (SOT-23) package pinout information to <i>Pin Functions: TLV9061S</i> table | 7 |
| • Added TLV9062S RUG (VSSOP) package pinout drawing to <i>Pin Configuration and Functions</i> section | 8 |
| • Added TLV9062S RUG (VSSOP) package pinout information to <i>Pin Functions: TLV9062S</i> table | 8 |
| • Added TLV9064 RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section | 9 |
| • Added TLV9064 RTE pinout information to <i>Pin Functions: TLV9064</i> table | 9 |
| • Added TLV9064S RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section | 11 |

Changes from Revision C (March 2018) to Revision D
Page

| | |
|---|----|
| • Added shutdown suffix to "TLV906x" to document title..... | 1 |
| • Added "Shutdown Version" bullet to <i>Features</i> list | 1 |
| • Added TLV9062S device to <i>Device Information</i> table..... | 1 |
| • Added shutdown text to <i>Description (continued)</i> section | 5 |
| • Added "(V _S = [V+] – [V-]) supply voltage parameter in <i>Absolute Maximum Ratings</i> table..... | 12 |
| • Added "input voltage range" and "output voltage range" parameters and values to <i>Recommended Operating Conditions</i> table | 12 |
| • Added shutdown pin recommended operating conditions in <i>Recommended Operating Conditions</i> table | 12 |
| • Added "T _A " symbol to "specified temperature" parameter to <i>Recommended Operating Conditions</i> table | 12 |
| • Added <i>Thermal Information: TLV9062S</i> thermal table data | 14 |
| • Added <i>Thermal Information: TLV9062S</i> thermal table data | 14 |
| • Added shutdown section to <i>Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V-) = 1.8 V to 5.5 V</i> table..... | 16 |

| | |
|--|----|
| • Added <i>Shutdown Function</i> section | 25 |
|--|----|

| Changes from Revision B (October 2017) to Revision C | Page |
|--|-------------|
| • Changed device status from Production Data/Mixed Status to Production Data | 1 |
| • Deleted package preview note from TLV9061 DPW (X2SON) package in <i>Device Information</i> table | 1 |
| • Deleted package preview note from TLV9061 DPW (X2SON) package pinout drawing | 6 |
| • Changed formatting of <i>ESD Ratings</i> table to show different results for all packages | 12 |
| • Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table | 13 |
| • Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table | 13 |

| Changes from Revision A (June 2017) to Revision B | Page |
|---|-------------|
| • Added 8-pin PW package to <i>Pin Configuration and Functions</i> section | 7 |
| • Added DSG (WSON) package to <i>Thermal Information</i> table | 13 |
| • Added PW (TSSOP) to TLV9062 <i>Thermal Information</i> table | 13 |
| • Changed maximum input offset voltage value from ± 1.6 mV to 2 mV | 15 |
| • Changed maximum input offset voltage value from ± 1.5 to ± 1.6 mV..... | 15 |
| • Changed minimum common-mode rejection ratio input voltage range from 86 dB to 80 dB | 15 |
| • Changed typical input current noise density value from 10 to 23 fA/ $\sqrt{\text{Hz}}$ | 15 |
| • Changed THD + N test conditions from $V_S = 5$ V to $V_S = 5.5$ V..... | 15 |
| • Added $V_{CM} = 2.5$ V test condition to THD + N parameter in <i>Electrical Characteristics</i> table | 15 |
| • Added maximum output voltage swing value from 25 mV to 60 mV..... | 15 |
| • Changed maximum output voltage swing value from 15 mV to 20 mV | 15 |

| Changes from Original (March 2017) to Revision A | Page |
|---|-------------|
| • Changed device status from Advance Information to Production Data | 1 |

5 Description (continued)

The TLV906xS devices include a shutdown mode that allow the amplifiers to switch into standby mode with typical current consumption less than 1 μ A.

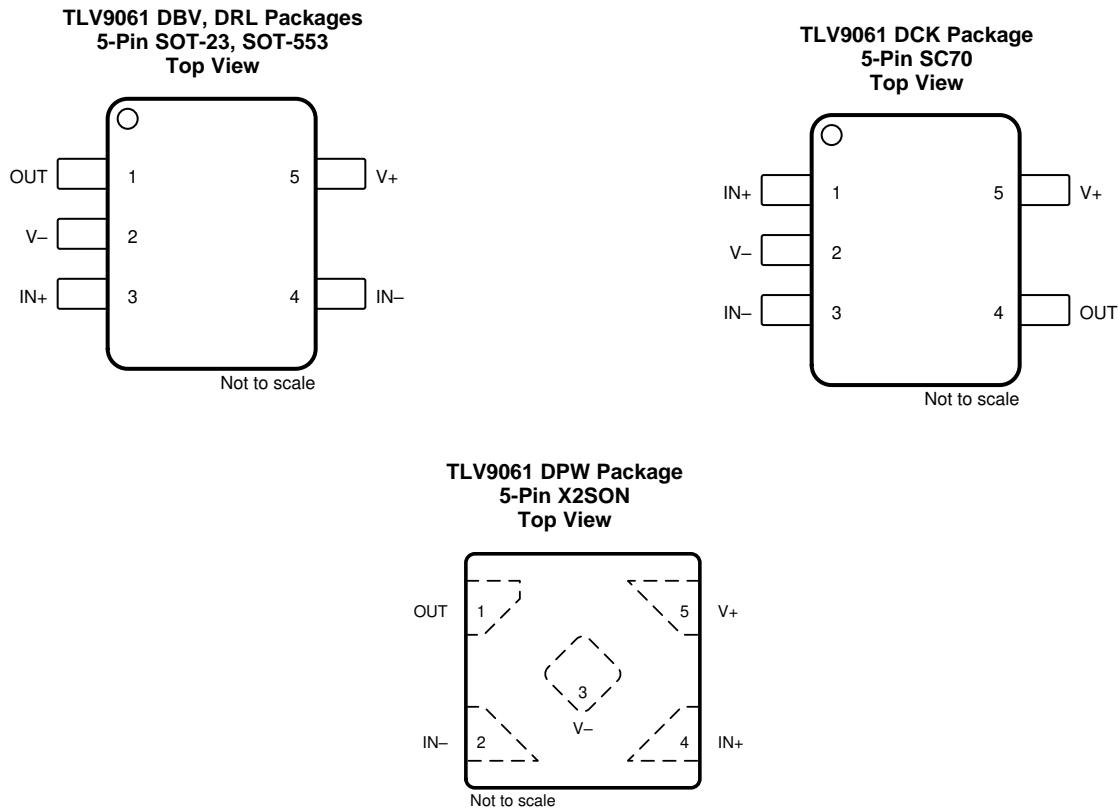
The TLV906xS family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

Micro size packages, such as X2SON and X2QFN, are offered for all the channel variants (single, dual and quad), along with industry-standard packages, such as SOIC, MSOP, SOT-23, and TSSOP.

6 Device Comparison Table

| DEVICE | NO. OF CHANNELS | PACKAGE LEADS | | | | | | | | | | | | |
|----------|-----------------|---------------|------------|-----------|-----------|-----------|-----------|-------------|----------|----------|------------|----------|-----------|-----------|
| | | SOIC D | SOT-23 DBV | SC-70 DCK | VSSOP DGK | VSSOP DGS | X2SON DPW | SOT-553 DRL | WSON DSG | TSSOP PW | SOT-23 DDF | WQFN RTE | X2QFN RUC | X2QFN RUG |
| TLV9061 | 1 | 8 | 5 | 5 | — | — | 5 | 5 | — | — | — | — | — | — |
| TLV9061S | | — | 6 | — | — | — | — | — | — | — | — | — | — | — |
| TLV9062 | 2 | 8 | — | — | 8 | 10 | — | — | 8 | 8 | 8 | — | — | — |
| TLV9062S | | — | — | — | — | 10 | — | — | — | — | — | — | — | 10 |
| TLV9064 | 4 | 14 | — | — | — | — | — | — | — | 14 | — | 16 | 14 | — |
| TLV9064S | | — | — | — | — | — | — | — | — | — | — | 16 | — | — |

7 Pin Configuration and Functions



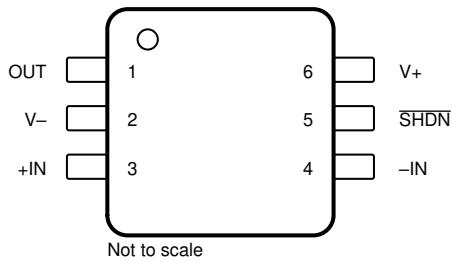
Pin Functions: TLV9061

| PIN | | | | I/O | DESCRIPTION |
|------|--------------------|------|-------|--------|---|
| NAME | SOT-23, SOT-553 | SC70 | X2SON | | |
| IN- | 4 | 3 | 2 | I | Inverting input |
| IN+ | 3 | 1 | 4 | I | Noninverting input |
| OUT | 1 | 4 | 1 | O | Output |
| V- | 2 | 2 | 3 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 5 | 5 | 5 | I | Positive (high) supply |

TLV9061S DBV Package

6-Pin SOT-23

Top View

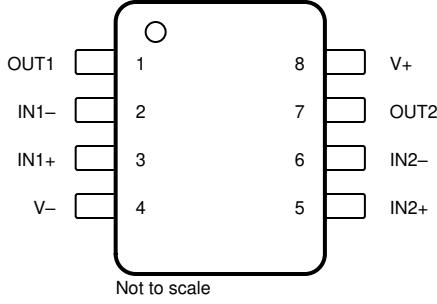

Pin Functions: TLV9061S

| PIN | | I/O | DESCRIPTION |
|-------------|------------|------------|---|
| NAME | NO. | | |
| IN- | 4 | I | Inverting input |
| IN+ | 3 | I | Noninverting input |
| OUT | 1 | O | Output |
| SHDN | 5 | I | Shutdown: low = amp disabled, high = amp enabled. See Shutdown Function section for more information. |
| V- | 2 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 6 | I | Positive (high) supply |

TLV9062 D, DGK, PW, DDF Packages

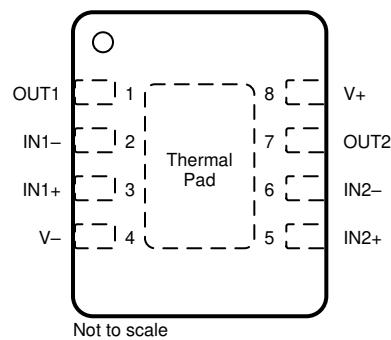
8-Pin SOIC, VSSOP, TSSOP, SOT-23

Top View


TLV9062 DSG Package

8-Pin WSON With Exposed Thermal Pad

Top View

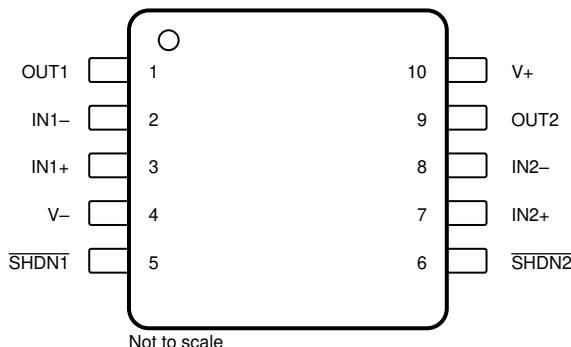


(1) Connect thermal pad to V-

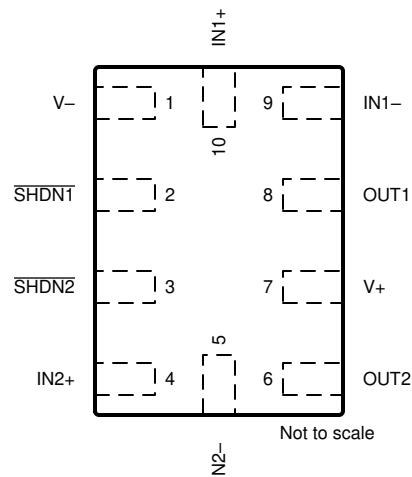
Pin Functions: TLV9062

| PIN | | I/O | DESCRIPTION |
|-------------|------------|------------|--|
| NAME | NO. | | |
| IN1- | 2 | I | Inverting input, channel 1 |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN2- | 6 | I | Inverting input, channel 2 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| V- | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 8 | — | Positive (highest) supply |

**TLV9062S DGS Package
10-Pin VSSOP
Top View**

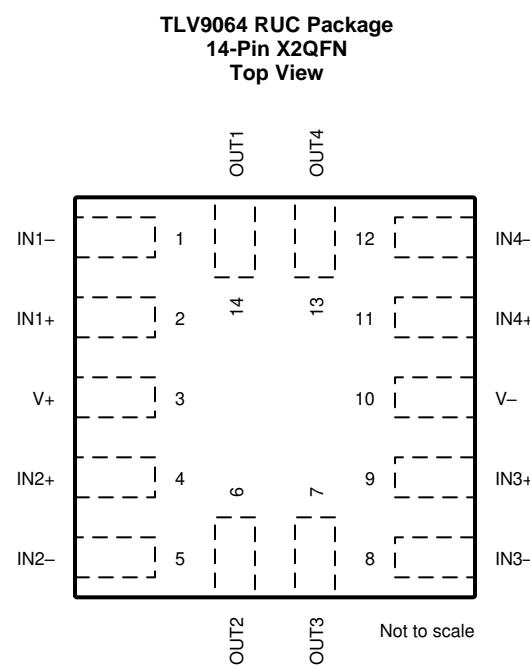
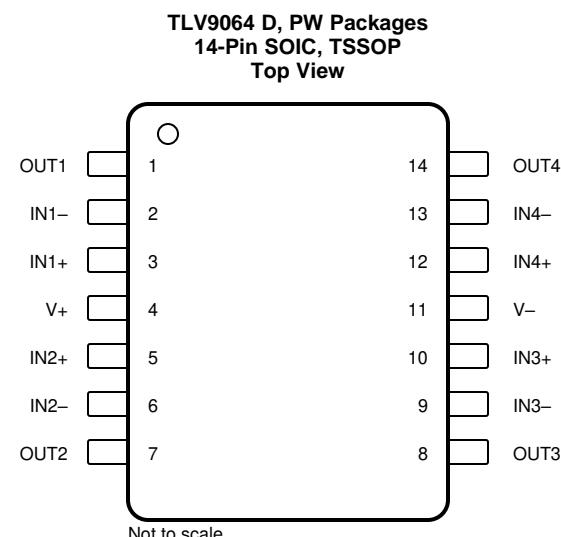


**TLV9062S RUG Package
10-Pin X2QFN
Top View**

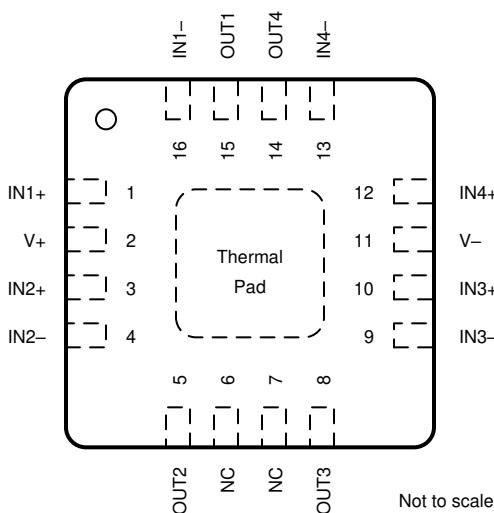


Pin Functions: TLV9062S

| PIN | | | I/O | DESCRIPTION |
|-------|-------|-------|--------|--|
| NAME | VSSOP | X2QFN | | |
| IN1– | 2 | 9 | I | Inverting input, channel 1 |
| IN1+ | 3 | 10 | I | Noninverting input, channel 1 |
| IN2– | 8 | 5 | I | Inverting input, channel 2 |
| IN2+ | 7 | 4 | I | Noninverting input, channel 2 |
| OUT1 | 1 | 8 | O | Output, channel 1 |
| OUT2 | 9 | 6 | O | Output, channel 2 |
| SHDN1 | 5 | 2 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information. |
| SHDN2 | 6 | 3 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 2. See Shutdown Function section for more information. |
| V– | 4 | 1 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 10 | 7 | I | Positive (high) supply |



TLV9064 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



(1) Connect thermal pad to V-

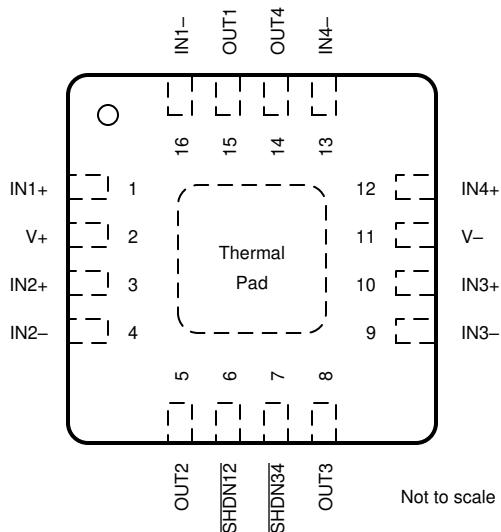
Pin Functions: TLV9064

| NAME | PIN | | | I/O | DESCRIPTION |
|------|----------------|------|-------|-----|-------------------------------|
| | SOIC, TSSOP | WQFN | X2QFN | | |
| IN1– | 2 | 16 | 1 | I | Inverting input, channel 1 |
| IN1+ | 3 | 1 | 2 | I | Noninverting input, channel 1 |
| IN2– | 6 | 4 | 5 | I | Inverting input, channel 2 |
| IN2+ | 5 | 3 | 4 | I | Noninverting input, channel 2 |
| IN3– | 9 | 9 | 8 | I | Inverting input, channel 3 |
| IN3+ | 10 | 10 | 9 | I | Noninverting input, channel 3 |
| IN4– | 13 | 13 | 12 | I | Inverting input, channel 4 |
| IN4+ | 12 | 12 | 11 | I | Noninverting input, channel 4 |

Pin Functions: TLV9064 (continued)

| PIN | | | | I/O | DESCRIPTION |
|----------------|----------------|------|-------|--------|---|
| NAME | SOIC, TSSOP | WQFN | X2QFN | | |
| NC | — | 6, 7 | — | — | No internal connection |
| OUT1 | 1 | 15 | 14 | O | Output, channel 1 |
| OUT2 | 7 | 5 | 6 | O | Output, channel 2 |
| OUT3 | 8 | 8 | 7 | O | Output, channel 3 |
| OUT4 | 14 | 14 | 13 | O | Output, channel 4 |
| V ⁻ | 11 | 11 | 10 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V ⁺ | 4 | 2 | 3 | I | Positive (high) supply |

TLV9064S RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



(1) Connect thermal pad to V–

Pin Functions: TLV9064S

| PIN | | I/O | DESCRIPTION |
|--------|-----|--------|--|
| NAME | NO. | | |
| IN1– | 16 | I | Inverting input, channel 1 |
| IN1+ | 1 | I | Noninverting input, channel 1 |
| IN2– | 4 | I | Inverting input, channel 2 |
| IN2+ | 3 | I | Noninverting input, channel 2 |
| IN3– | 9 | I | Inverting input, channel 3 |
| IN3+ | 10 | I | Noninverting input, channel 3 |
| IN4– | 13 | I | Inverting input, channel 4 |
| IN4+ | 12 | I | Noninverting input, channel 4 |
| OUT1 | 15 | O | Output, channel 1 |
| OUT2 | 5 | O | Output, channel 2 |
| OUT3 | 8 | O | Output, channel 3 |
| OUT4 | 14 | O | Output, channel 4 |
| SHDN12 | 6 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information. |
| SHDN34 | 7 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information. |
| V– | 11 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 2 | I | Positive (high) supply |

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT | |
|-------------------------------------|---------------------------|--------------|-------------------|------------|-------------|--|
| Supply voltage [(V+) – (V–)] | | | 0 | 6 | V | |
| Signal input pins | Voltage ⁽²⁾ | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V | |
| | | Differential | (V+) – (V–) + 0.2 | | V | |
| | Current ⁽²⁾ | | –10 | 10 | mA | |
| Output short-circuit ⁽³⁾ | | | Continuous | | mA | |
| Temperature | Specified, T _A | | –40 | 125 | °C | |
| | Junction, T _J | | 150 | | | |
| | Storage, T _{stg} | | –65 | 150 | | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

8.2 ESD Ratings

| | | | VALUE | UNIT |
|---------------------------|-------------------------|--|--------------|-------------|
| TLV9061 PACKAGES | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |
| ALL OTHER PACKAGES | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|----------------------|--|--|------------|------------|-------------|
| V _S | Supply voltage (V _S = [V+] – [V–]) | | 1.8 | 5.5 | V |
| V _I | Input voltage range | | (V–) – 0.1 | (V+) + 0.1 | V |
| V _O | Output voltage range | | V– | V+ | V |
| V _{SHDN_IH} | High level input voltage at shutdown pin (amplifier enabled) | | 1.1 | V+ | V |
| V _{SHDN_IL} | Low level input voltage at shutdown pin (amplifier disabled) | | V– | 0.2 | V |
| T _A | Specified temperature | | –40 | 125 | °C |

8.4 Thermal Information: TLV9061

| THERMAL METRIC ⁽¹⁾ | | TLV9061 | | | UNIT |
|-------------------------------|--|--------------|------------|-------------|------|
| | | DBV (SOT-23) | DCK (SC70) | DPW (X2SON) | |
| | | 5 PINS | 5 PINS | 5 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 221.7 | 263.3 | 467 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 144.7 | 75.5 | 211.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 49.7 | 51 | 332.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 26.1 | 1 | 29.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 49 | 50.3 | 330.6 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 125 | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.5 Thermal Information: TLV9061S

| THERMAL METRIC ⁽¹⁾ | | TLV9061S | | UNIT |
|-------------------------------|--|--------------|--------|------|
| | | DBV (SOT-23) | 6 PINS | |
| | | 5 PINS | 5 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 216.5 | °C/W | |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 155.1 | °C/W | |
| R _{θJB} | Junction-to-board thermal resistance | 96.2 | °C/W | |
| Ψ _{JT} | Junction-to-top characterization parameter | 80.3 | °C/W | |
| Ψ _{JB} | Junction-to-board characterization parameter | 95.9 | °C/W | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | °C/W | |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.6 Thermal Information: TLV9062

| THERMAL METRIC ⁽¹⁾ | TLV9062 | | | | | UNIT | |
|-------------------------------|--|-------------|------------|------------|--------------|-------|------|
| | D (SOIC) | DGK (VSSOP) | DSG (WSON) | PW (TSSOP) | DDF (SOT-23) | | |
| | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 8 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 157.6 | 201.2 | 94.4 | 205.8 | 184.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 104.6 | 85.7 | 116.5 | 106.7 | 112.8 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 99.7 | 122.9 | 61.3 | 133.9 | 99.9 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 55.6 | 21.2 | 13 | 34.4 | 18.7 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 99.2 | 121.4 | 61.7 | 132.6 | 99.3 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 34.4 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.7 Thermal Information: TLV9062S

| THERMAL METRIC ⁽¹⁾ | TLV9062S | | | UNIT |
|-------------------------------|--|---------|-------------|------|
| | DGS (VSSOP) | | RUG (X2QFN) | |
| | 10 PINS | 10 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 170.4 | 197.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 84.9 | 93.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 113.5 | 123.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 16.4 | 3.7 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 112.3 | 120.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.8 Thermal Information: TLV9064

| THERMAL METRIC ⁽¹⁾ | TLV9064 | | | | UNIT | |
|-------------------------------|--|----------|------------|-------------|-------|------|
| | PW (TSSOP) | D (SOIC) | RTE (WQFN) | RUC (X2QFN) | | |
| | 14 PINS | 14 PINS | 16 PINS | 14 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 135.8 | 106.9 | 65.1 | 205.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 64 | 64 | 67.9 | 72.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 79 | 63 | 40.4 | 150.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 15.7 | 25.9 | 5.5 | 3.0 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 78.4 | 62.7 | 40.2 | 149.6 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 23.8 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.9 Thermal Information: TLV9064S

| THERMAL METRIC ⁽¹⁾ | TLV9064S | | UNIT | |
|-------------------------------|--|------|------|--|
| | RTE (WQFN) | | | |
| | 16 PINS | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 65.1 | °C/W | |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 67.9 | °C/W | |
| R _{θJB} | Junction-to-board thermal resistance | 40.4 | °C/W | |
| Ψ _{JT} | Junction-to-top characterization parameter | 5.5 | °C/W | |
| Ψ _{JB} | Junction-to-board characterization parameter | 40.2 | °C/W | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 23.8 | °C/W | |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

8.10 Electrical Characteristics

For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8 \text{ V}$ to 5.5 V at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-------|--------------|--------------|------------------------------|
| OFFSET VOLTAGE | | | | | |
| V_{OS} Input offset voltage | $V_S = 5 \text{ V}$ | | ± 0.3 | ± 1.6 | mV |
| | $V_S = 5 \text{ V}, T_A = -40^\circ\text{C}$ to 125°C | | | ± 2 | |
| dV_{OS}/dT Drift | $V_S = 5 \text{ V}, T_A = -40^\circ\text{C}$ to 125°C | | ± 0.53 | | $\mu\text{V}/^\circ\text{C}$ |
| PSRR Power-supply rejection ratio | $V_S = 1.8 \text{ V}$ to 5.5 V , $V_{CM} = (V-)$ | | ± 7 | ± 80 | $\mu\text{V}/\text{V}$ |
| | Channel separation, DC | At DC | | 100 | dB |
| INPUT VOLTAGE RANGE | | | | | |
| V_{CM} Common-mode voltage range | $V_S = 1.8 \text{ V}$ to 5.5 V | | $(V-) - 0.1$ | $(V+) + 0.1$ | V |
| | $V_S = 5.5 \text{ V}, (V-) - 0.1 \text{ V} < V_{CM} < (V+) - 1.4 \text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C | 80 | 103 | | dB |
| | $V_S = 5.5 \text{ V}, V_{CM} = -0.1 \text{ V}$ to 5.6 V , $T_A = -40^\circ\text{C}$ to 125°C | 57 | 87 | | |
| | $V_S = 1.8 \text{ V}, (V-) - 0.1 \text{ V} < V_{CM} < (V+) - 1.4 \text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C | | 88 | | |
| | $V_S = 1.8 \text{ V}, V_{CM} = -0.1 \text{ V}$ to 1.9 V , $T_A = -40^\circ\text{C}$ to 125°C | | 81 | | |
| INPUT BIAS CURRENT | | | | | |
| I_B Input bias current | | | ± 0.5 | | pA |
| I_{OS} Input offset current | | | ± 0.05 | | pA |
| NOISE | | | | | |
| E_n Input voltage noise (peak-to-peak) | $V_S = 5 \text{ V}, f = 0.1 \text{ Hz}$ to 10 Hz | | 4.77 | | μV_{PP} |
| e_n Input voltage noise density | $V_S = 5 \text{ V}, f = 10 \text{ kHz}$ | | 10 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | $V_S = 5 \text{ V}, f = 1 \text{ kHz}$ | | 16 | | |
| i_n Input current noise density | $f = 1 \text{ kHz}$ | | 23 | | $\text{fA}/\sqrt{\text{Hz}}$ |
| INPUT CAPACITANCE | | | | | |
| C_{ID} Differential | | | 2 | | pF |
| C_{IC} Common-mode | | | 4 | | pF |
| OPEN-LOOP GAIN | | | | | |
| A_{OL} Open-loop voltage gain | $V_S = 1.8 \text{ V}, (V-) + 0.04 \text{ V} < V_O < (V+) - 0.04 \text{ V}$, $R_L = 10 \text{ k}\Omega$ | | 100 | | dB |
| | $V_S = 5.5 \text{ V}, (V-) + 0.05 \text{ V} < V_O < (V+) - 0.05 \text{ V}$, $R_L = 10 \text{ k}\Omega$ | 104 | 130 | | |
| | $V_S = 1.8 \text{ V}, (V-) + 0.06 \text{ V} < V_O < (V+) - 0.06 \text{ V}$, $R_L = 2 \text{ k}\Omega$ | | 100 | | |
| | $V_S = 5.5 \text{ V}, (V-) + 0.15 \text{ V} < V_O < (V+) - 0.15 \text{ V}$, $R_L = 2 \text{ k}\Omega$ | | 130 | | |
| FREQUENCY RESPONSE | | | | | |
| GBP Gain bandwidth product | $V_S = 5 \text{ V}, G = +1$ | | 10 | | MHz |
| ϕ_m Phase margin | $V_S = 5 \text{ V}, G = +1$ | | 55 | | ° |
| SR Slew rate | $V_S = 5 \text{ V}, G = +1$ | | 6.5 | | $\text{V}/\mu\text{s}$ |
| t_s Settling time | To 0.1%, $V_S = 5 \text{ V}$, 2-V step, $G = +1$, $C_L = 100 \text{ pF}$ | | 0.5 | | μs |
| | To 0.01%, $V_S = 5 \text{ V}$, 2-V step, $G = +1$, $C_L = 100 \text{ pF}$ | | 1 | | |
| t_{OR} Overload recovery time | $V_S = 5 \text{ V}, V_{IN} \times \text{gain} > V_S$ | | 0.2 | | μs |
| THD + N Total harmonic distortion + noise ⁽¹⁾ | $V_S = 5.5 \text{ V}, V_{CM} = 2.5 \text{ V}, V_O = 1 \text{ V}_{RMS}, G = +1$, $f = 1 \text{ kHz}$ | | 0.0008% | | |
| OUTPUT | | | | | |
| V_O Voltage output swing from supply rails | $V_S = 5.5 \text{ V}, R_L = 10 \text{ k}\Omega$ | | 20 | | mV |
| | $V_S = 5.5 \text{ V}, R_L = 2 \text{ k}\Omega$ | | 60 | | |
| I_{SC} Short-circuit current | $V_S = 5 \text{ V}$ | | ± 50 | | mA |
| Z_O Open-loop output impedance | $V_S = 5 \text{ V}, f = 10 \text{ MHz}$ | | 100 | | Ω |

(1) Third-order filter; bandwidth = 80 kHz at -3 dB .

Electrical Characteristics (continued)

For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8 \text{ V to } 5.5 \text{ V}$ at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-----|------------------------|------------------------|--------------------------------------|
| POWER SUPPLY | | | | | | |
| I_Q | Quiescent current per amplifier | $V_S = 5.5 \text{ V}, I_O = 0 \text{ mA}$ | | 538 | 750 | μA |
| | | $V_S = 5.5 \text{ V}, I_O = 0 \text{ mA}, T_A = -40^\circ\text{C to } 125^\circ\text{C}$ | | | 800 | |
| SHUTDOWN | | | | | | |
| I_{QSD} | Quiescent current per amplifier | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, all amplifiers disabled, $\overline{SHDN} = \text{Low}$ | | 0.5 | 1.5 | μA |
| Z_{SHDN} | Output impedance during shutdown | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, amplifier disabled | | 10 \parallel 8 | | $\text{G}\Omega \parallel \text{pF}$ |
| $V_{SHDN_THR_HI}$ | High level voltage shutdown threshold (amplifier enabled) | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$ | | $(V-) + 0.9 \text{ V}$ | $(V-) + 1.1 \text{ V}$ | V |
| $V_{SDHN_THR_LO}$ | Low level voltage shutdown threshold (amplifier disabled) | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$ | | $(V-) + 0.2 \text{ V}$ | $(V-) + 0.7 \text{ V}$ | V |
| t_{ON} | Amplifier enable time (shutdown) ⁽²⁾ | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, full shutdown; $G = 1$, $V_{OUT} = 0.9 \times V_S / 2$, R_L connected to $V-$ | | 10 | | μs |
| t_{OFF} | Amplifier disable time ⁽²⁾ | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, $G = 1$, $V_{OUT} = 0.1 \times V_S / 2$, R_L connected to $V-$ | | 0.6 | | μs |
| \overline{SHDN} pin input bias current (per pin) | | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, $V+ \geq \overline{SHDN} \geq (V+) - 0.8 \text{ V}$ | | 130 | | pA |
| | | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, $V- \leq \overline{SHDN} \leq V- + 0.8 \text{ V}$ | | 40 | | |

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the \overline{SHDN} pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

8.11 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

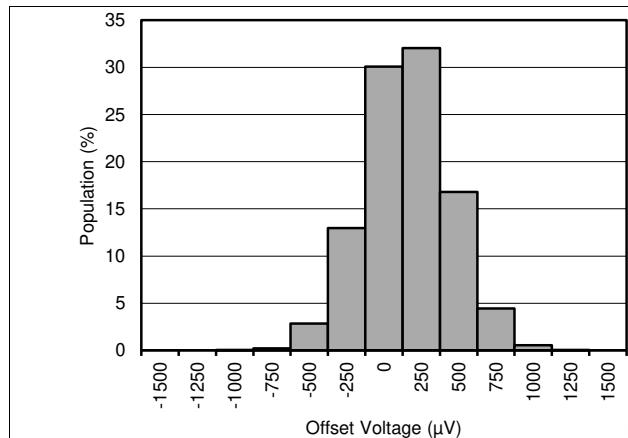
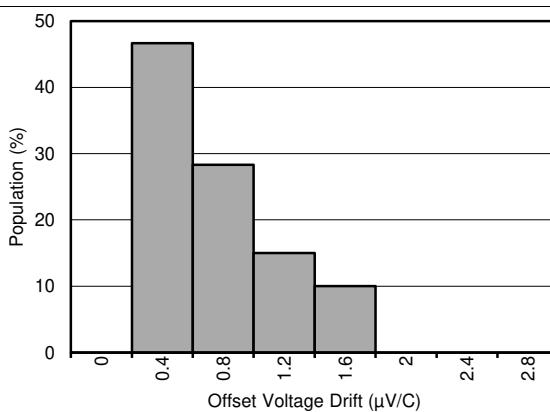


Figure 1. Offset Voltage Production Distribution



$T_A = -40^\circ\text{C}$ to 125°C

Figure 2. Offset Voltage Drift Distribution

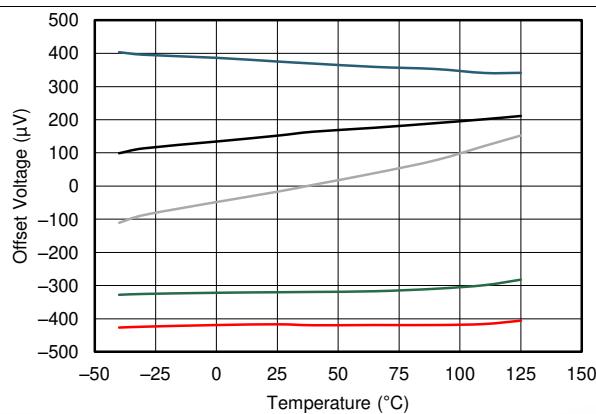


Figure 3. Offset Voltage vs Temperature

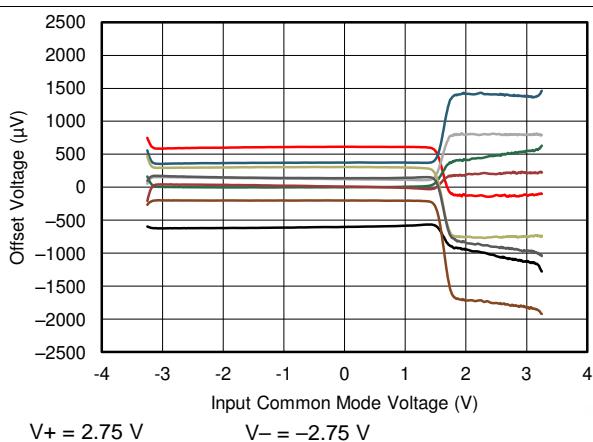


Figure 4. Offset Voltage vs Common-Mode Voltage

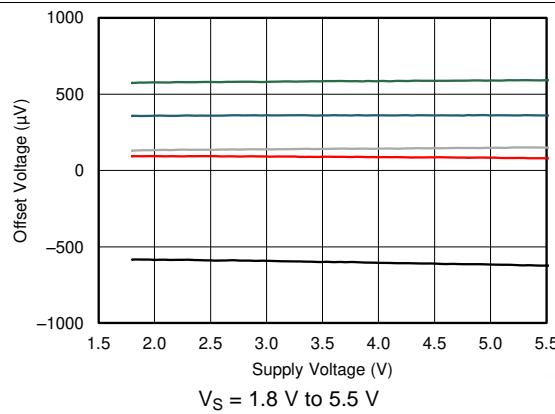


Figure 5. Offset Voltage vs Power Supply

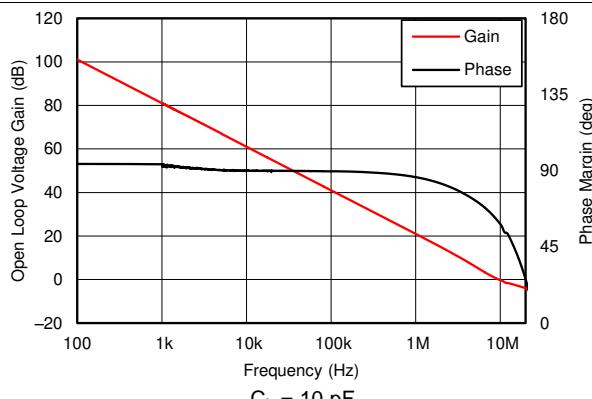


Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

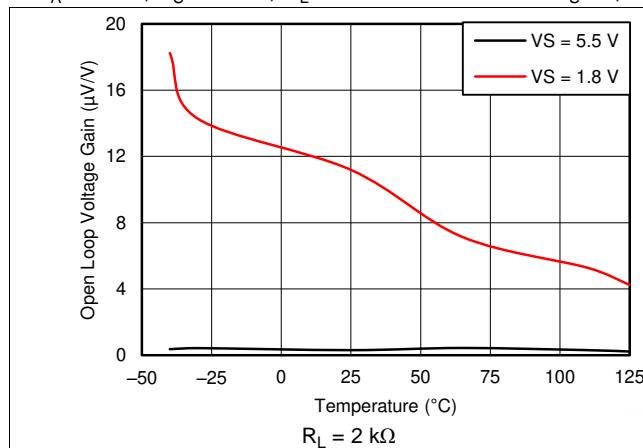


Figure 7. Open-Loop Gain vs Temperature

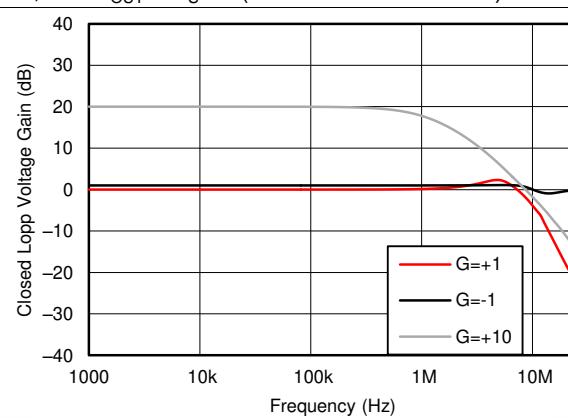


Figure 8. Closed-Loop Gain vs Frequency

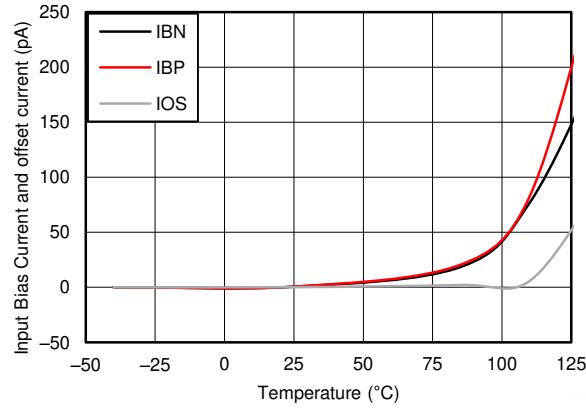


Figure 9. Input Bias Current vs Temperature

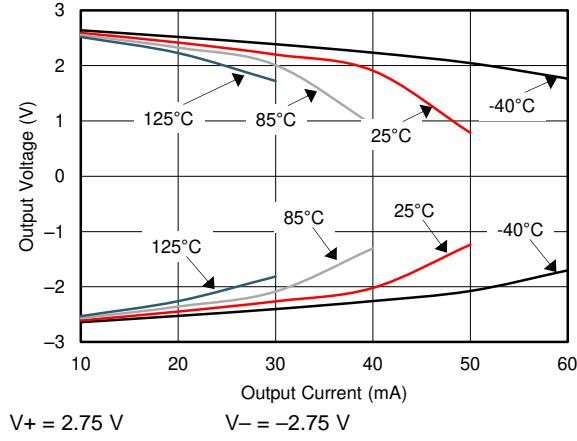


Figure 10. Output Voltage Swing vs Output Current

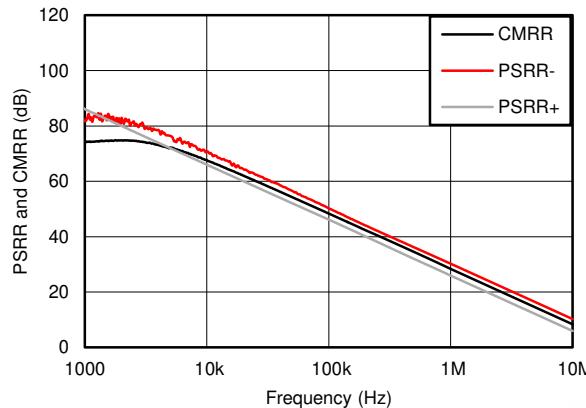
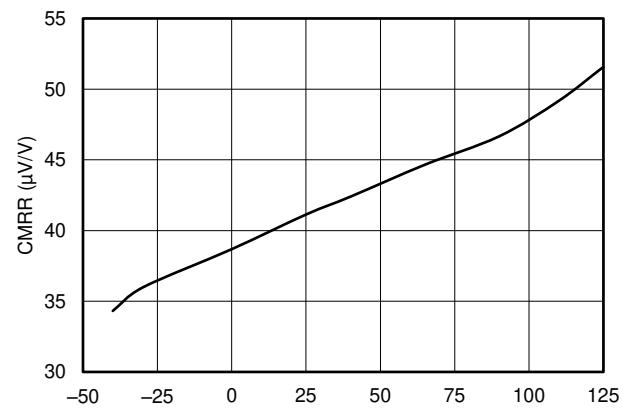


Figure 11. CMRR and PSRR vs Frequency (Referred to Input)

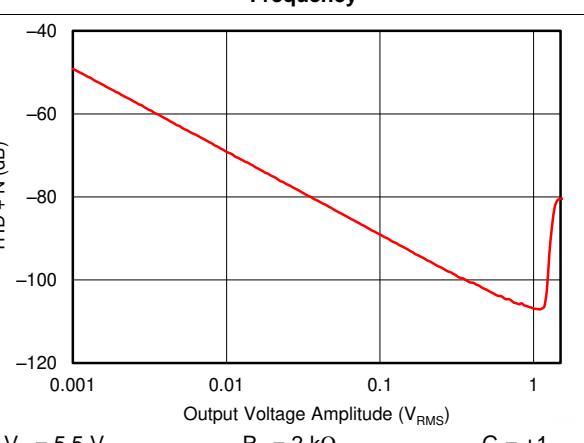
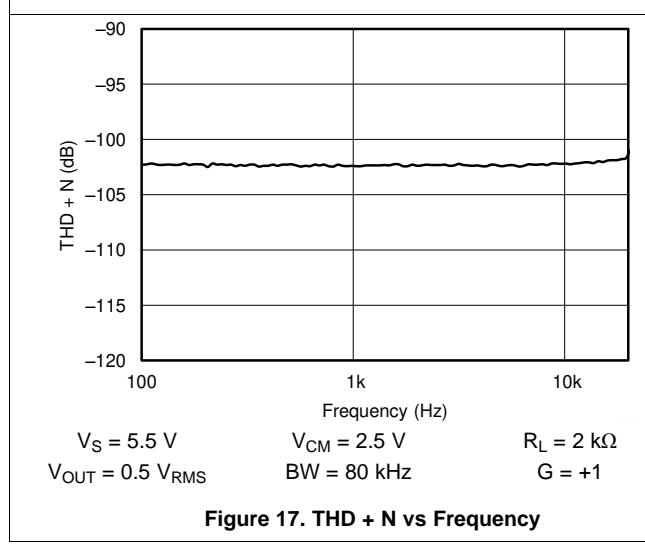
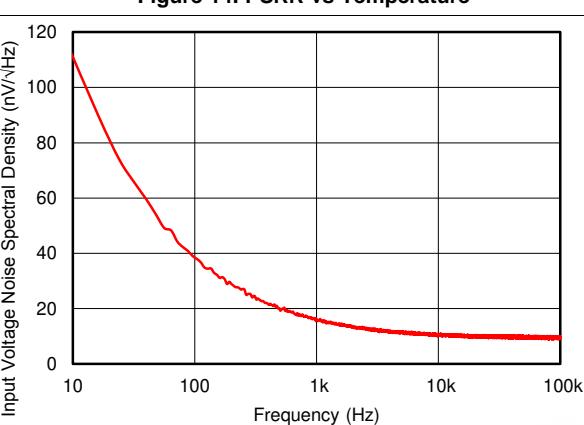
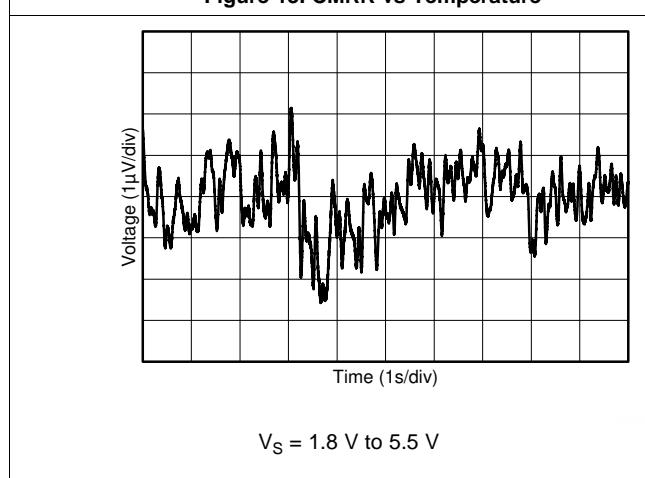
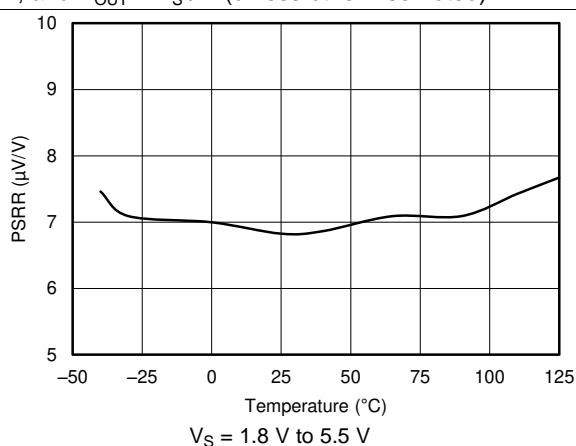
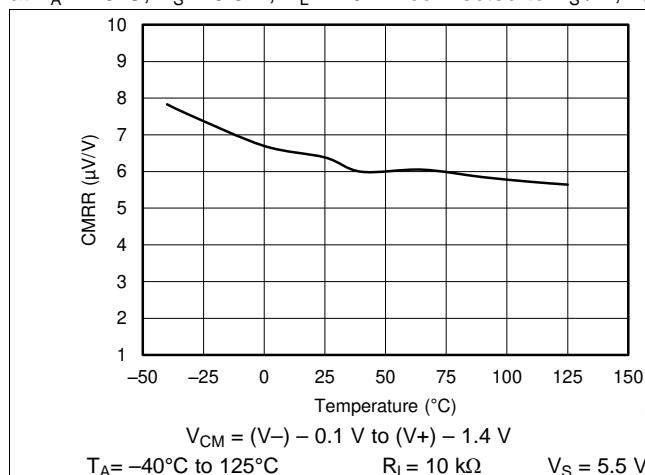


$V_S = 5.5 \text{ V}$ $V_{CM} = -0.1 \text{ V to } 5.6 \text{ V}$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$
 $R_L = 10 \text{ k}\Omega$

Figure 12. CMRR vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

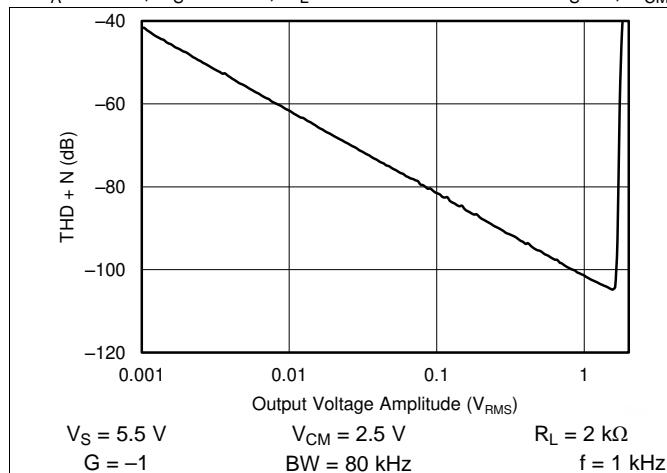


Figure 19. THD + N vs Amplitude

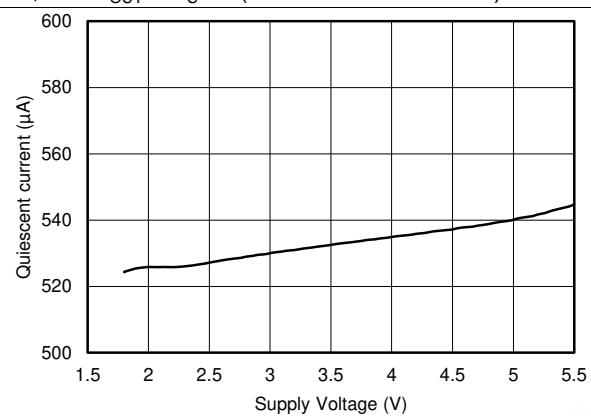


Figure 20. Quiescent Current vs Supply Voltage

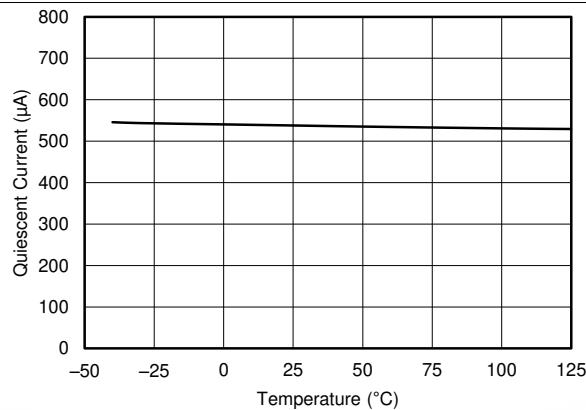


Figure 21. Quiescent Current vs Temperature

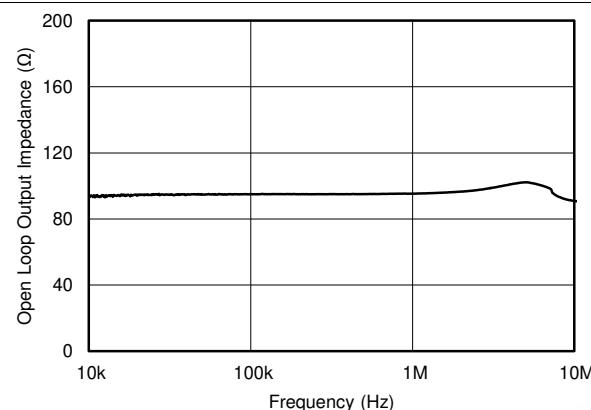


Figure 22. Open-Loop Output Impedance vs Frequency

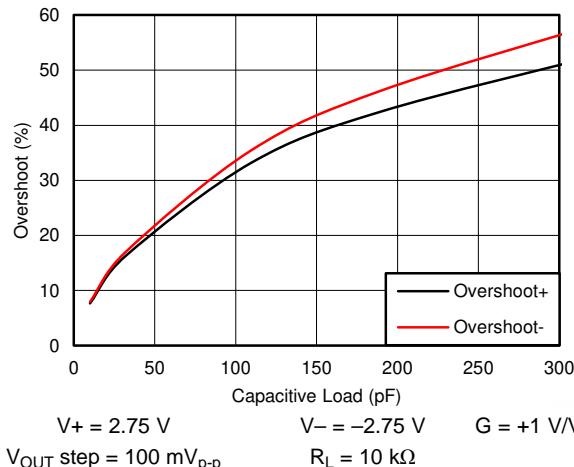


Figure 23. Small-Signal Overshoot vs Load Capacitance

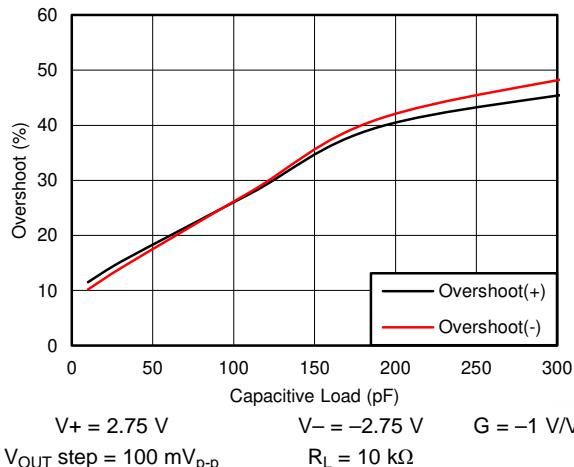
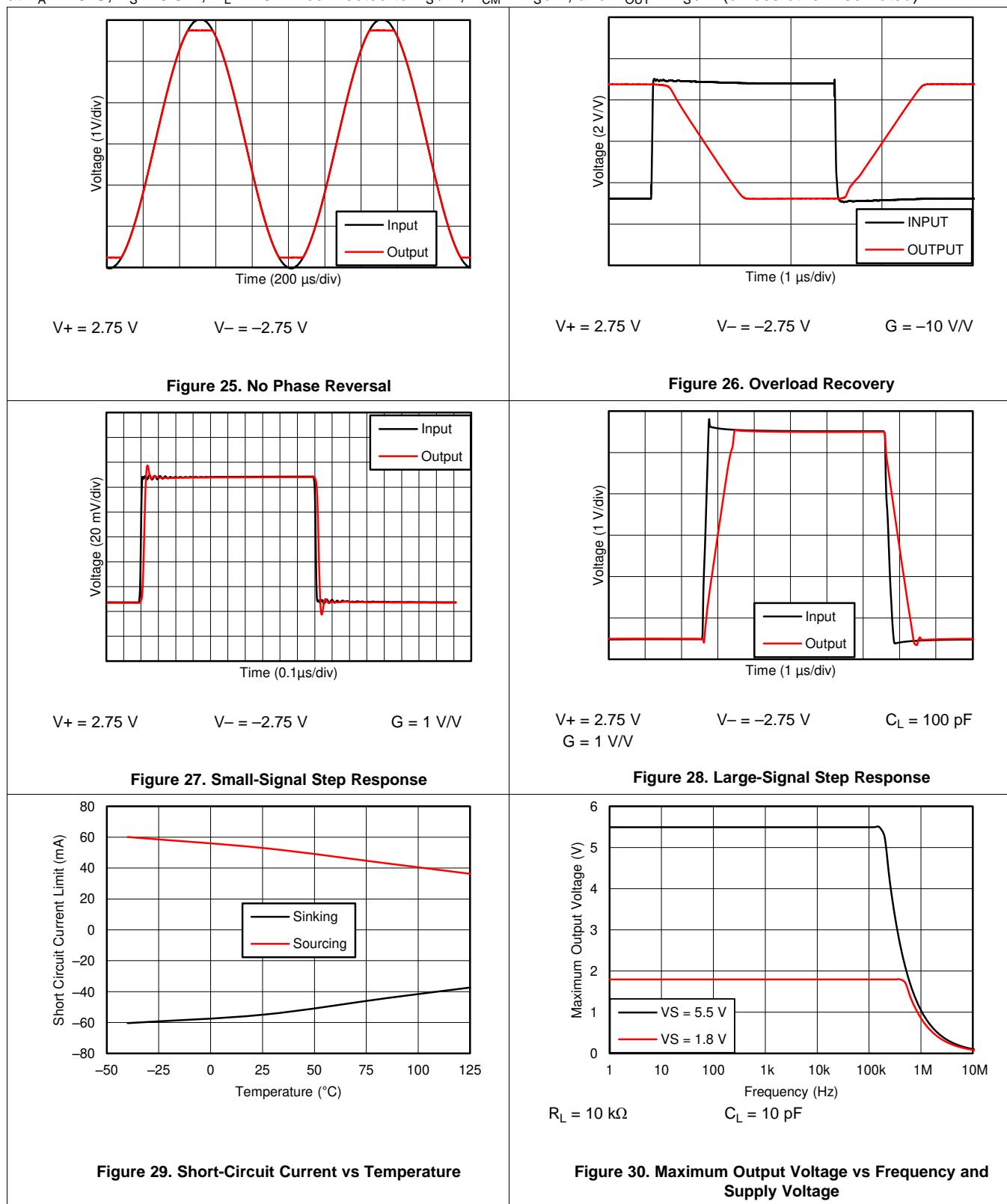


Figure 24. Small-Signal Overshoot vs Load Capacitance

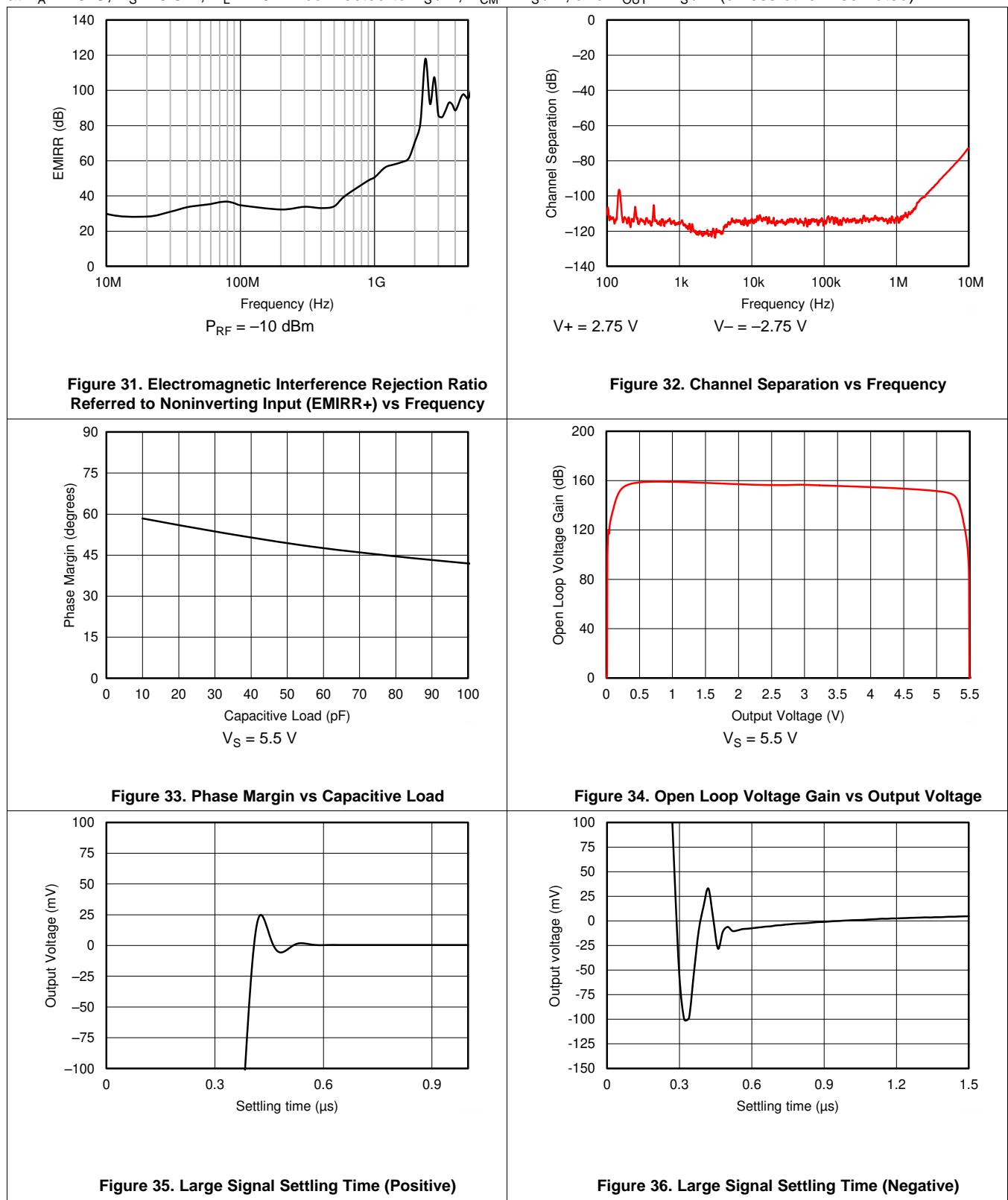
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

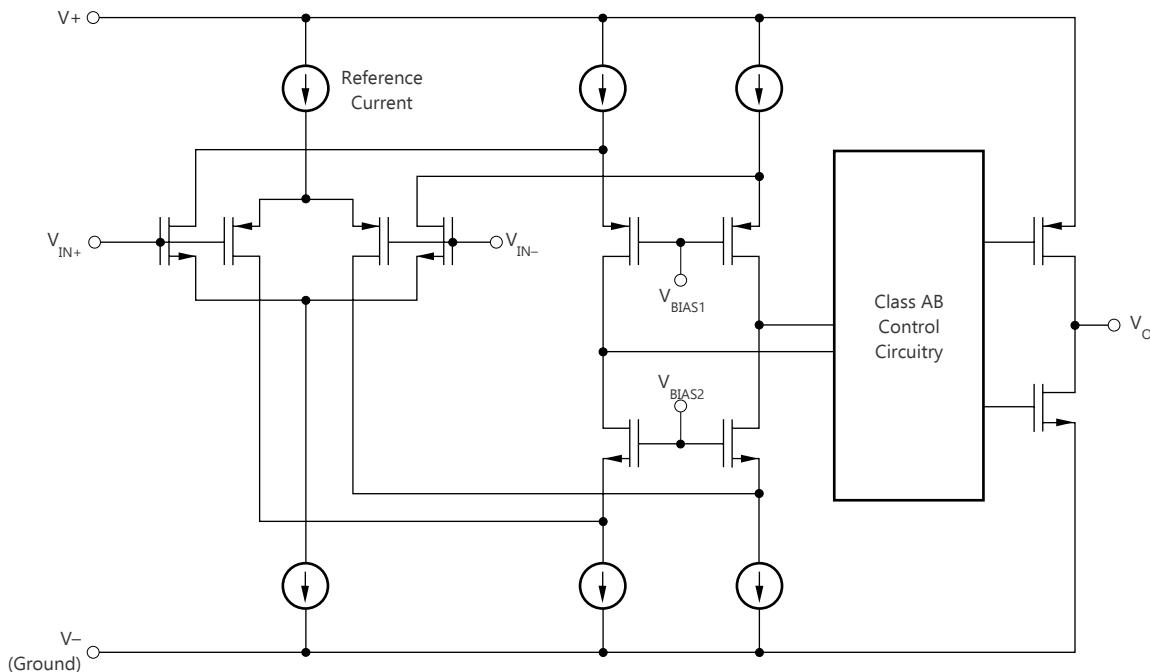


9 Detailed Description

9.1 Overview

The TLV906x devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-hold circuitry of analog-to-digital converters (ADCs).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V_+) - 1.4$ V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately $(V_+) - 1.4$ V. There is a small transition region, typically $(V_+) - 1.2$ V to $(V_+) - 1$ V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from $(V_+) - 1.4$ V to $(V_+) - 1.2$ V on the low end, and up to $(V_+) - 1$ V to $(V_+) - 0.8$ V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

9.3.3 EMI Rejection

The TLV906x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV906x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 37](#) shows the results of this testing on the TLV906x. [Table 1](#) shows the EMIRR IN+ values for the TLV906x at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

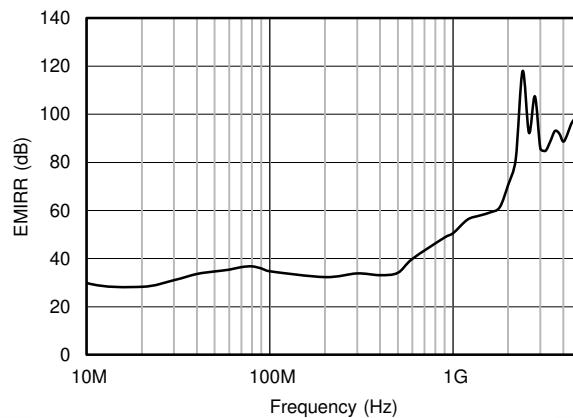


Figure 37. EMIRR Testing

Table 1. TLV906x EMIRR IN+ For Frequencies of Interest

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|-----------|---|-----------|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 59.5 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 68.9 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 77.8 dB |

Feature Description (continued)

Table 1. TLV906x EMIRR IN+ For Frequencies of Interest (continued)

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|-----------|--|-----------|
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 78.0 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 88.8 dB |
| 5 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 87.6 dB |

9.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x family is approximately 200 ns.

9.3.5 Shutdown Function

The TLV906xS devices feature SHDN pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 μ A. The SHDN pins are active-low, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V₋ and V₋ + 0.2 V. A valid logic high is defined as a voltage between V₋ + 1.2 V and V₊. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is **no** internal pull-up to enable the amplifier.

The SHDN pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 μ s for full shutdown of all channels; disable time is 6 μ s. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k Ω load to midsupply (V_S / 2) is required. If using the TLV906xS without a load, the resulting turnoff time is significantly increased.

9.4 Device Functional Modes

The TLV906x family are operational when the power-supply voltage is between 1.8 V (± 0.9 V) and 5.5 V (± 2.75 V). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLV906x family features 10-MHz bandwidth and 6.5-V/ μ s slew rate with only 538 μ A of supply current per channel, providing good AC-performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10 nV/ $\sqrt{\text{Hz}}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

10.2 Typical Applications

10.2.1 Typical Low-Side Current Sense Application

Figure 38 shows the TLV906x configured in a low-side current-sensing application.

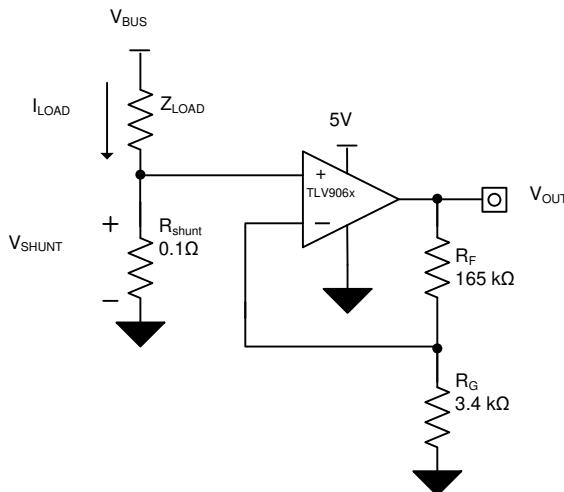


Figure 38. TLV906x in a Low-Side, Current-Sensing Application

10.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 38](#) is given in [Equation 1](#).

$$V_{\text{OUT}} = I_{\text{LOAD}} \times R_{\text{SHUNT}} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{\text{SHUNT}} = \frac{V_{\text{SHUNT_MAX}}}{I_{\text{LOAD_MAX}}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} equals 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x to produce an output voltage of approximately 0 V to 4.95 V. [Equation 3](#) calculates the gain required for the TLV906x to produce the required output voltage.

$$\text{Gain} = \frac{(V_{\text{OUT_MAX}} - V_{\text{OUT_MIN}})}{(V_{\text{IN_MAX}} - V_{\text{IN_MIN}})} \quad (3)$$

Using [Equation 3](#), the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. [Equation 4](#) sizes the R_F and R_G resistors to set the gain of the TLV906x to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165 kΩ and R_G to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. [Figure 39](#) shows the measured transfer function of the circuit shown in [Figure 38](#). Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

10.2.1.3 Application Curve

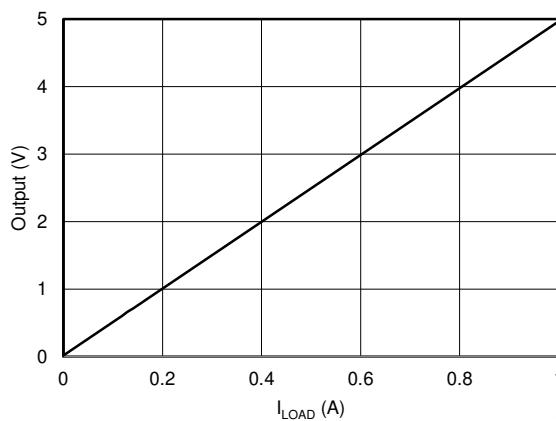


Figure 39. Low-Side, Current-Sense, Transfer Function

11 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V); many specifications apply from -40°C to 125°C . The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the *Absolute Maximum Ratings* table. Figure 40 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

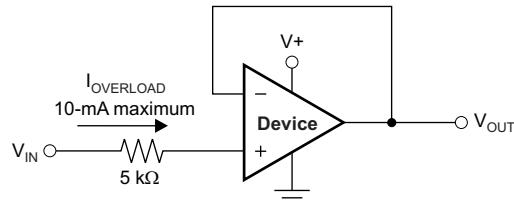


Figure 40. Input Current Protection

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 42](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

12.2 Layout Example

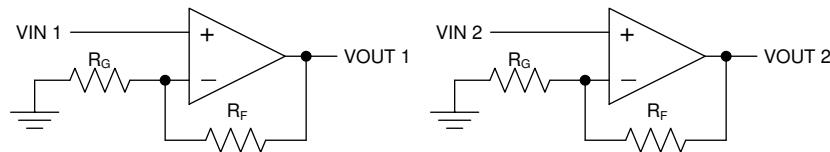


Figure 41. Schematic Representation for Figure 42

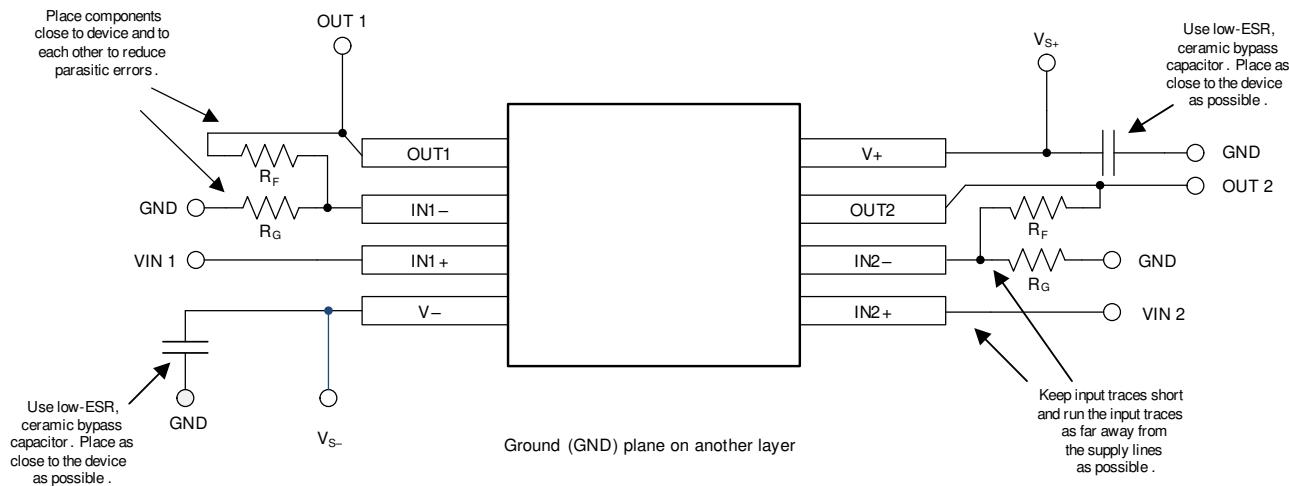


Figure 42. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Texas Instruments, [TLVx313 Low-Power, Rail-to-Rail In/Out, 500- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#)

Texas Instruments, [TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier](#)

Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#)

Texas Instruments, [QFN/SON PCB Attachment](#)

Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#)

Texas Instruments, [Circuit Board Layout Techniques](#)

Texas Instruments, [Single-Ended Input to Differential Output Conversion Circuit Reference Design](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TLV9061 | Click here |
| TLV9062 | Click here |
| TLV9064 | Click here |

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.5 Trademarks

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TLV9061IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | Call TI SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OAF | Samples |
| TLV9061IDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | 1CA | Samples |
| TLV9061IDPWR | ACTIVE | X2SON | DPW | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | CG | Samples |
| TLV9061SIDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF | Samples |
| TLV9062IDDFR | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 | Samples |
| TLV9062IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG SN | Level-2-260C-1 YEAR | -40 to 125 | T062 | Samples |
| TLV9062IDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | NIPDAUAG SN | Level-2-260C-1 YEAR | -40 to 125 | T062 | Samples |
| TLV9062IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU SN | Level-2-260C-1 YEAR | -40 to 125 | TL9062 | Samples |
| TLV9062IDSGR | ACTIVE | WSON | DSG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 | Samples |
| TLV9062IDSGT | ACTIVE | WSON | DSG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 | Samples |
| TLV9062IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU SN | Level-2-260C-1 YEAR | -40 to 125 | TL9062 | Samples |
| TLV9062SIDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1TDX | Samples |
| TLV9062SIRUGR | ACTIVE | X2QFN | RUG | 10 | 3000 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | EOF | Samples |
| TLV9064IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV9064D | Samples |
| TLV9064IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 | Samples |
| TLV9064IPWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 | Samples |
| TLV9064IRTER | ACTIVE | WQFN | RTE | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064 | Samples |
| TLV9064IRUCR | ACTIVE | QFN | RUC | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1DD | Samples |
| TLV9064SIRTER | ACTIVE | WQFN | RTE | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064S | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

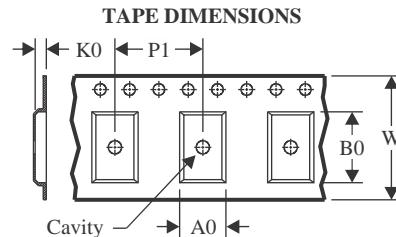
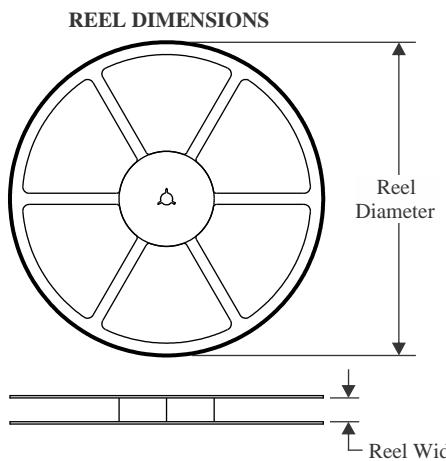
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9061, TLV9062, TLV9064 :

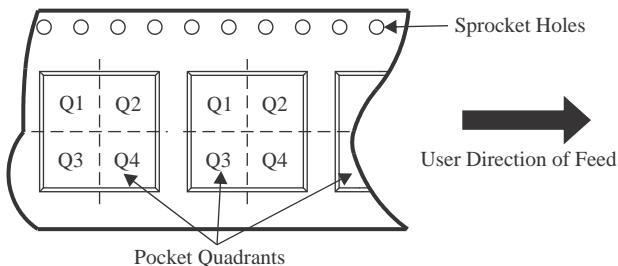
- Automotive : [TLV9061-Q1](#), [TLV9062-Q1](#), [TLV9064-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

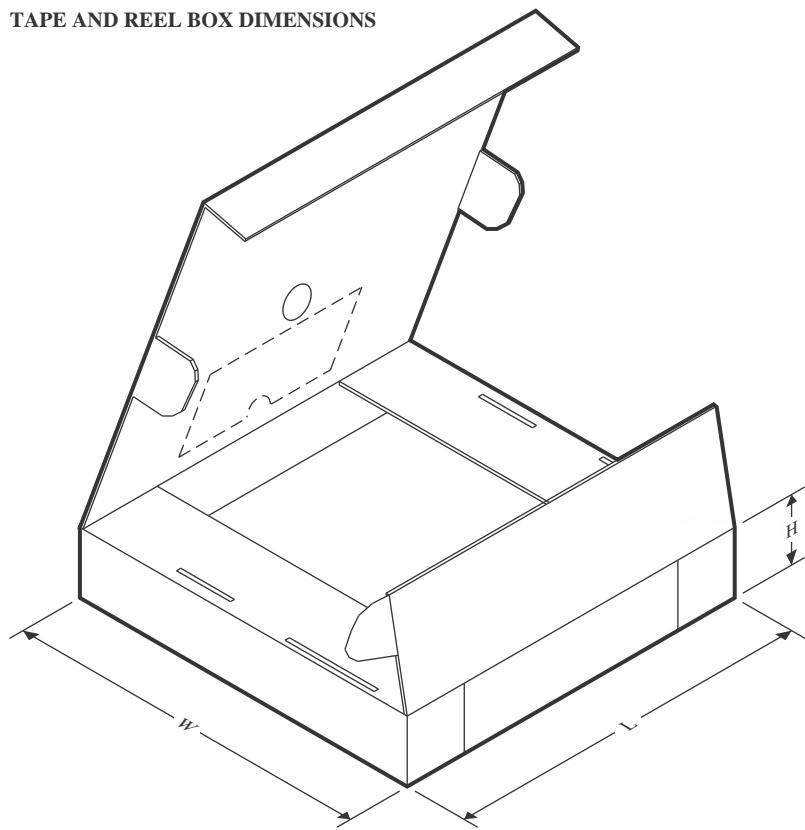
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061IDCCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9061IDPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q2 |
| TLV9061SIDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9062IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9062IDSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV9062SIDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062SIRUGR | X2QFN | RUG | 10 | 3000 | 178.0 | 8.4 | 1.75 | 2.25 | 0.56 | 4.0 | 8.0 | Q1 |
| TLV9064IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV9064IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9064IPWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9064IRTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TLV9064IRUCR | QFN | RUC | 14 | 3000 | 180.0 | 9.5 | 2.16 | 2.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TLV9064SIRTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


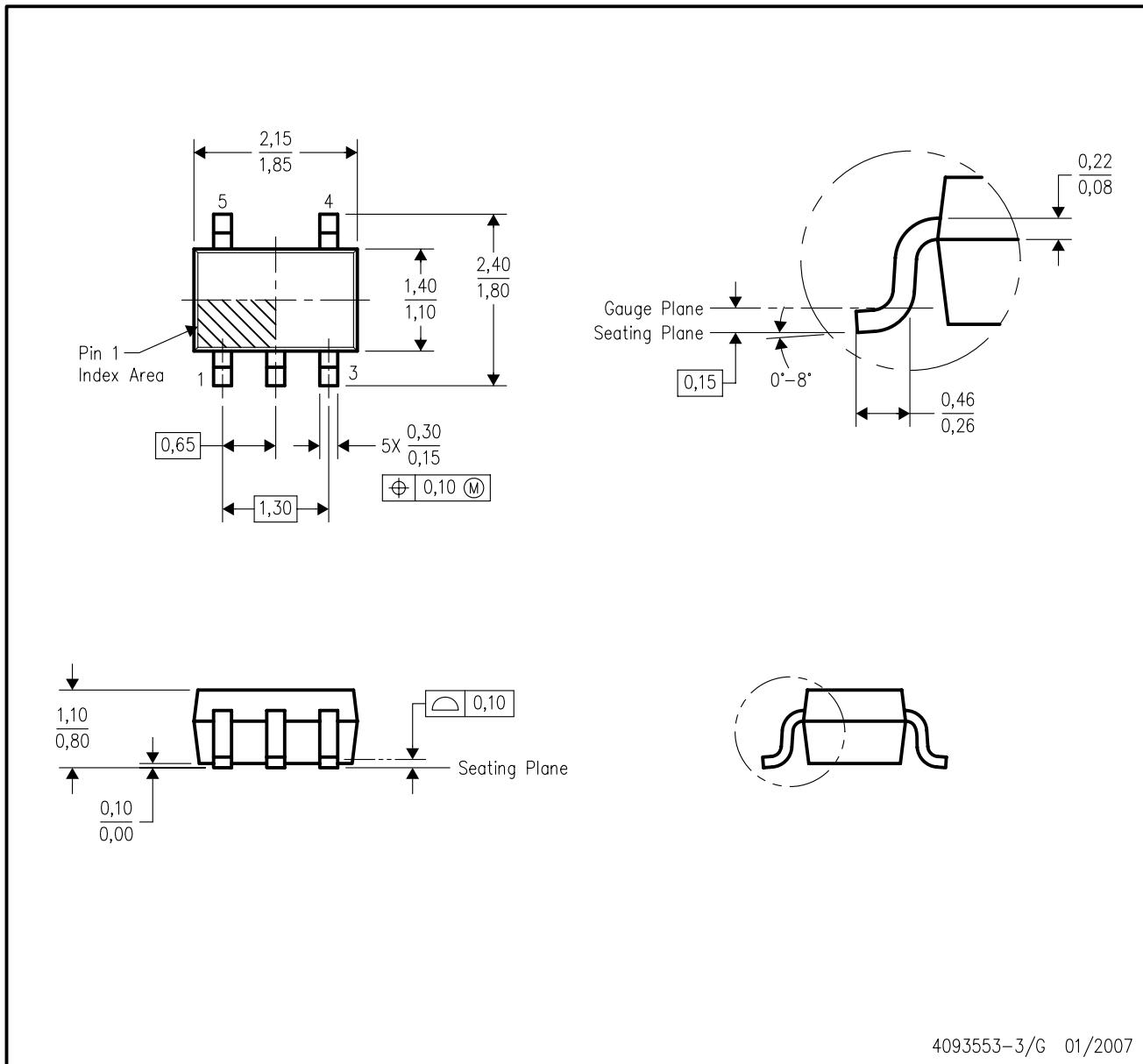
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061IDCKR | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |
| TLV9061IDPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| TLV9061SIDBVR | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 366.0 | 364.0 | 50.0 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 366.0 | 364.0 | 50.0 |
| TLV9062IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TLV9062IDSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 366.0 | 364.0 | 50.0 |
| TLV9062SIDGSR | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV9062SIRUGR | X2QFN | RUG | 10 | 3000 | 205.0 | 200.0 | 33.0 |
| TLV9064IDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV9064IPWR | TSSOP | PW | 14 | 2000 | 366.0 | 364.0 | 50.0 |
| TLV9064IPWT | TSSOP | PW | 14 | 250 | 366.0 | 364.0 | 50.0 |
| TLV9064IRTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TLV9064IRUCR | QFN | RUC | 14 | 3000 | 205.0 | 200.0 | 30.0 |
| TLV9064SIRTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

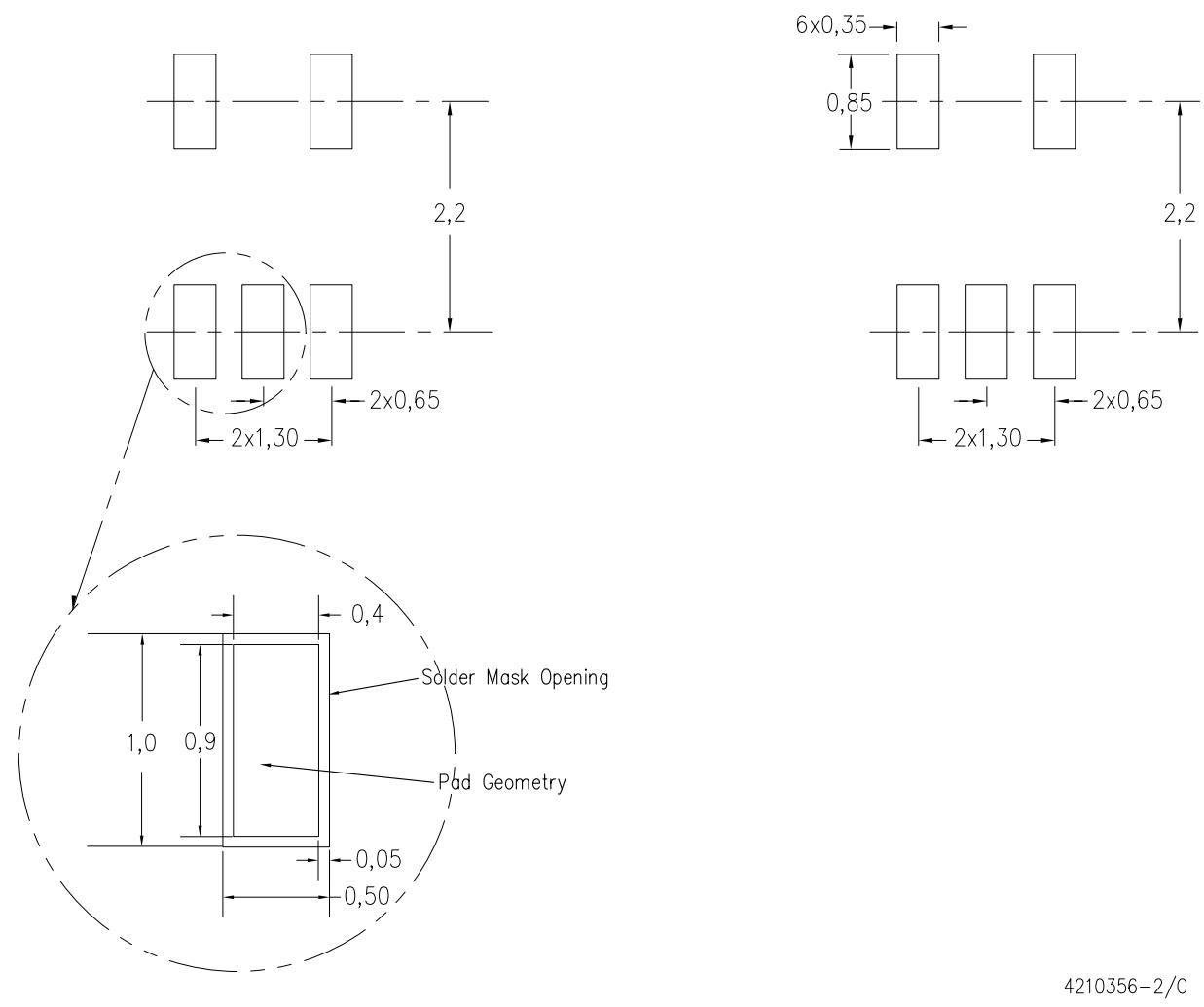
LAND PATTERN DATA

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4210356-2/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

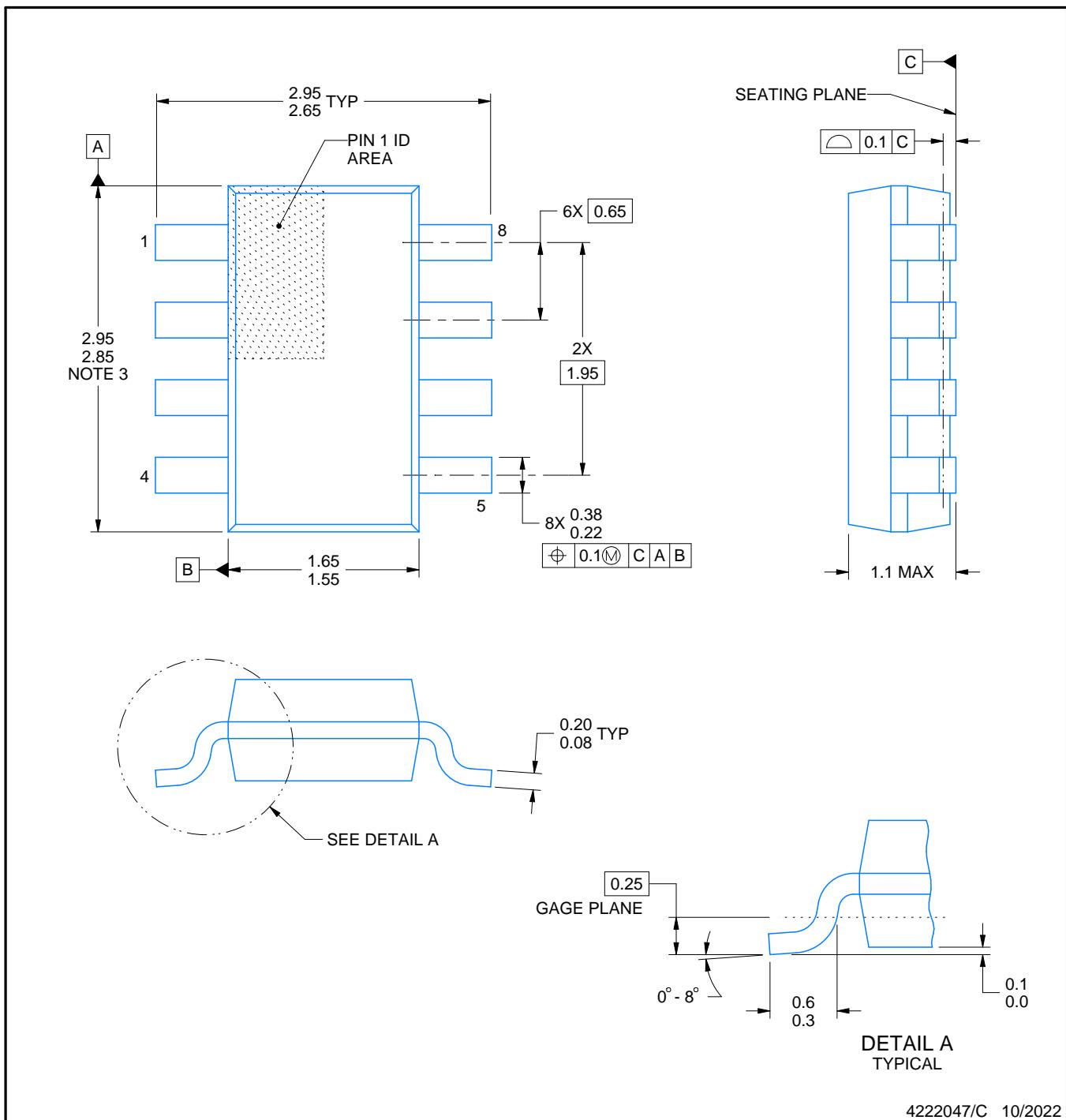
PACKAGE OUTLINE

DDF0008A



SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

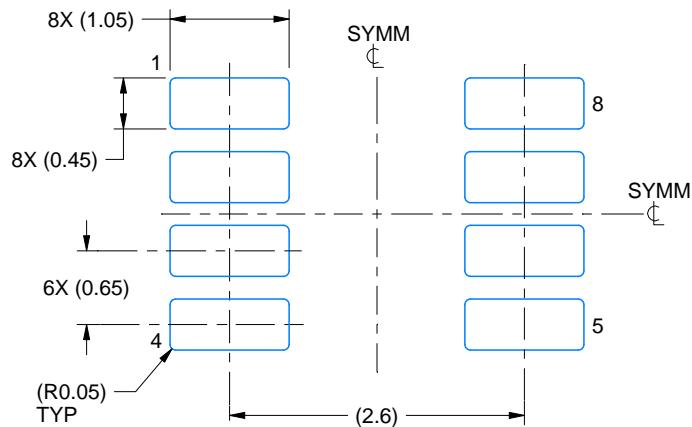
4222047/C 10/2022

EXAMPLE BOARD LAYOUT

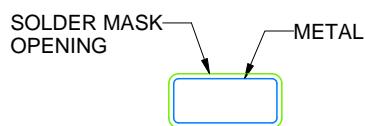
DDF0008A

SOT-23 - 1.1 mm max height

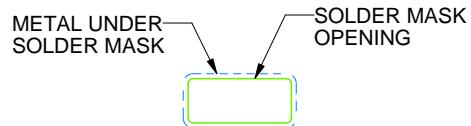
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

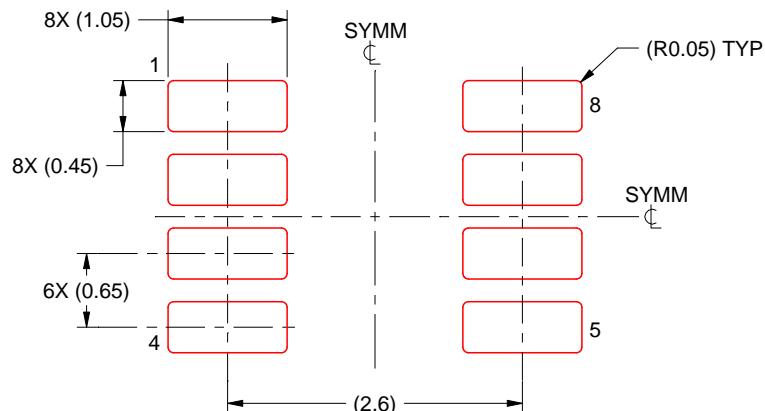
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

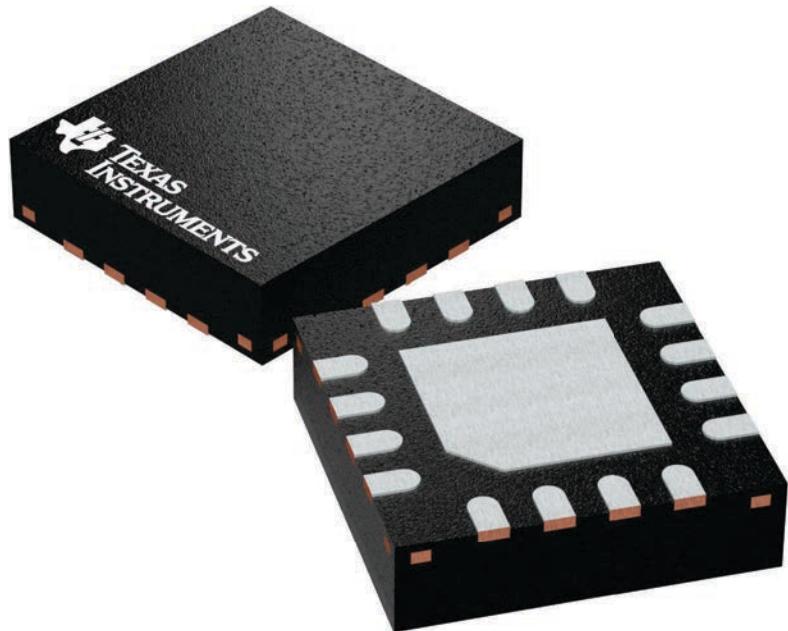
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A

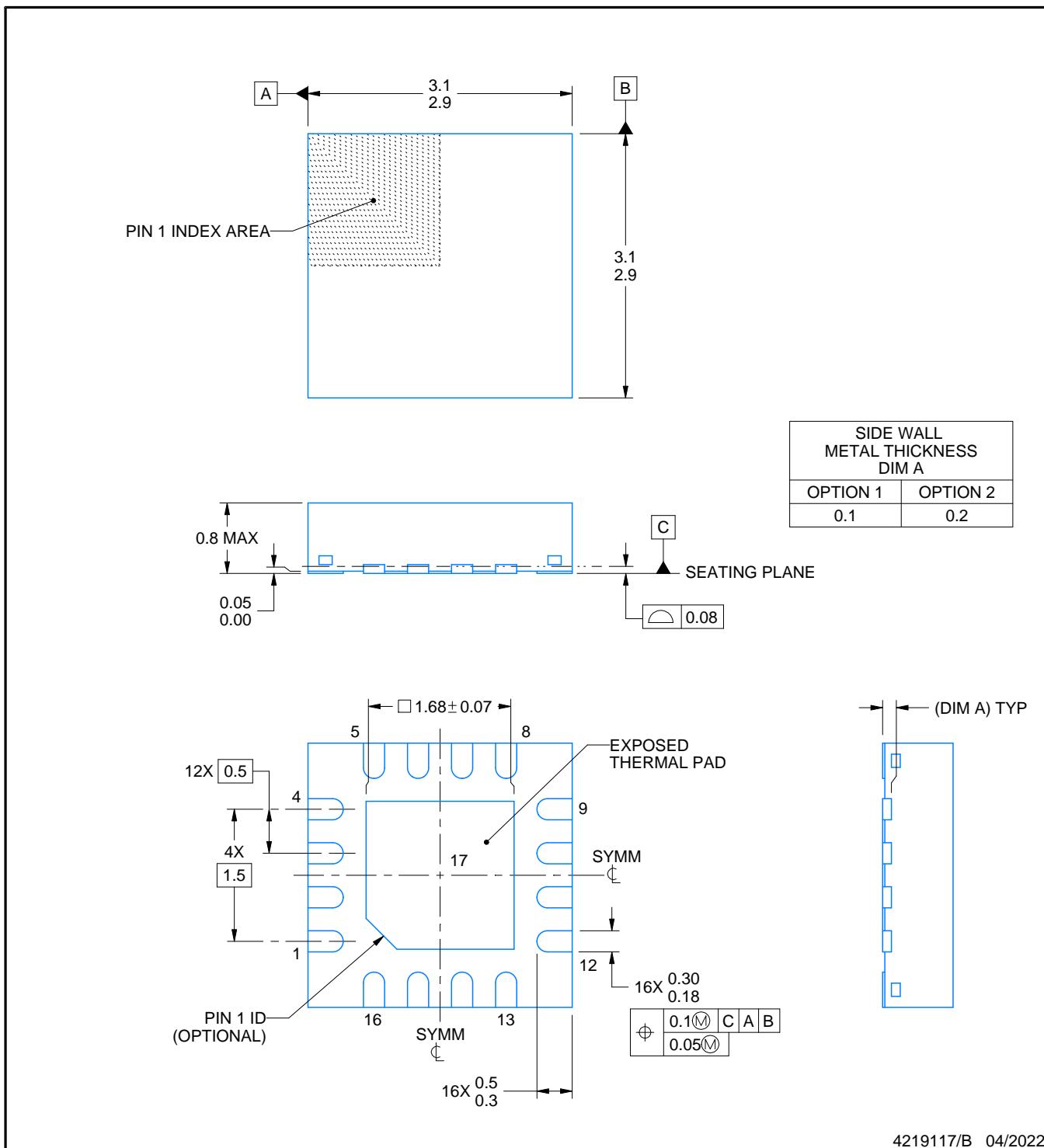
PACKAGE OUTLINE

RTE0016C



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219117/B 04/2022

NOTES:

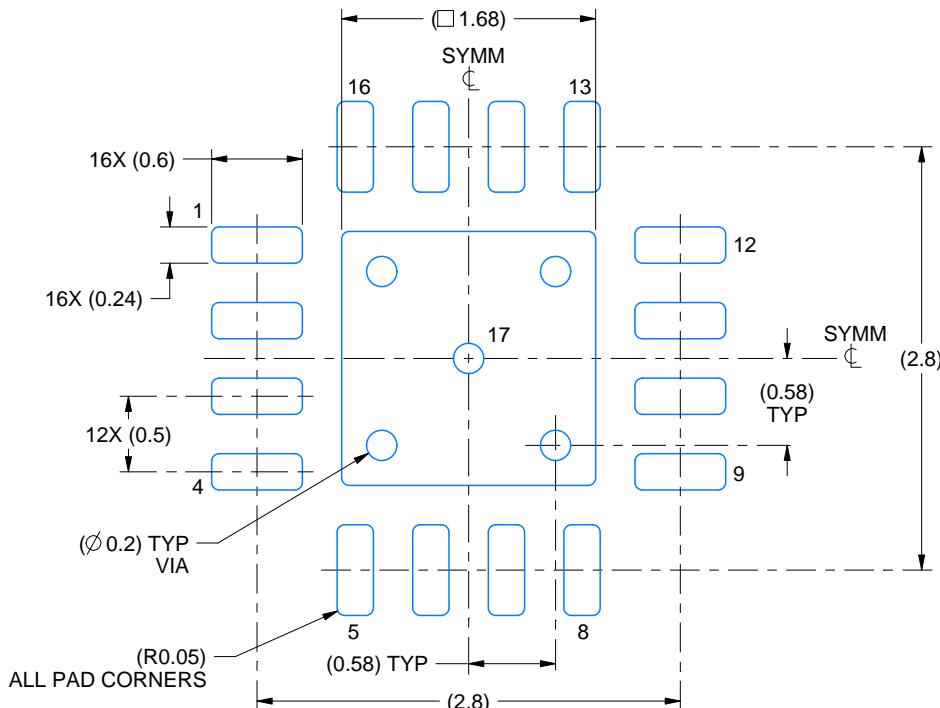
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

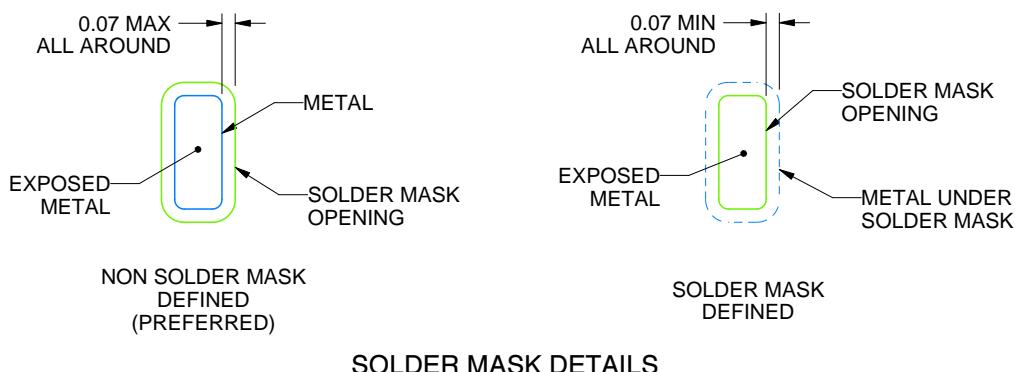
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

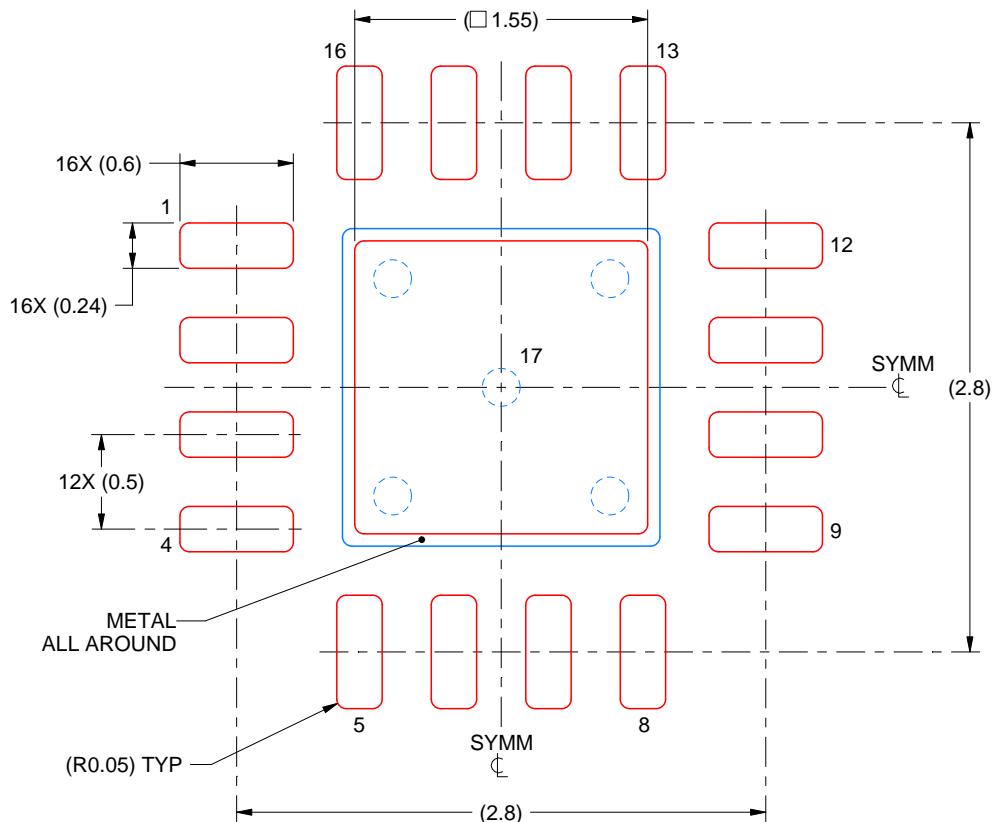
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

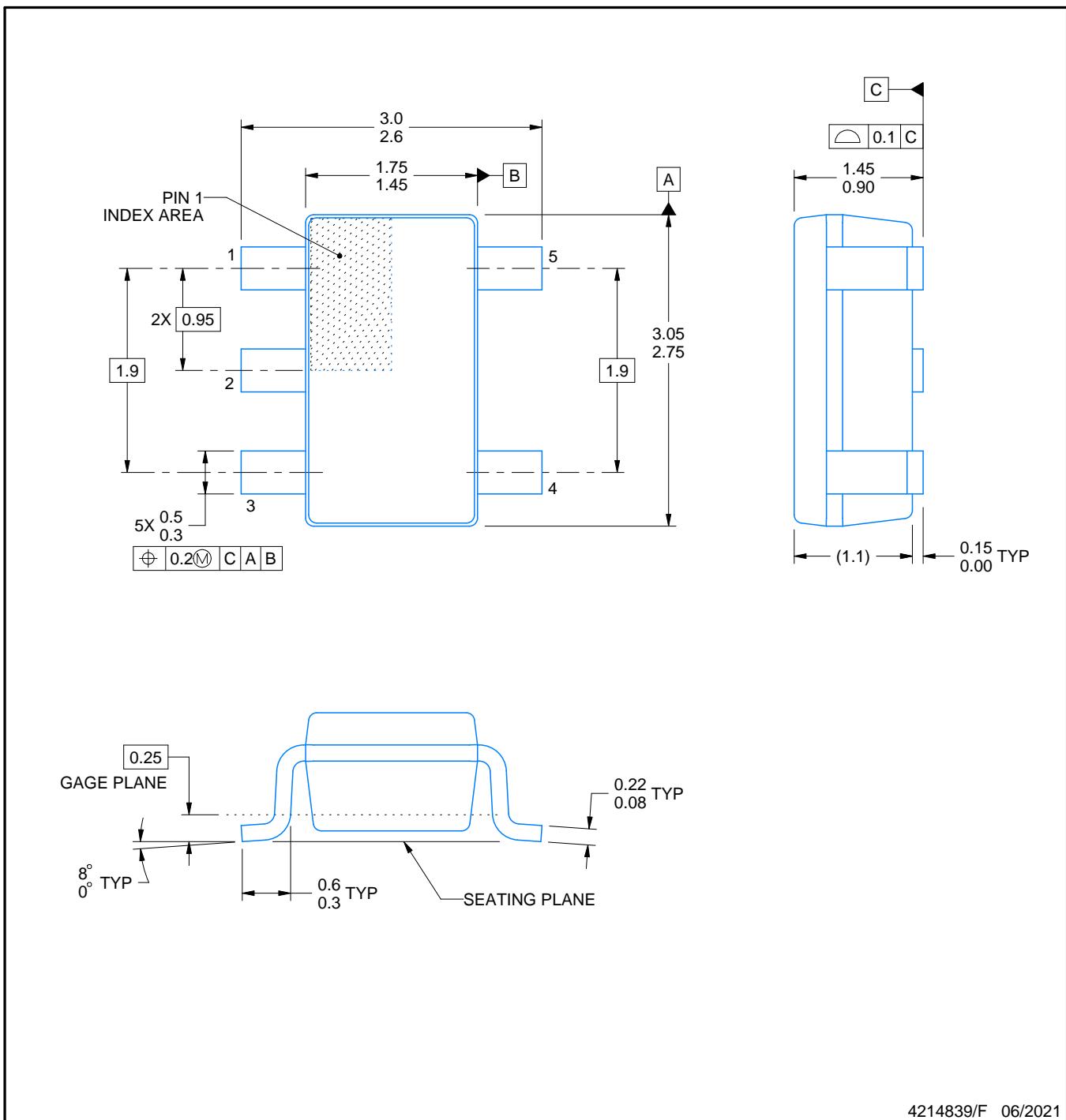
PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

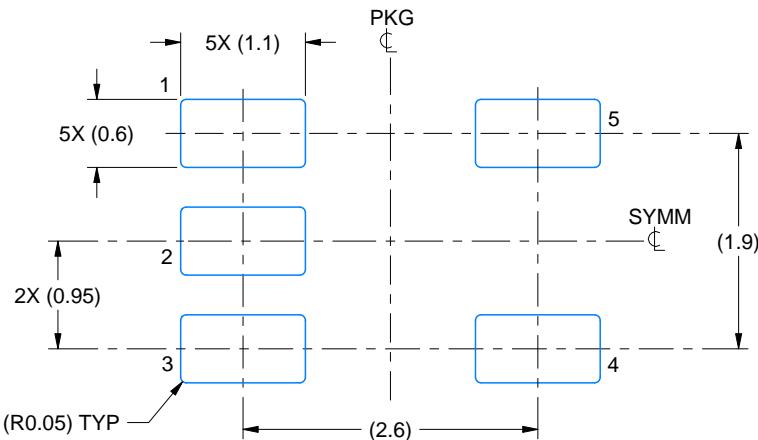
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

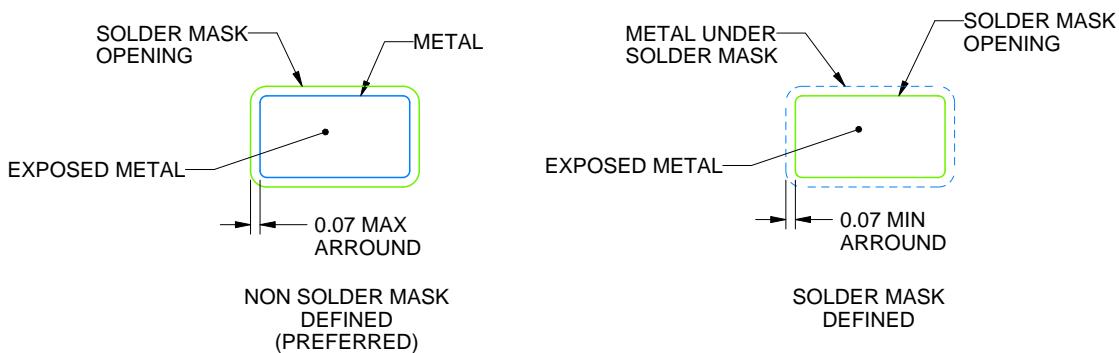
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

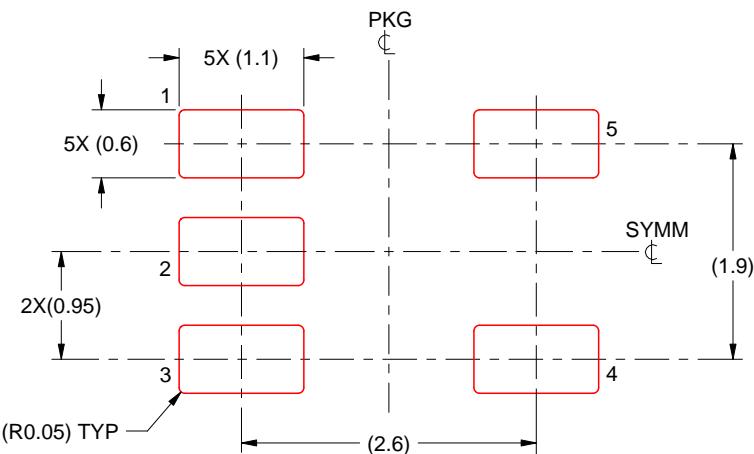
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

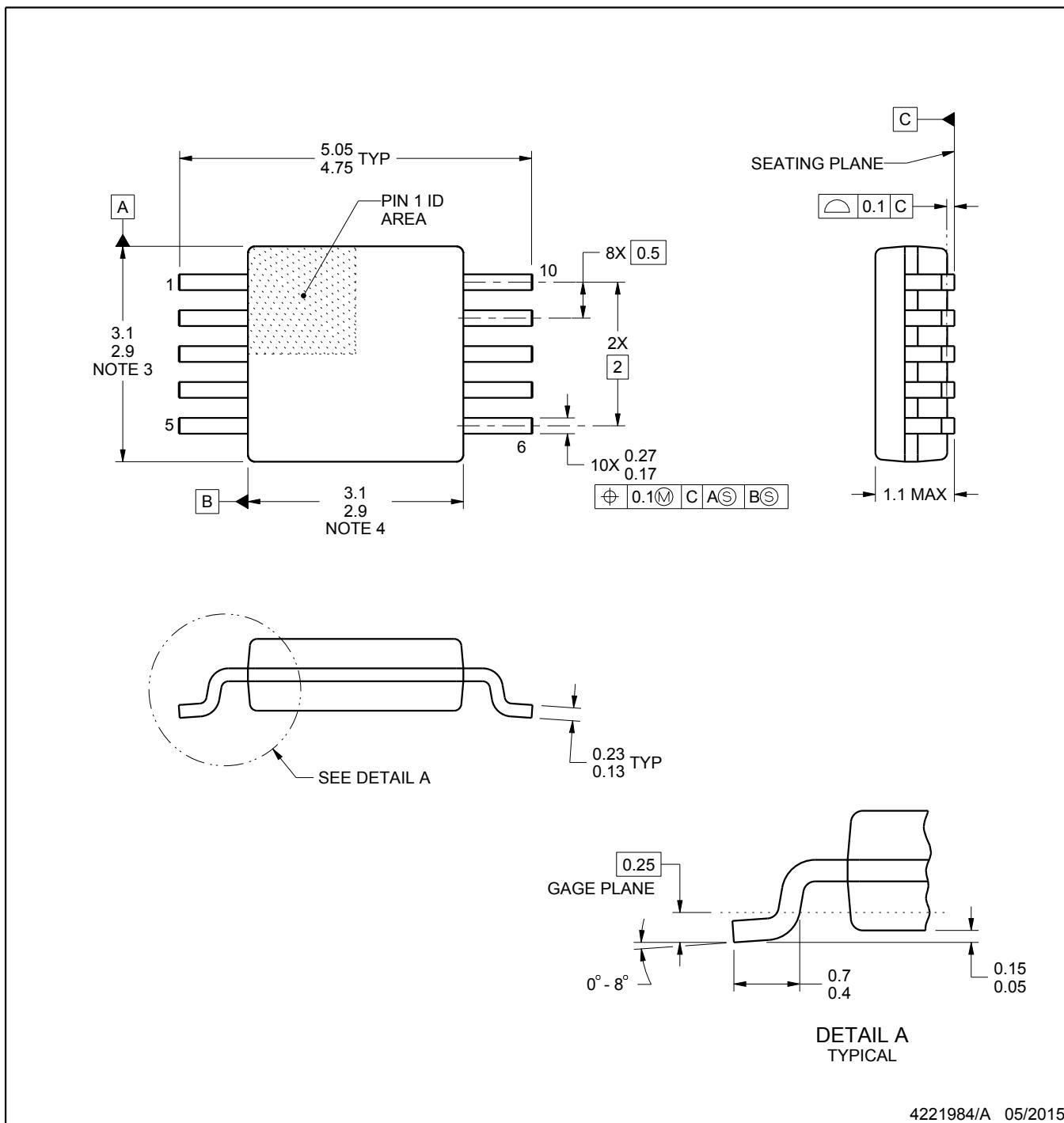
PACKAGE OUTLINE

DGS0010A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

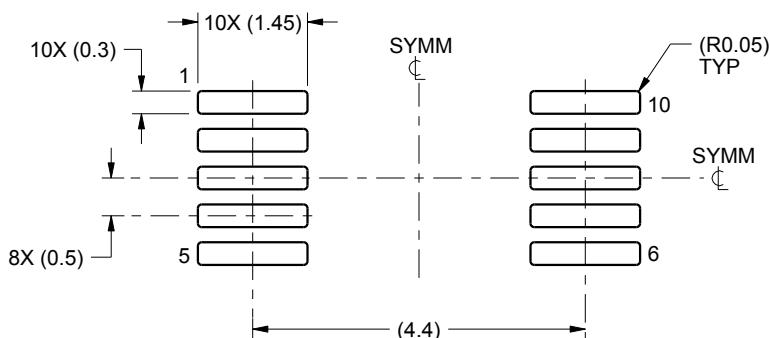
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

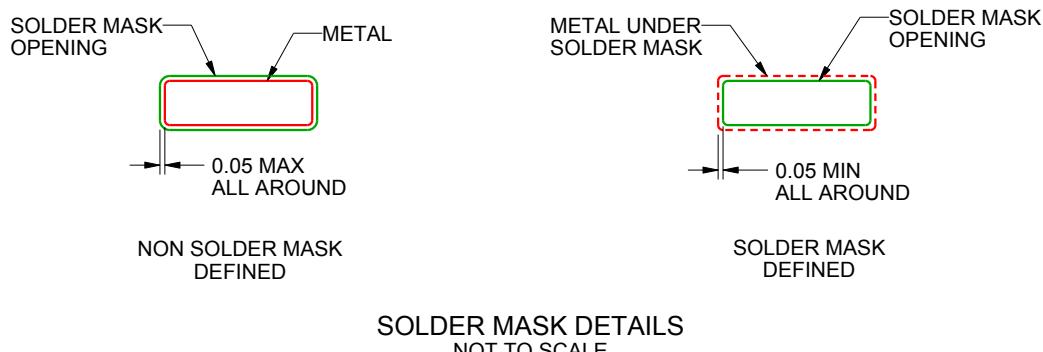
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

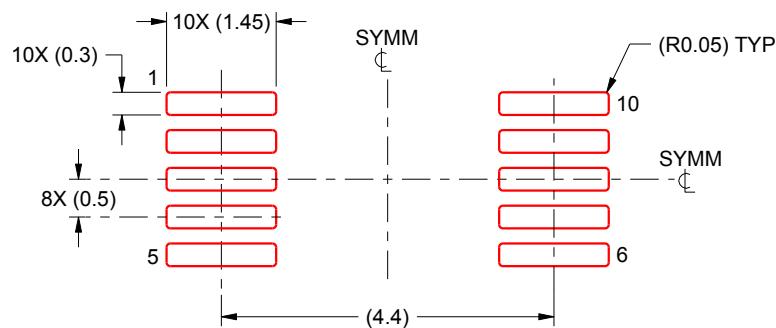
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DPW 5

GENERIC PACKAGE VIEW

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D

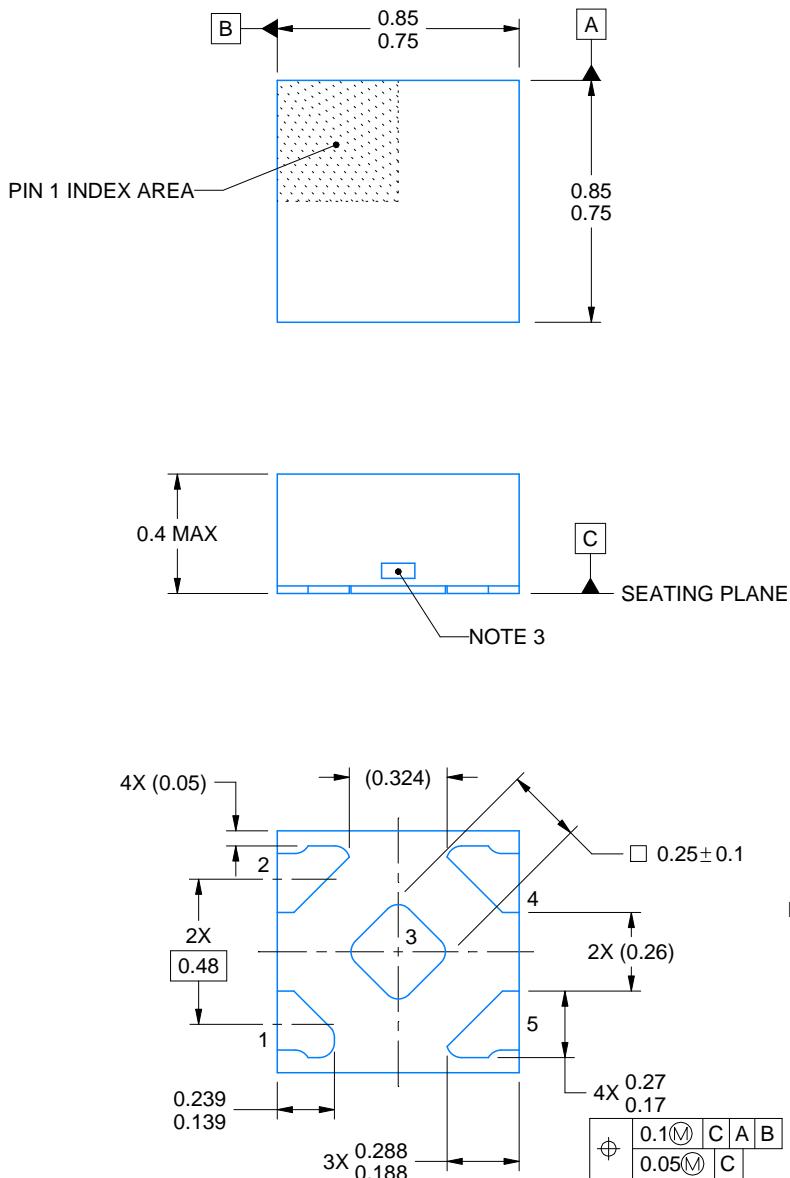
PACKAGE OUTLINE

DPW0005A



X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

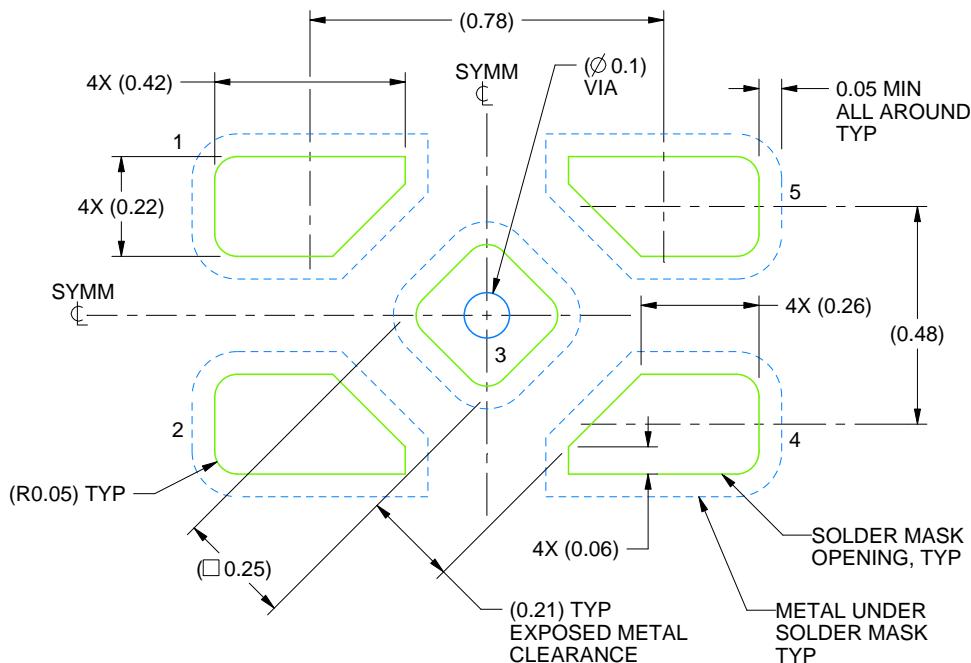
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

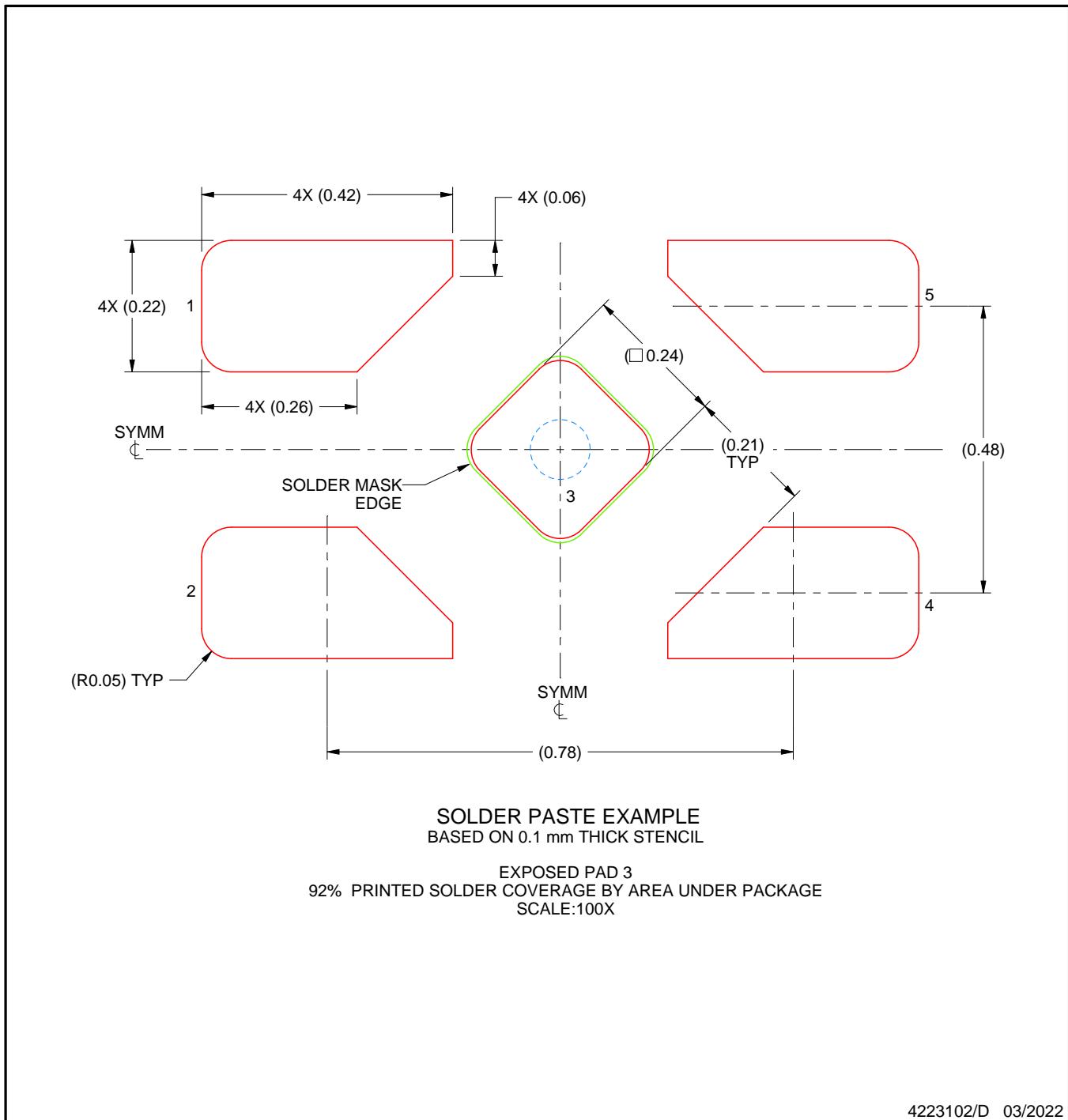
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

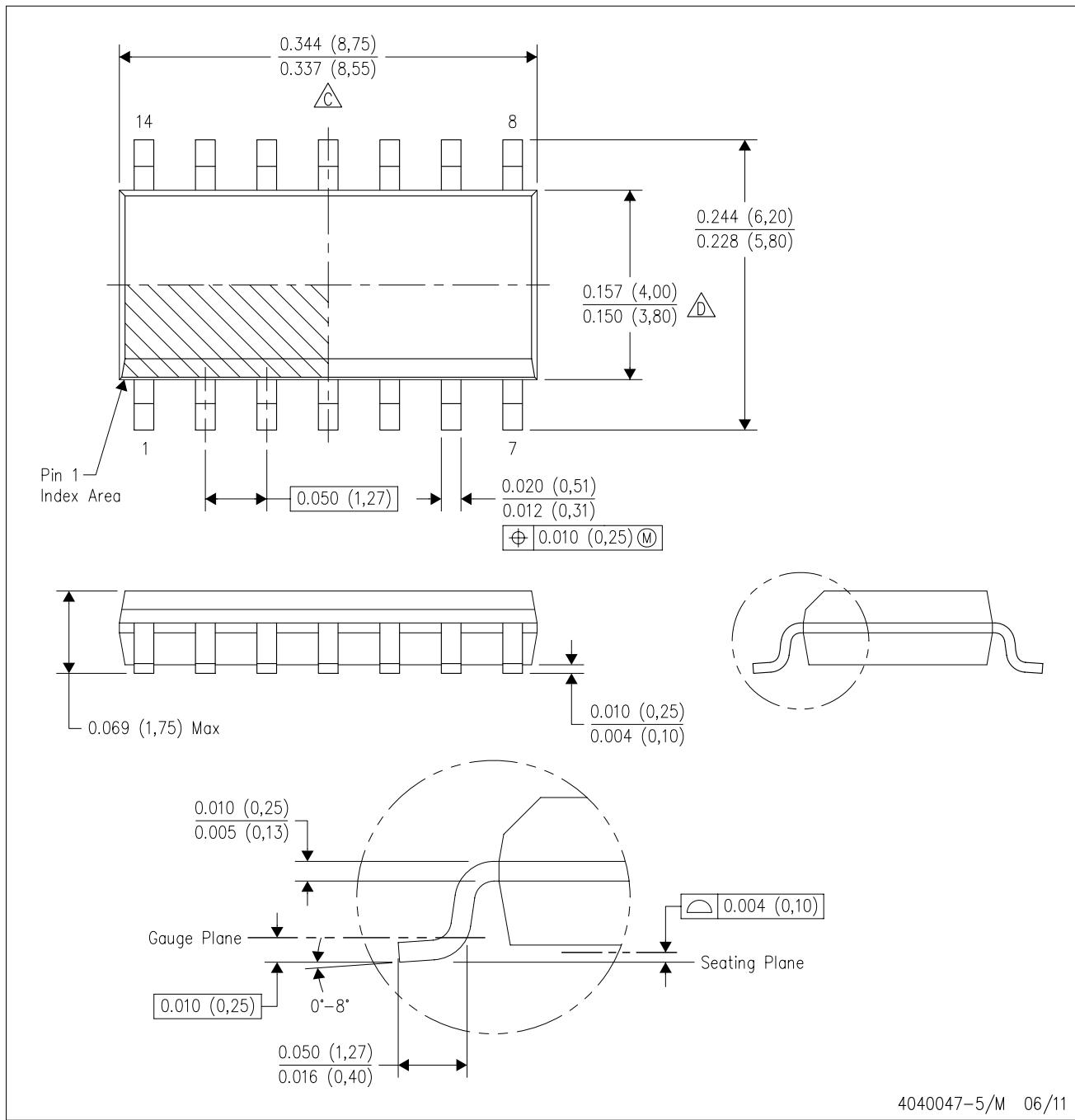


NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

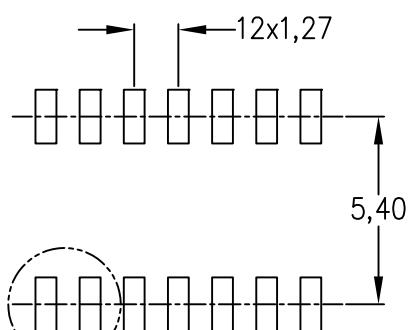
E. Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

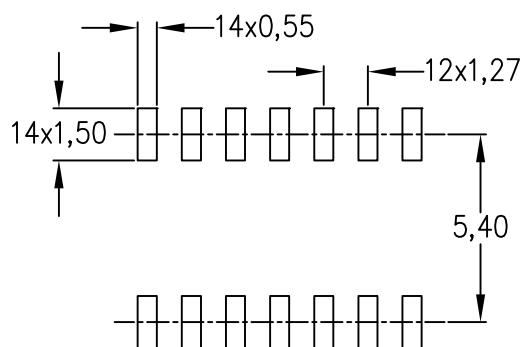
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

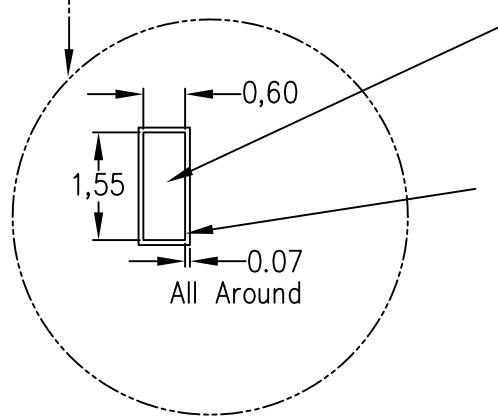
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

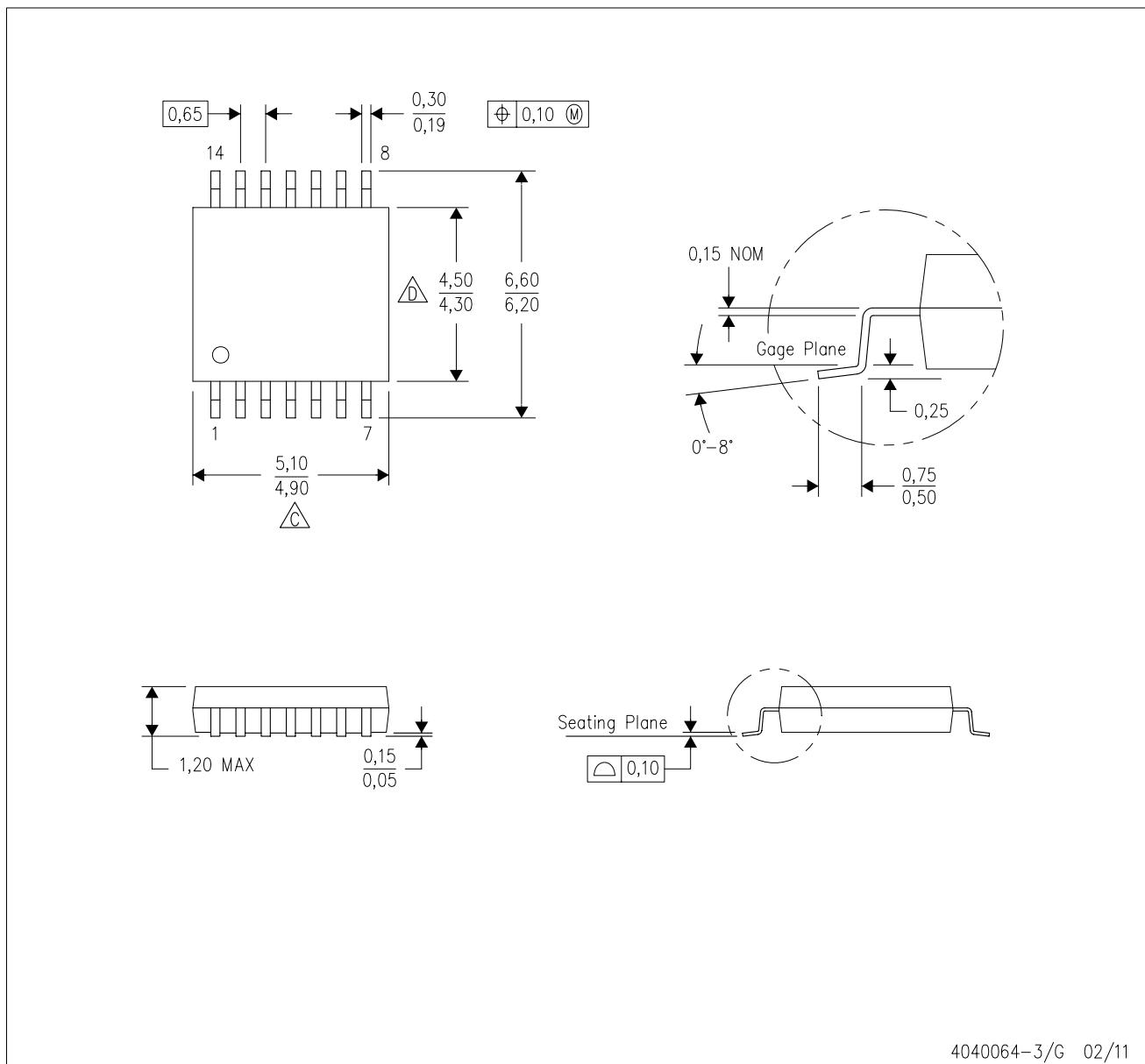
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

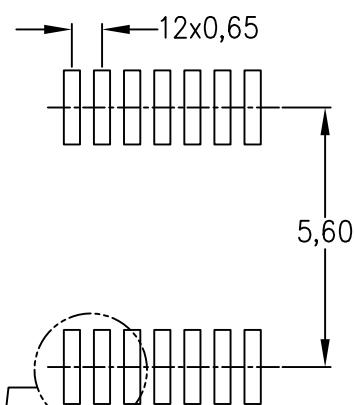
E. Falls within JEDEC MO-153

LAND PATTERN DATA

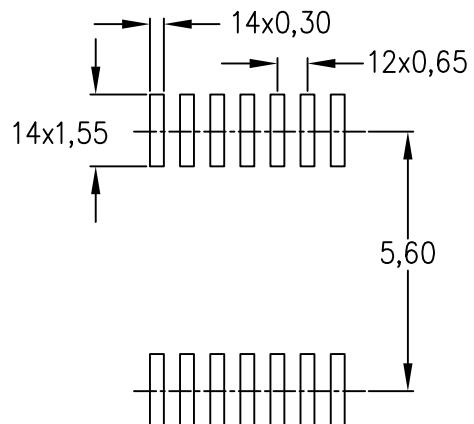
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

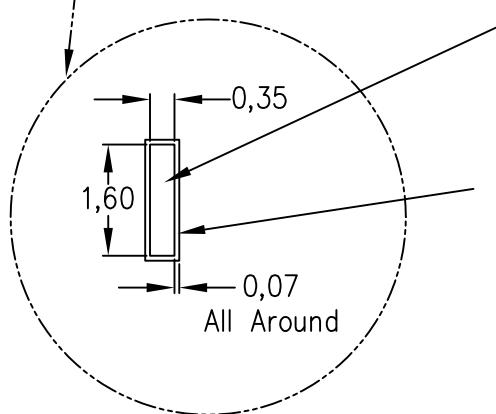
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

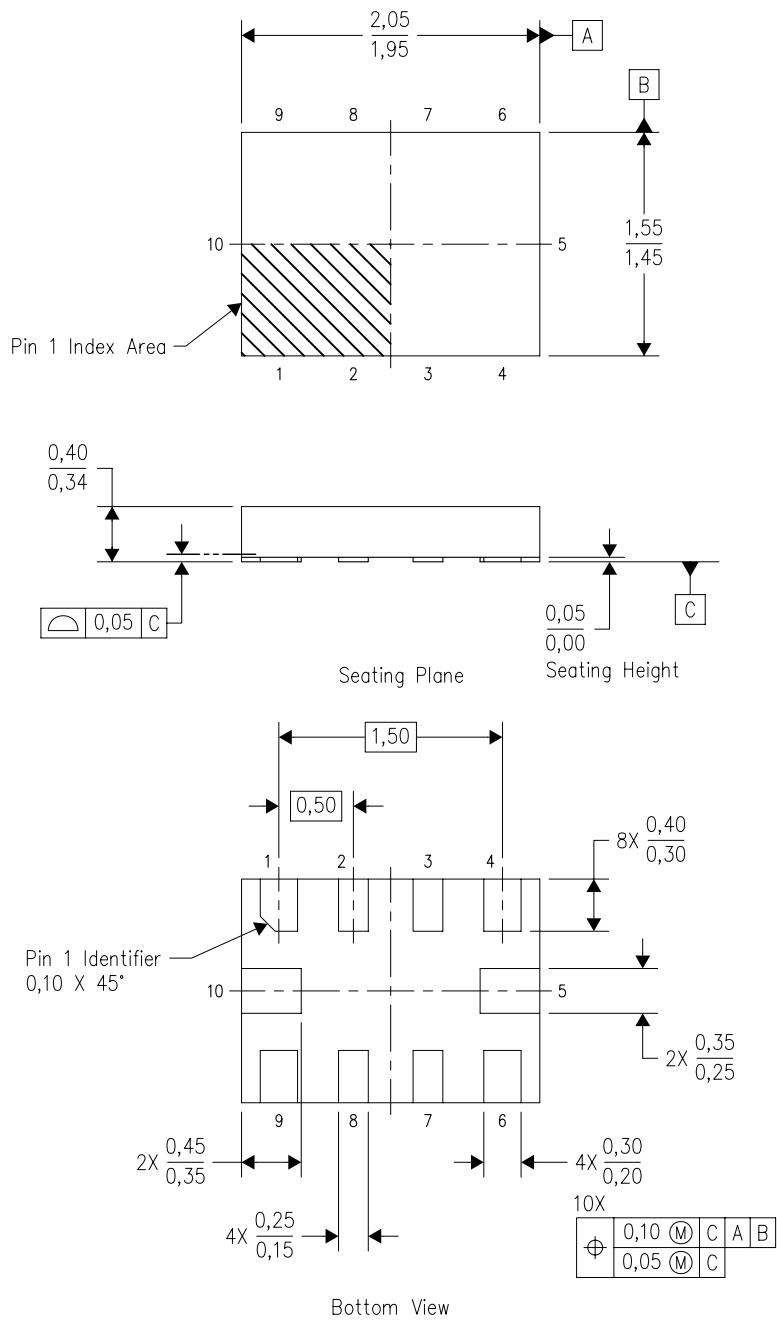
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RUG (R-PQFP-N10)

PLASTIC QUAD FLATPACK

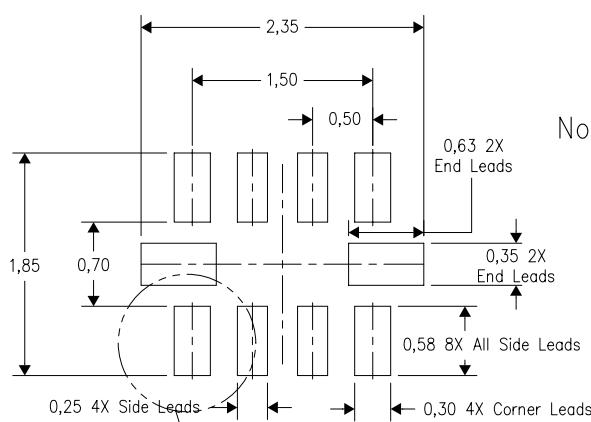
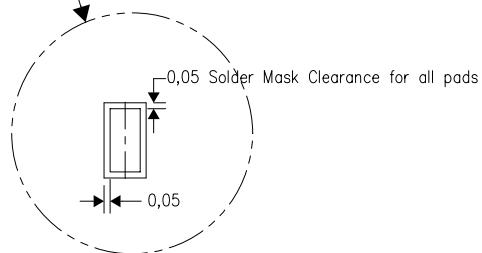
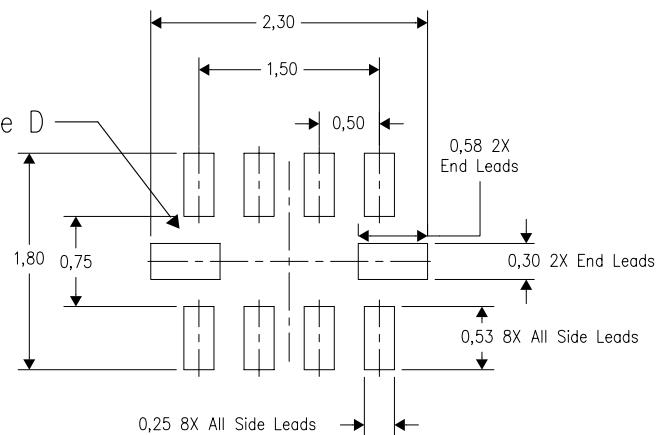


4208528-3/B 04/2008

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - This package complies to JEDEC MO-288 variation X2EFD.

RUG (R-PQFP-N10)

Example Board Layout

Example Stencil Design
(Note E)

4210299-3/A 06/09

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

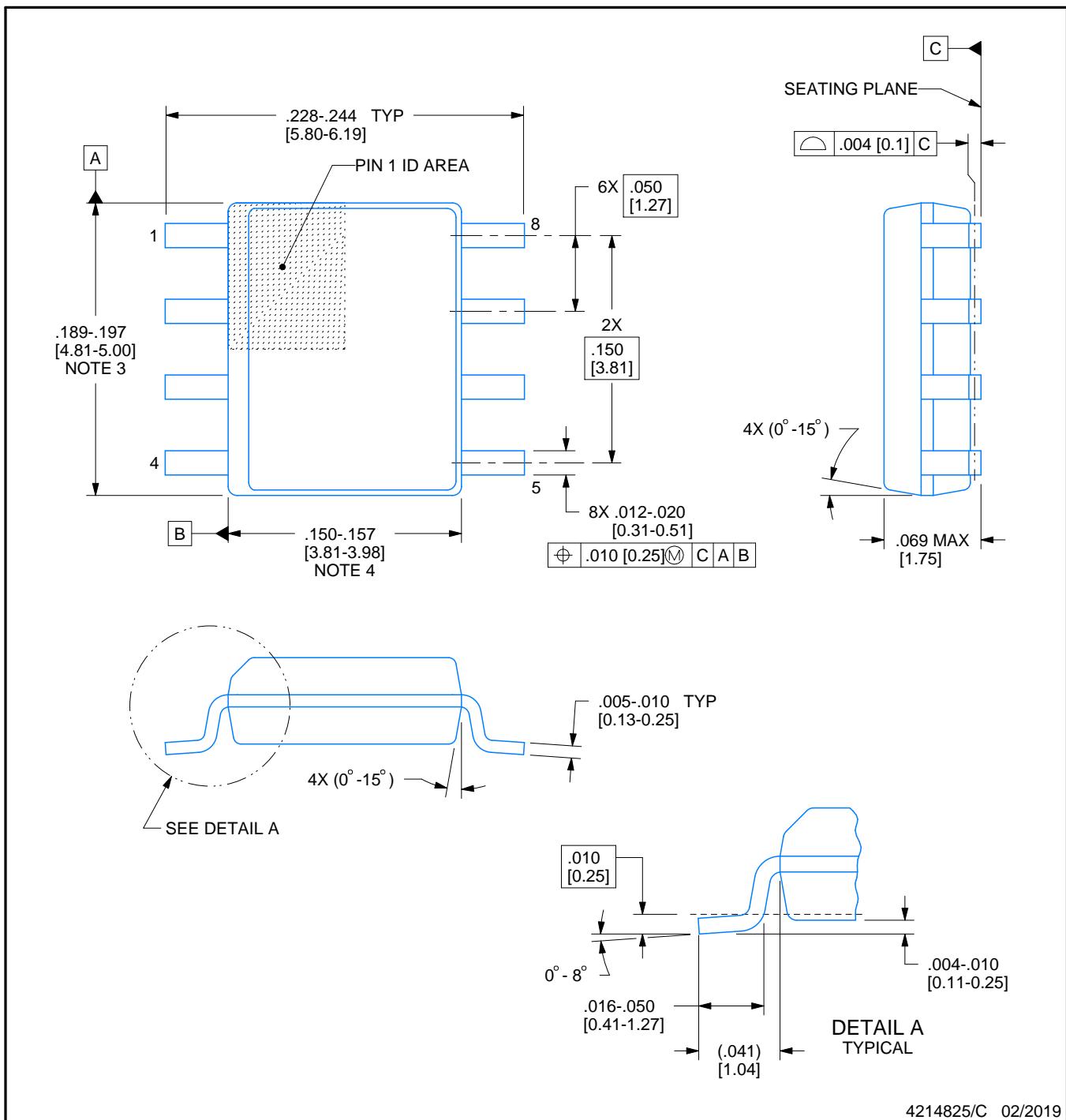
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

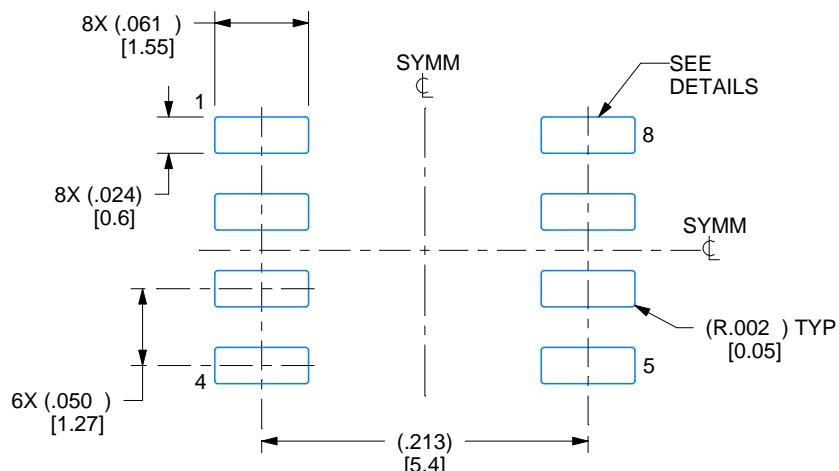
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

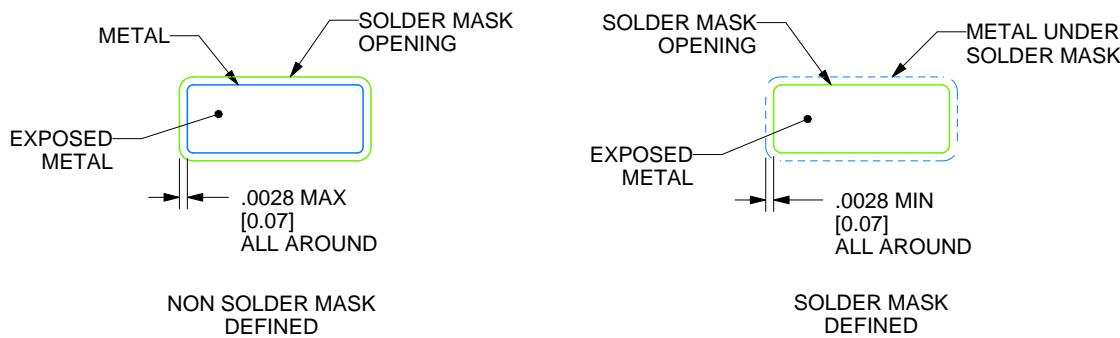
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

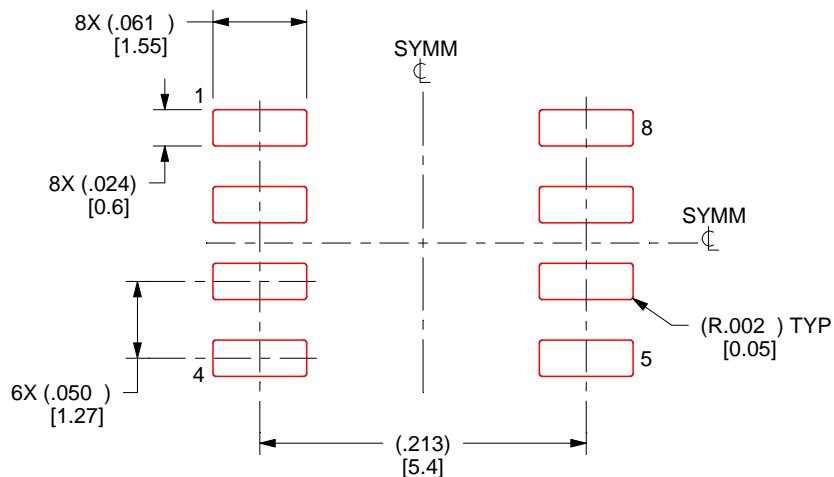
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

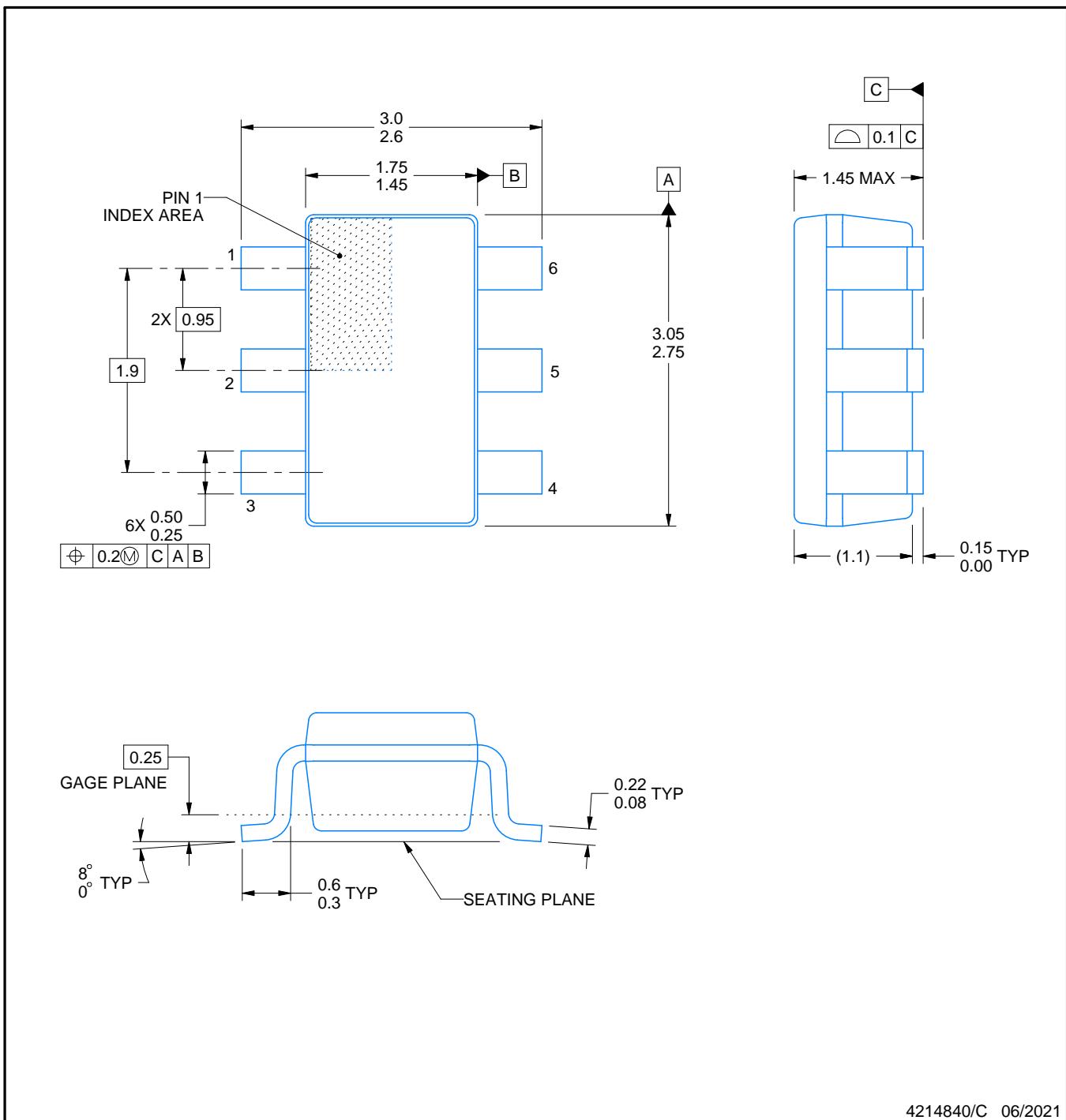
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

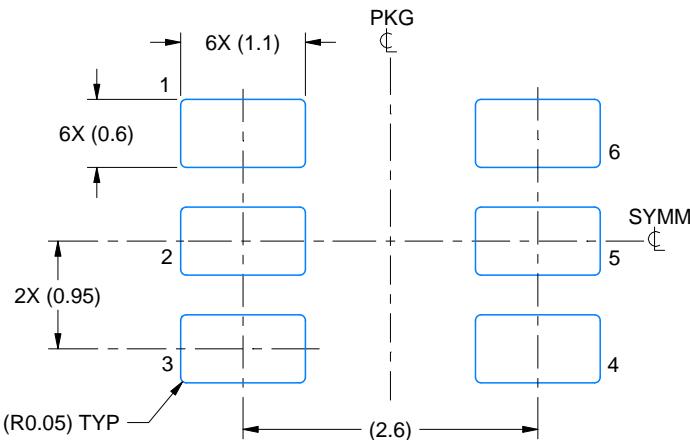
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

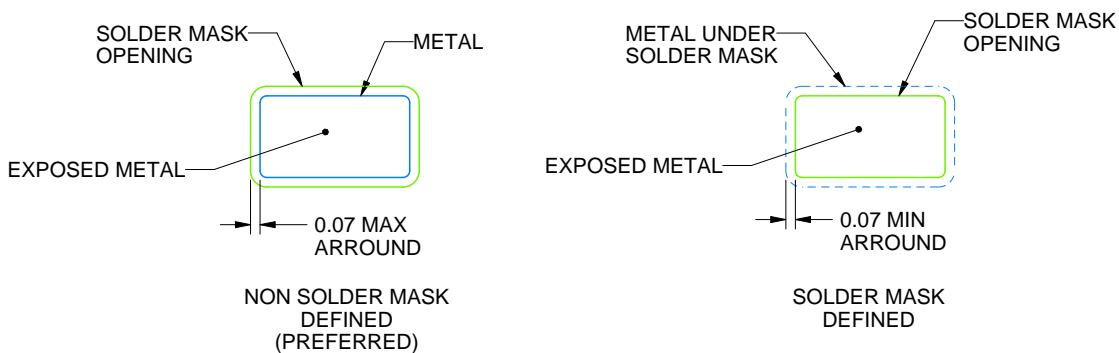
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

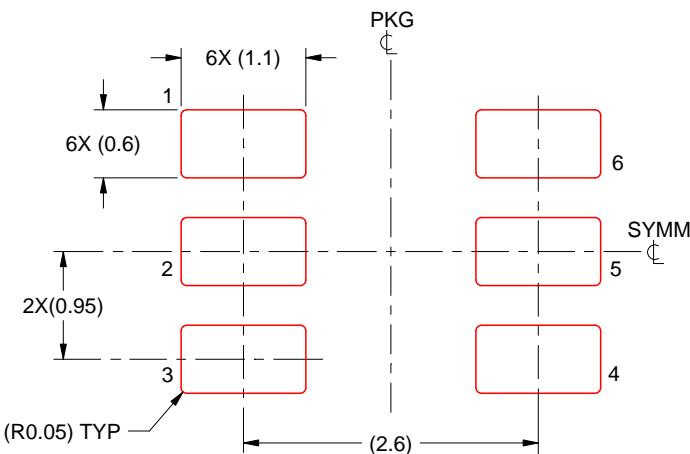
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

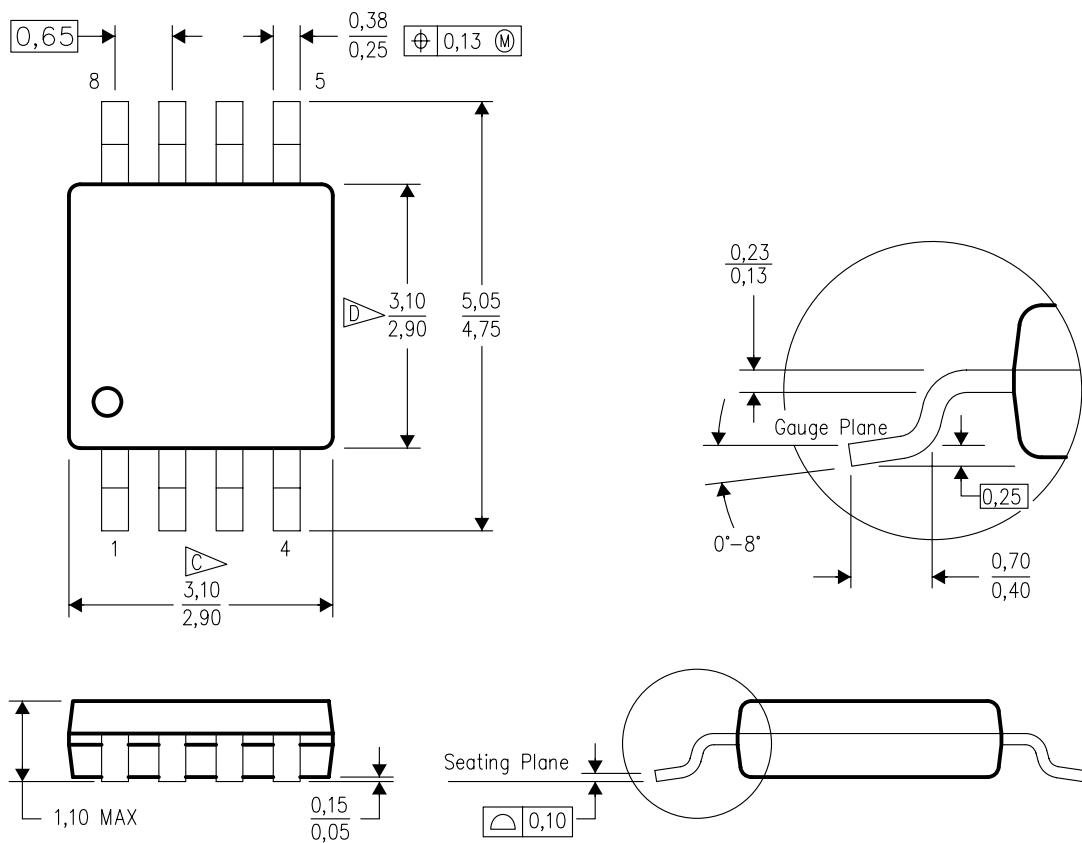
4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

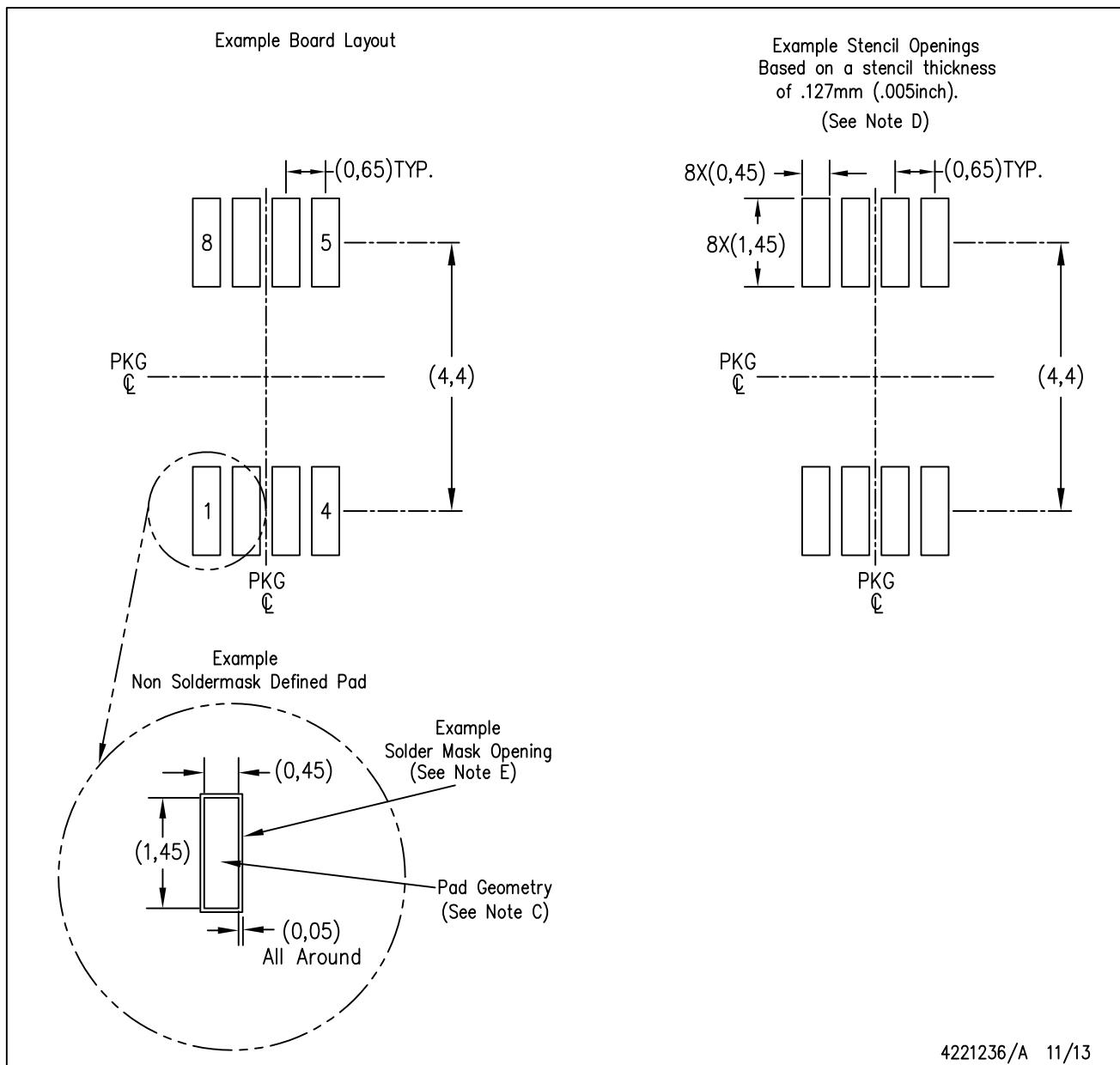
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

LAND PATTERN DATA

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

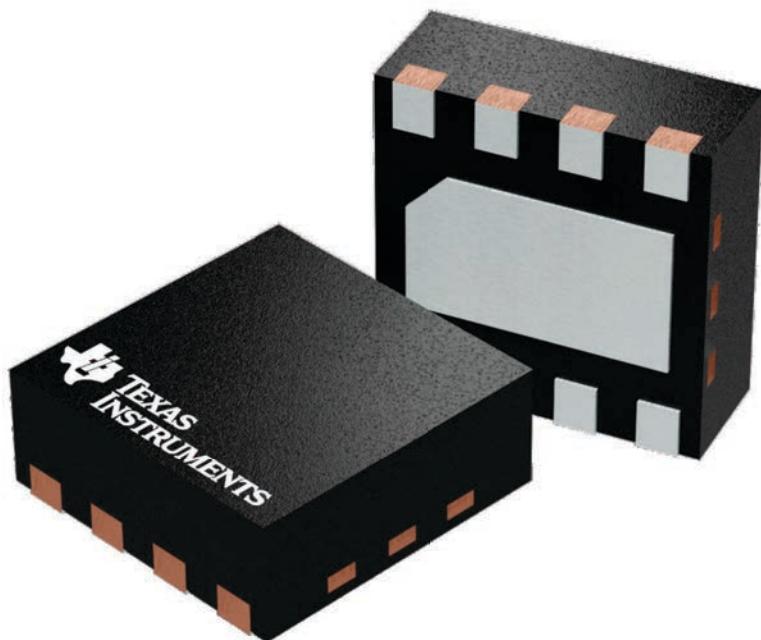
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

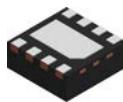
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

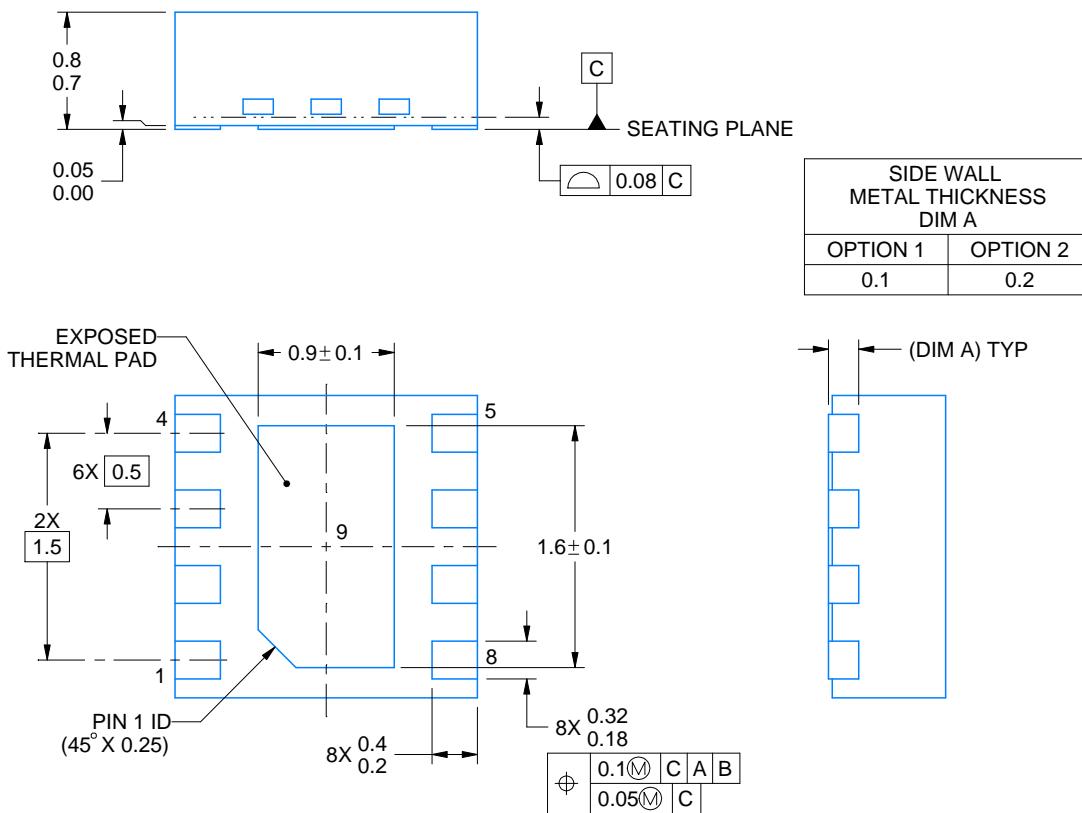
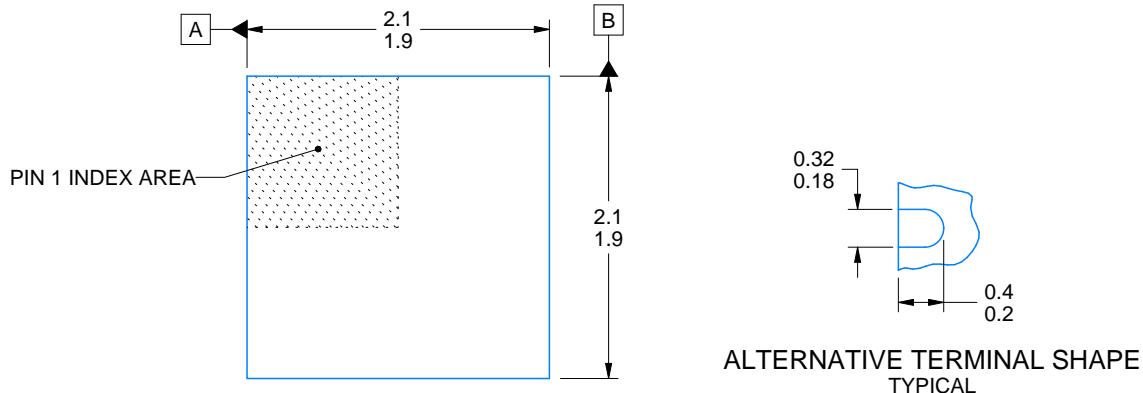
PACKAGE OUTLINE

DSG0008A



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218900/E 08/2022

NOTES:

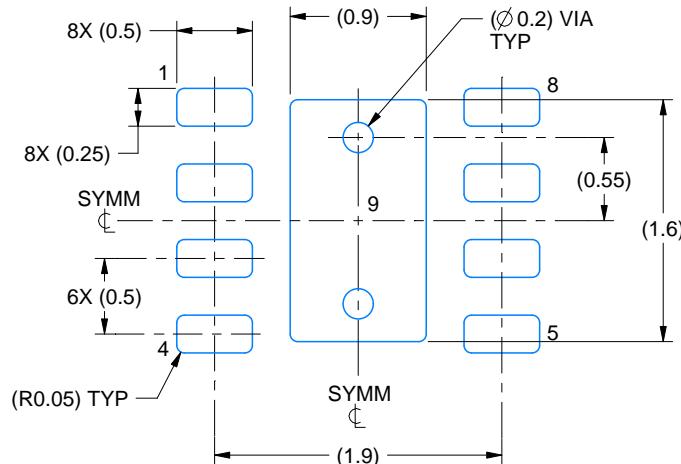
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

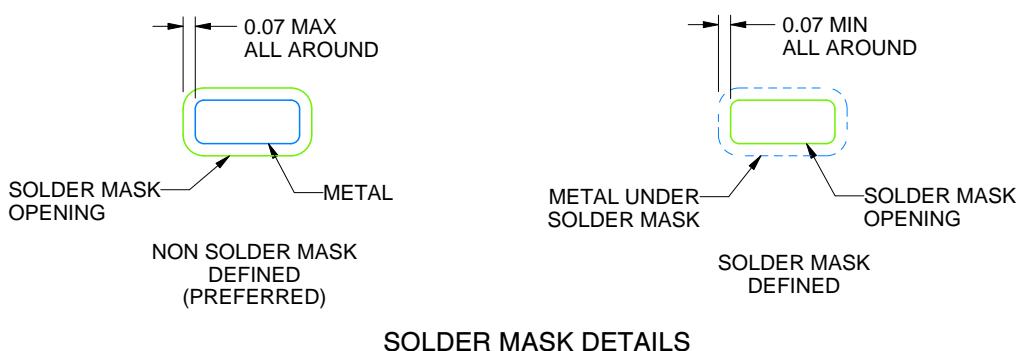
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

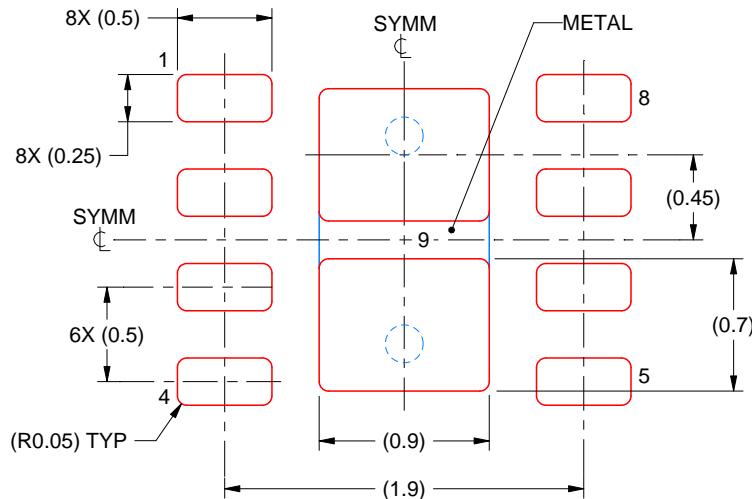
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

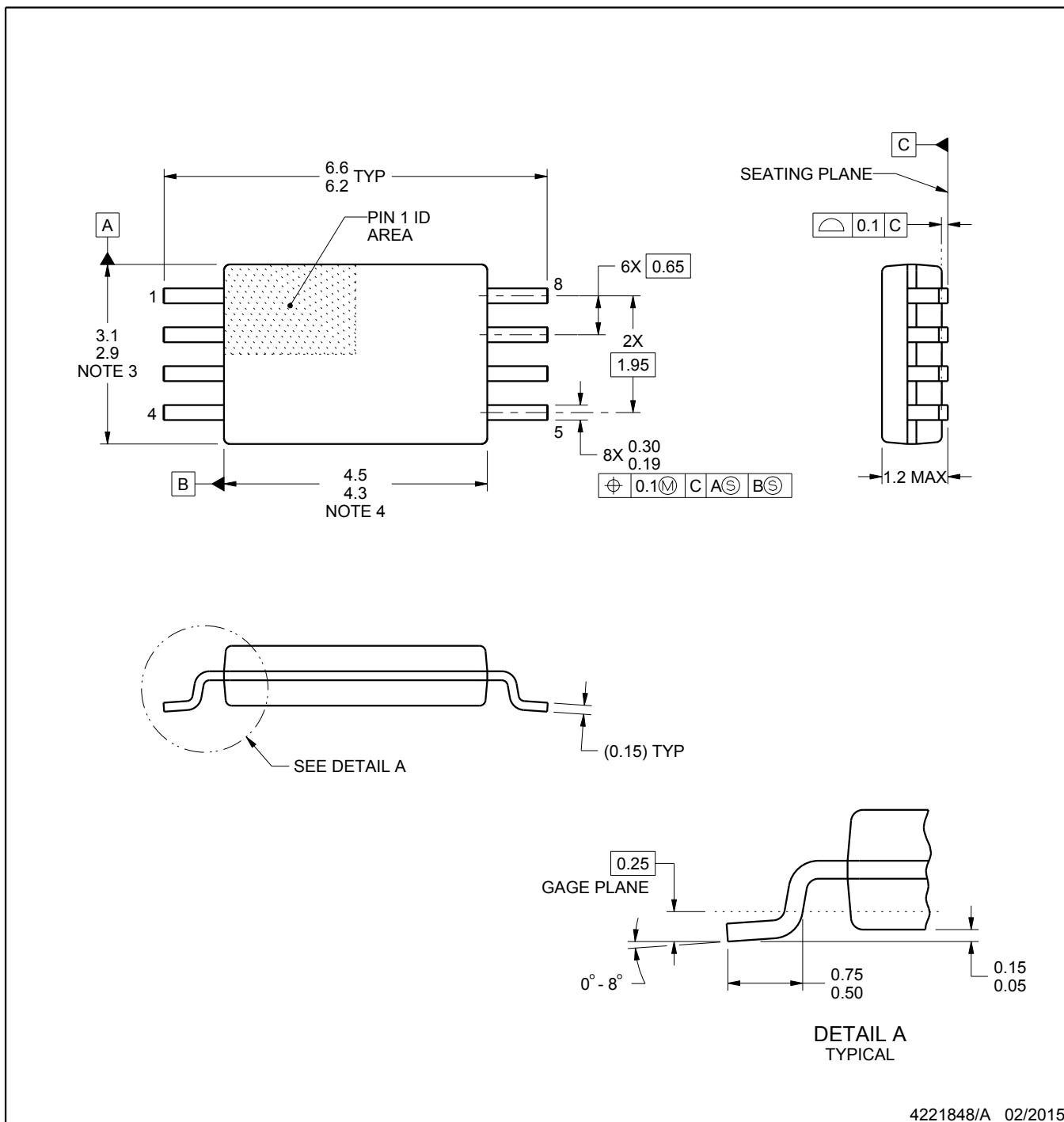
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

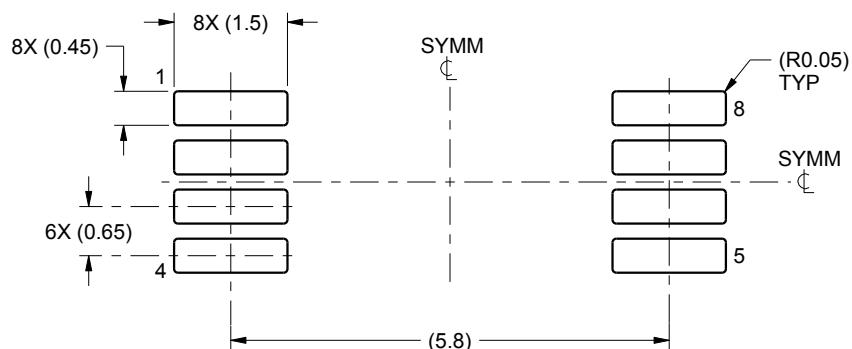
4221848/A 02/2015

EXAMPLE BOARD LAYOUT

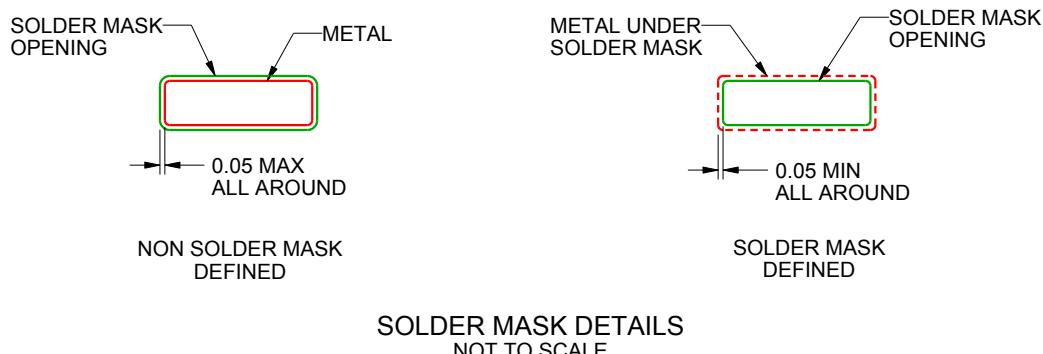
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

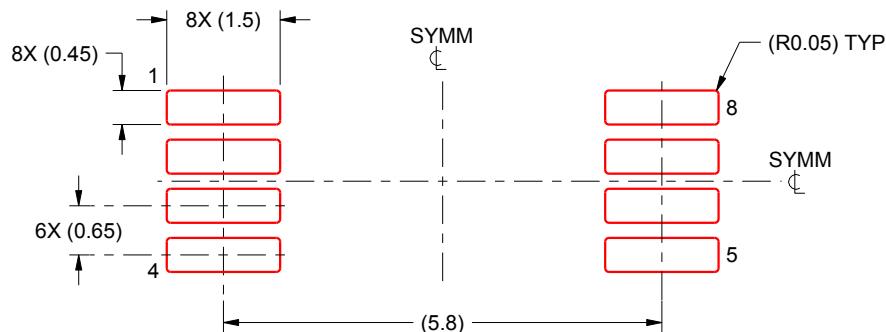
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

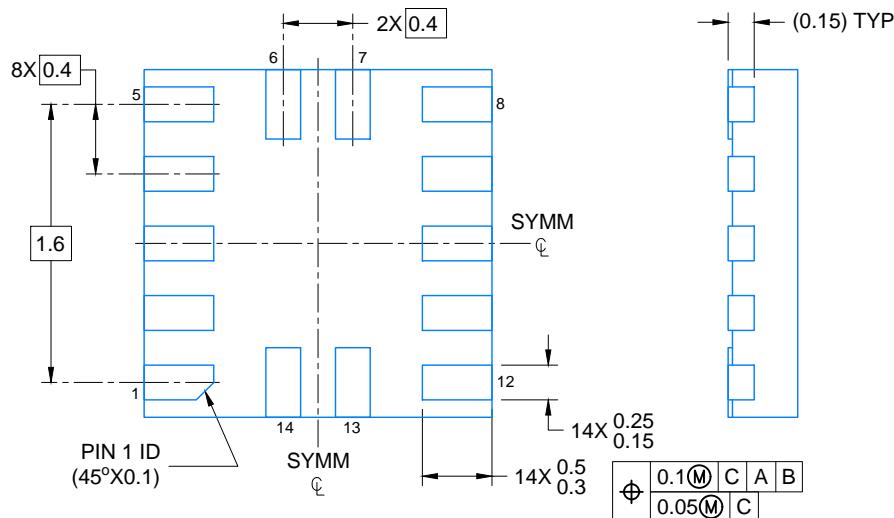
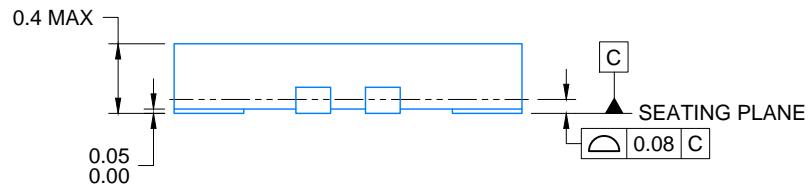
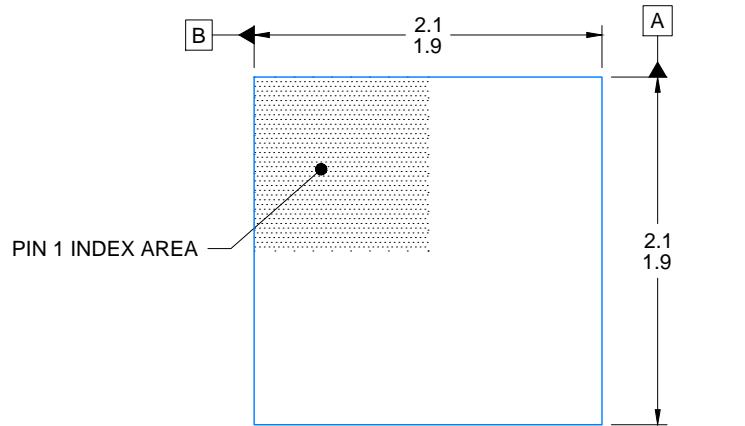
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RUC0014A

PACKAGE OUTLINE

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



4220584/A 05/2019

NOTES:

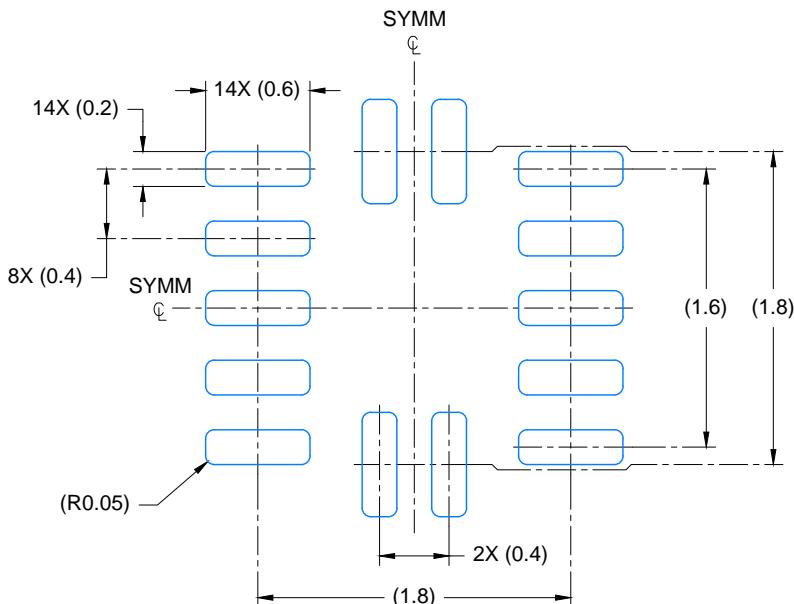
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

RUC0014A

EXAMPLE BOARD LAYOUT

X2QFN - 0.4 mm max height

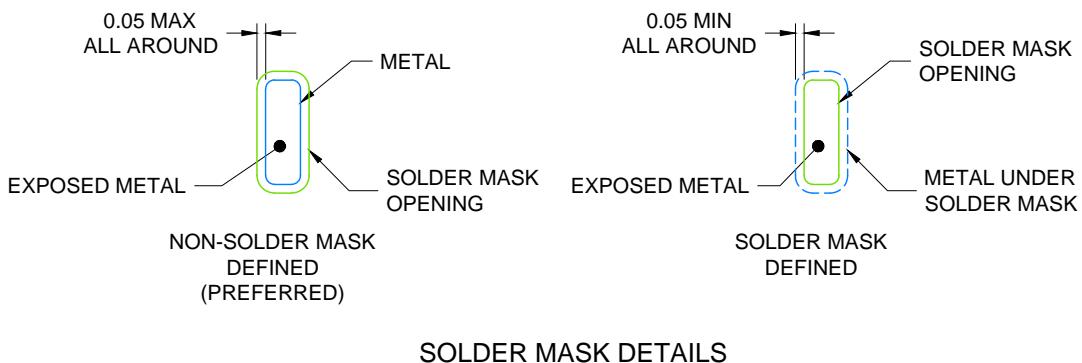
PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

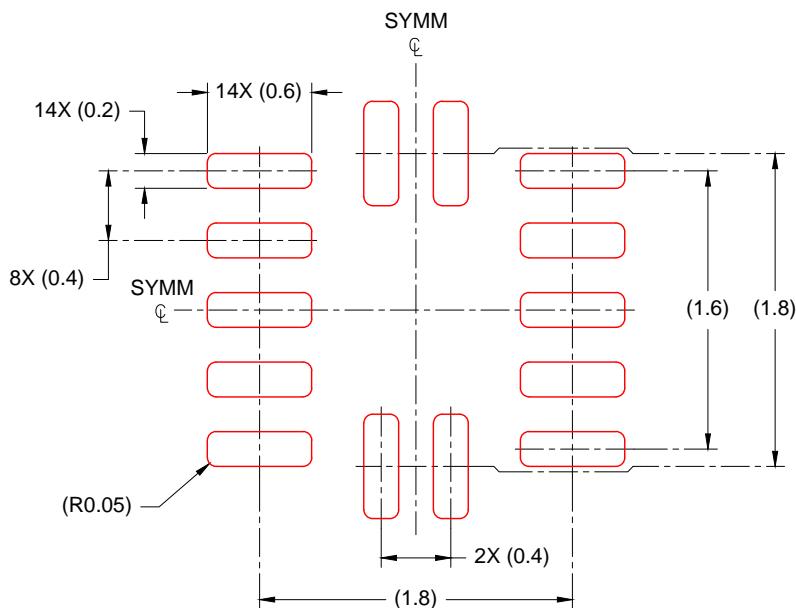
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

X2QFN - 0.4 mm max height

RUC0014A

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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