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Arquiteturas para Sistemas Embutidos

Aula3

ESP32-WROOM-32E is a powerful, generic Wi-Fi + Bluetooth + Bluetooth LE MCU module that targets a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

ESP32-DevKitC is a low-footprint and entry-level development board that is part of the ESP32 series. This board has a rich peripheral set. The built-in ESP32 pinout is optimized for hassle-free prototyping!

ESP32-WROOM-32E - Micro Processor

General purpose processors lack the bandwidth needed to perform complex tasks, so Xtensa LX6 processors are ideal for dealing with complex compute-intensive digital signal processing (DSP) applications. They are:

- **Configurable**: users are offered with pre-verified options ranging from memory size and width to complex DSP functions.
- **Extensible**: It is possible to implement datapath elements in the processor pipeline and add more I/Os.

The Xtensa LX6 processor contains a 32-bit base architecture. Its memories follow the Harvard model, with two separate memories one for data and the other for instructions. The processor pipeline can be selectable for 5-or-7 stages to accommodate different memory speeds. The type of instructions of this processor is VLIW (Very Long Instruction Word) which means that a fixed number of independent instructions formatted either as one large instruction, or a fixed instruction packet, are issued together. It was implemented the FLIX (Flexible Length Instruction eXtensions) technologie that allows for the definition of different size instructions (16- or 24-bit) rather than one fixed size for all instructions.

LX6 also features a 32 bit ALU, up to 64 physical registers and 6 special purpose registers. It contains 80 base instructions, and its ISA is backwards compatible. It also supports floating point (IEEE 754 single or double precision) operations.
There is support for caches (up to 128 kB) associated with data and instruction memories up to 4 way-set associative. There are also two units of load and store and the possibility of connecting memory banks for instruction and data access.

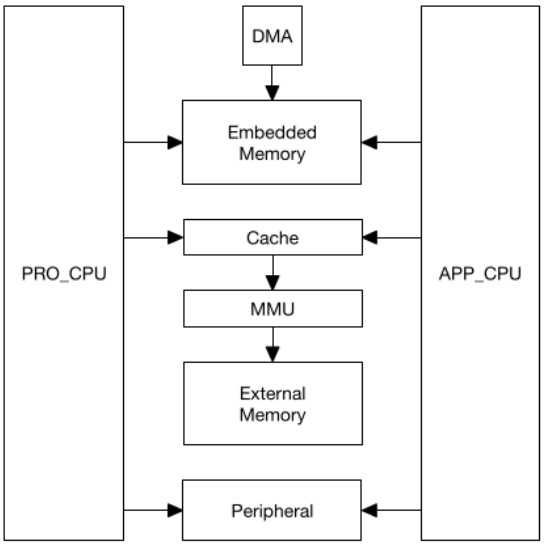
In terms of interruptions, this processor features up to 32 interrupts with 7 levels of priority, as well as specific registers to deal with these situations. To monitor peripherals, there are a series of GPIO ports accessible from the “outside”.

ESP32-WROOM-32E - System Structure and Memory

The ESP32 SoC, contains two Xtensa LX6 processors:

- **PRO_CPU** for dealing with protocols such as WiFi, Bluetooth and communication with peripherals.
- **APP_CPU** is more directed to application code.

Both of these processors are mapped symmetrically to the address space, however there are mechanisms to manage the switching between processors and the data exchanged between them.



In terms of memory there is two types of memory:

- Embedded memory on the chip
  - 448 kB of ROM and 520 kB of SRAM.
  - 8 kB of RTC FAST Memory and 8 kB of RTC SLOW Memory
- External memory
  - 16 MB of off-chip SPI Flash Memory and 8 MB of SPI-SRAM

ESP32-WROOM-32E - RTC Module

Designed to handle the entry into, and exit from, the low-power mode, and control the clock sources and power switch to generate power-gating, clock-gating, and reset signals.

It contains a FSM to record the power state, sleep and wake controllers to handle entry and exit from low power mode, an RTC timer and a ULP Co-Processor (Ultra Power). The ULP Co-Processor stays on during sleep mode and is able to wake the CPU and contains 16 general purpose registers for manipulating data and accessing memory. It can be a good supplement to, or replacement of, the CPU, especially for power-sensitive applications.

ESP32-WROOM-32E - Cryptographic Hardware Accelerator

Cryptographic hardware accelerators are optimized to execute cryptographic operations (very computationally intensive) in a more efficient way than if executed by a CPU. The ESP32 contains 3 accelerators one for each cryptographic function (AES, SHA and RSA). There is also a Random number generator that generates 32 bit random numbers to be used in cryptographic operations.
This modules can be used in Flash encryption or decryption in order to enhance hardware security.

ESP32-WROOM-32E - Peripherals

ESP 32 peripherals include:

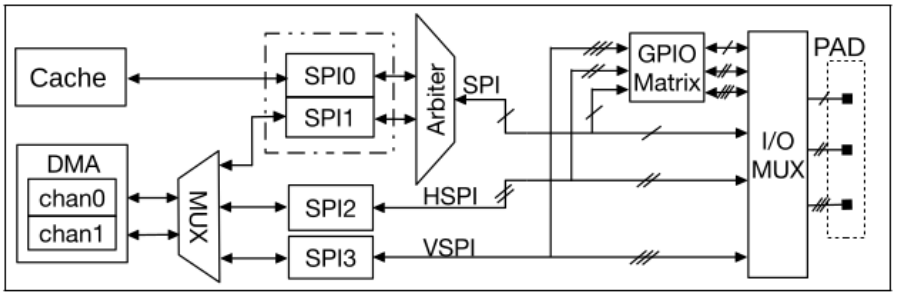
- 3 UART controllers, for exchanging data that need minimal system resources
- 2 I2S interfaces for streaming digital data in multimedia applications
- I2C bus for communication several external devices connected to the same bus as ESP32
- 4 SPI controllers to communicate with external devices that use the SPI protocol
- 3 Watchdog Timers (one in the RTC module)
- 4 General purpose 64 bit timers based in 16 bit prescalers
- 5 controllers dedicated to operating ADCs
- 2 8-bit DAC channels
- PWM peripheral for motor and power control. It provides six PWM outputs
- Ethernet PHY to send and receive data via Ethernet MAC
- Two sensors:
    - Touch (10 capacitive touch pads / GPIOs)
    - Hall effect sensor

ESP32 also features DMA for high-speed data transfer between peripherals and memory, as well as from memory to memory without any CPU intervention, thus allowing for more

efficient use of the cores when processing data. Supports half and full duplex data transfers. 13 peripherals are able to use DMA.

ESP32-WROOM-32E - SPI

ESP32 integrates four SPI controllers which can be used to communicate with external devices that use the SPI protocol.SPI0 can be used as a buffer for accessing external memory. SPI1 can be used as a master. SPI2 and SPI3 can be configured as either a master or a slave. SPI1, SPI2 and SPI3 share two DMA channels.



The SPI controller supports four-line full-duplex/half-duplex communication (MOSI, MISO, CS, and CLK lines) or three-line half-duplex-only communication (DATA, CS, and CLK lines).

There is also hardware support for two types of interruptions, SPI and SPI DMA interruptions.

ESP32-DevKitC

Generally is used in applications such as Prototyping of IoT devices, Low power battery operated applications, Network projects or projects requiring Multiple I/O interfaces with Wi-Fi and Bluetooth functionalities. The Kit features 34 physical GPIO, 2 buttons one for boot and another for resetting the device. In terms of power supplies there are 3 ways to power the kit there are three alternatives:

- Through USB-micro-USB port (preferably) (1),
- Through a regulated source using 3.3V and GND pins (2)
- Through unregulated source 5V and GND pins (3)

With the 3rd method, it is possible to power up to 12V but that causes massive heat dissipation and may over-heat the surroundings of the chip. The 2nd method is important

to provide only 3.3 V. This is because in this method the power supplied is not controlled internally in the chip and it will damage the chips permanently.

ESP32-DevKitC - Support for External RAM

ESP32 has a 520 kB of internal RAM, residing on the same die as the rest of the chip components. It can be insufficient for some purposes. So ESP32 has the ability to also use up to 4 MB of external SPI PSRAM (PseudoStatic RAM) memory.

Note: While ESP32 is capable of supporting several types of RAM chips, ESP-IDF currently only supports Espressif branded PSRAM chips (e.g., ESP-PSRAM32, ESP-PSRAM64, etc).

ESP-IDF fully supports the use of external RAM in applications. Once the external RAM is initialized at startup, ESP-IDF can be configured to integrate the external RAM in several ways like:

- Integrate RAM into the ESP32 Memory Map
- Add External RAM to the Capability Allocator
- Provide External RAM via malloc() (default)

Though external RAM as some restrictions like:

- When flash cache is disabled (for example, if the flash is being written to), the external RAM also becomes inaccessible; any reads from or writes to it will lead to an illegal cache access exception.

Bibliography

- **ESP32**
  - Xtensa LX6 Datasheet https://mirrobo.ru/wp-content/uploads/2016/11/Cadence_Tensillica_Xtensa_LX6_ds.pdf
  - ESP32 Technical Reference https://www.espressif.com/sites/default/files/documentation/esp32_technical_reference_manual_en.pdf
  - ESP32 Series Datasheet https://www.espressif.com/sites/default/files/documentation/esp32_datasheet_en.pdf
  - Overview of ESP32 features https://www.exploreembedded.com/wiki/Overview_of_ESP32_features._What_do_they_practically_mean%3F
- **ESP32-DevKitC**
  - ESP32 DevKit - Components101 https://components101.com/microcontrollers/esp32-devkitc
  - Support for external RAM - ESP-IDF Programming Guide https://docs.espressif.com/projects/esp-idf/en/latest/esp32/api-guides/external-ram.html
  - ESP32 - Dev kit power options - Tech Explorations https://techexplorations.com/guides/esp32/begin/power/