Assignment 1 – Cyclic Redundancy Check

Jorge Catarino (nº85028), Óscar Pimentel (nº80247)
Grupo 1 (P4) - ACA

Encoder - Our Approach

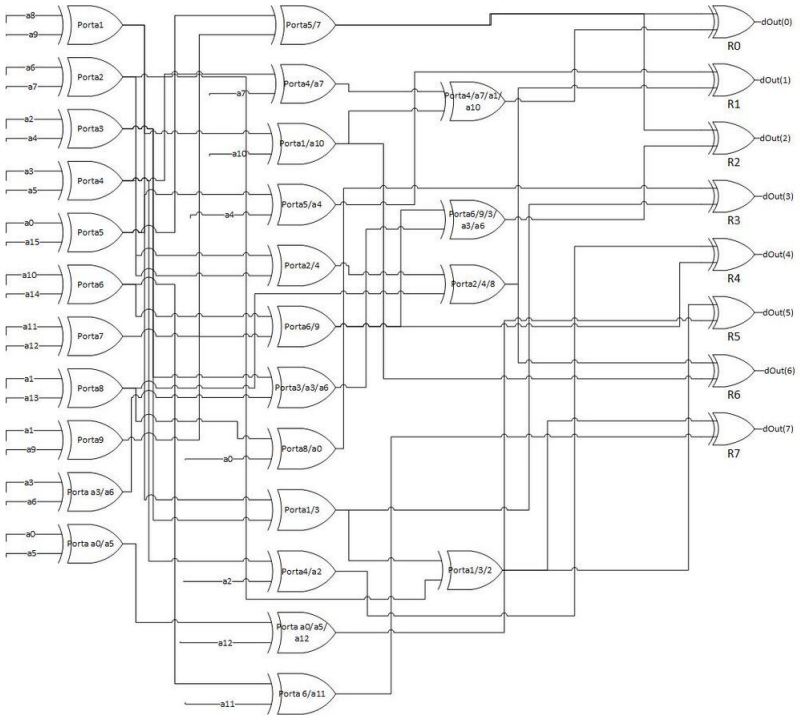
- Approach discussed in class - Properties of the Remainder:
  - 64 XOR gates needed;
  - 11 XOR propagation time delays in the worst case (r2);
- We took that basic solution and improved it by building a Parallel implementation:
  - we displayed the basic approach on a table and we found common groups of operations, therefore reducing the gate count;
  - we perform the operations in parallel, reducing the propagation time delays;

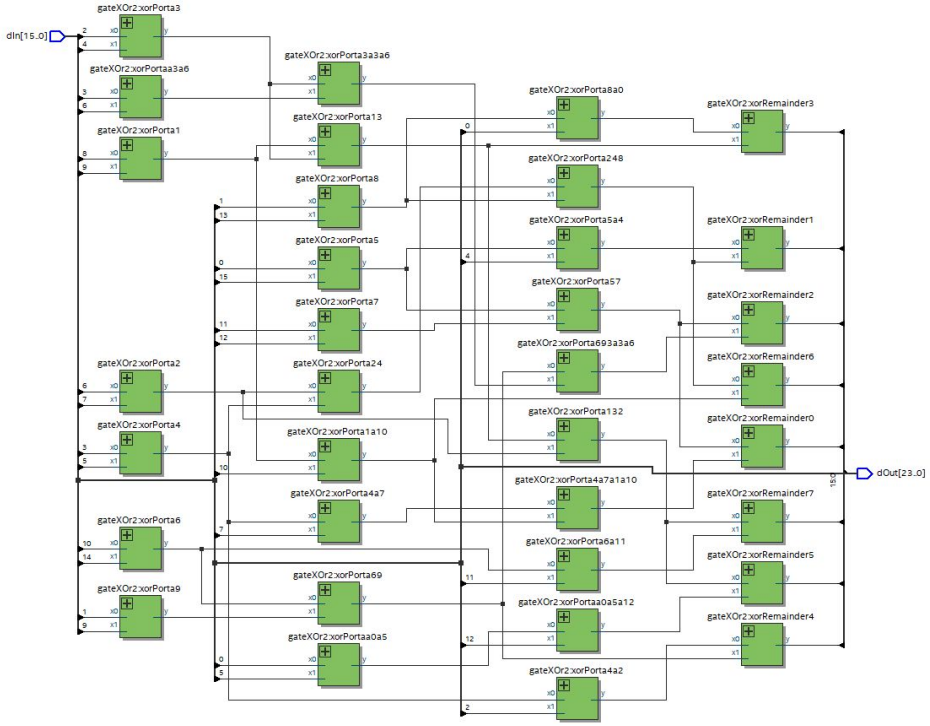
	r7	r6	r5	r4	r3	r2	r1	r0
a0			1		1	1	1	1
a1		1		1	1	1	1	
a2	1		1	1	1	1		
a3		1		1		1	1	1
a4	1		1		1	1	1	
a5		1	1	1			1	1
a6	1	1	1			1	1	
a7	1	1	1				1	1
a8	1	1	1		1			1
a9	1	1	1	1	1	1		1
a10	1	1		1		1		1
a11	1					1		1
a12			1			1		1
a13		1			1		1	
a14	1			1		1		
a15						1	1	1

5	Porta 1	a8, a9
4	Porta 2	a6, a7
4	Porta 3	a2, a4
4	Porta 4	a3, a5
3	Porta 5	a0, a15
3	Porta 6	a10, a14
2	Porta 7	a11, a12
3	Porta 8	a1, a13
2	Porta 9	a1, a9

Encoder - Results

- **Improved worst case propagation delay** -> 4 XOR propagation time delays (r0, r1, r2, r5, r6 and r7);
- **Improved gate count** -> 35 XOR gates;



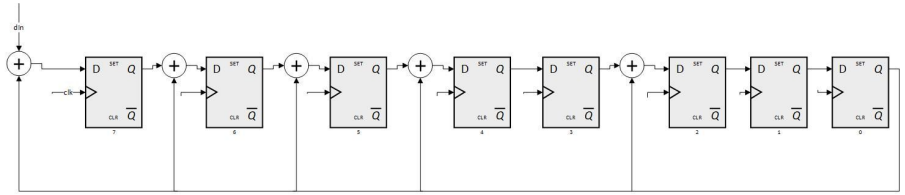


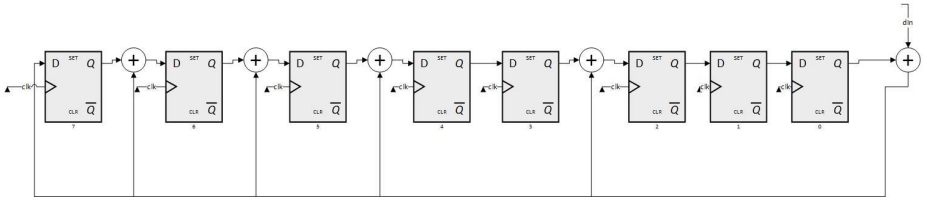
Checker - Our Approach

- Approach discussed in class - Division Algorithm:
  - When MSB is 0, shift left and bring the next bit down.
  - When MSB is 1, XOR with divisor and shift left.
  - With this algorithm, we can implement a bit-serial solution.

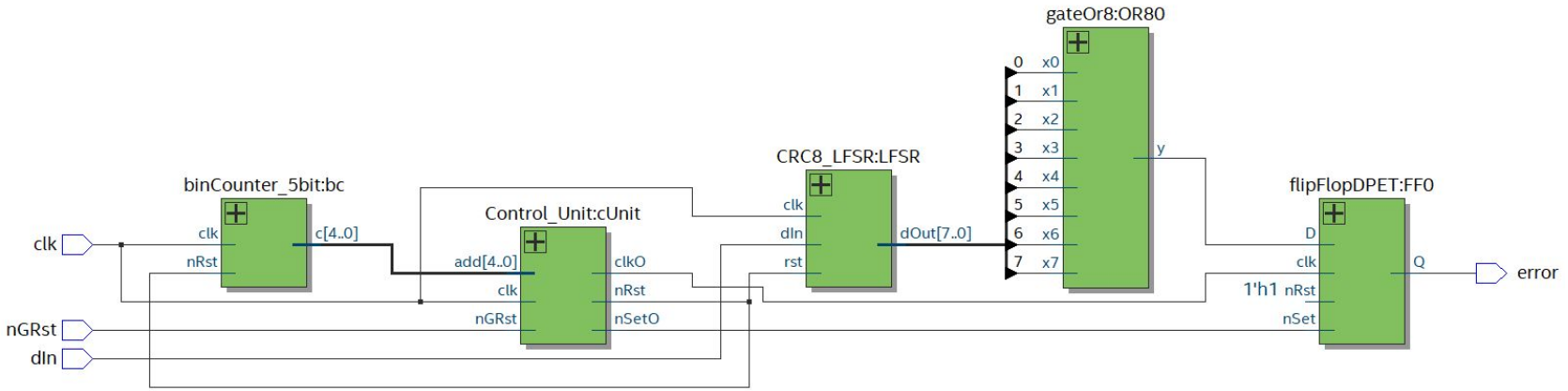
```
                0 0 0 0 1 0 1
            ┌──────────────────
10011       │ 1 0 1 1 0 0 1 0 0 0 0
            1 0 0 1 1
            ─────────
            0 0 1 0 1
              0 1 0 1 0
                1 0 1 0 1
                1 0 0 1 1
                ─────────
                0 0 1 0 0
```

- To implement this algorithm, we needed a shift register and a collection of modulo two adders (XOR). This module is called Linear Feedback Shift Register. With that we found two possible designs:





Checker - Results



- **Implementation Cost:**
  - 1 LFSR
    - 8 Flip-Flop D, 5 XOR gates ;
  - 1 5-bit Binary Counter
    - 5 Flip Flop D, 4 XOR gates, 3 AND gates ;
  - 1 Control Unit ;
    - 4 NAND gates, 1 NOR gate
  - 1 8-bit OR Gate;
  - 1 Flip-Flop D;
- **Operation time:**
  - 26 clock cycles (24+2);

References

- Culler, David. Lecture 26- LFSR, CRC's (and a little power). Fall 2004, https://www-inst.eecs.berkeley.edu/~cs150/archives.html. PowerPoint Presentation.
- W. W. Peterson and D. T. Brown, "Cyclic Codes for Error Detection," in Proceedings of the IRE, vol. 49, no. 1, pp. 228-235, Jan. 1961, doi: 10.1109/JRPROC.1961.287814.