**Notes on Vivado SystemVerilog Limitations**

| **Feature** | **Synthesis** |  | **Simulation** |
| --- | --- | --- | --- |
| logic | ✅ |  | ✅ |
| always\_comb, always\_ff, always\_latch | ✅ |  | ✅ |
| interface, modport, assert | ❌ |  | ✅ |
| initial blocks | ❌ |  | ✅ |
| Dynamic constructs (foreach, classes) | ❌ |  | ✅ |