TITLE:	A 20GHz Programmable Clock Delay Stage

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This subject is intended to be undertaken by students from:	**MEMN**	
	MEMAT	
	Any / Qualquer	X

ABSTRACT (for CLIP)

The design will be used in clock calibration to control the alignment of multi-phase clocks The goal of the project is to develop a circuit architecture that will meet the Target Performance requirements outlined below:

The Power Supply will be 0.9V (Typical);
The stage will be designed in a 3nm or 7nm CMOS technology;
The delay stage will be programmable with range of 10ps and a resolution of 10fs (~10-bit);
The design will have a DNL of +/- 1LSB and INL of +/-2LSB;
The buffer performance will be verified across PVT. The stage should be compatible with CMOS clocking amplitudes;
Apart from meeting the different performance targets, the buffer should also conform to 10 Year reliability requirements;
Design should be low area for ease of integrating multiple clock phases in a compact location.

DETAILED DESCRIPTION (for CLIP) (with chronogram)

The programmable clock delay stage is a crucial component in many high-speed digital and analog systems, particularly in clock generation circuits, timing adjustment, phase-locked loops (PLLs), and time-interleaved data converters (ADCs). The ability to introduce precise, programmable delays in clock signals at multi-GHz frequencies is essential for advanced communication systems and high-performance processors.

The goal of this project is to design and implement a 20 GHz programmable clock delay stage in FinFET CMOS technology. The proposed design can rely on current-starved inverters, shunt capacitors, or a combination of to achieve fine control over the delay. The project will explore different architectures and provide comparative analysis in terms of power consumption, jitter performance, delay range, and process variability.

Key Objectives:

1. Design a Programmable Delay Stage: Develop a delay circuit operating at 20 GHz with programmable delay steps.
2. Technology: Use FinFET CMOS technology (e.g., 16 nm or 7 nm process node) due to its advantages in terms of scalability, leakage control, and speed over traditional planar CMOS.
3. Achieve High Precision: The delay must be tunable with fine granularity (e.g., picosecond-level precision).

4. Low Power: Minimize power consumption to ensure efficiency, particularly for integration into larger systems (e.g., communication circuits, processors).
5. Analyze Key Metrics: Perform simulations to assess power dissipation, delay variation, phase noise, and jitter.
6. Process, Voltage, and Temperature (PVT) Variability: Ensure the design is robust under varying environmental conditions and process tolerances.

Approaches:

There are two primary design approaches that could be explored in this project:

1. Current-Starved Inverter Approach:
   - The current-starved inverter operates by limiting the current flowing through an inverter, allowing for programmable delay tuning.
   - In a basic current-starved inverter, additional transistors control the current flowing through the main inverter, thereby adjusting the switching speed of the circuit.
   - This method allows fine delay adjustments but requires careful design to ensure linearity and stable operation at high frequencies.
2. Shunt-Capacitor Approach:
   - The shunt-capacitor technique introduces an adjustable capacitive load at the output of the inverter stages. By varying the capacitance, the charging and discharging time of the output node can be adjusted, which in turn adjusts the delay.
   - This technique is straightforward and easy to implement, but care must be taken in managing parasitic capacitance and minimizing jitter caused by switching.

Time Planning:

The project is expected to be completed over the course of 6 months, with the following timeline:

Month 1: Literature Review & Project Specification

- Study the state-of-the-art techniques in high-speed clock delay circuits.
- Research the current-starved inverter and shunt-capacitor techniques.
- Define precise project requirements and success criteria.

Month 2: Initial Design & Architecture Selection

- Implement initial designs of current-starved inverters and shunt-capacitor-based delay stages in a standard simulation environment (e.g., Cadence Virtuoso or Synopsys).
- Simulate both architectures at lower frequencies to evaluate key metrics such as delay tunability, linearity, and power consumption.
- Select the optimal architecture based on the initial simulation results.

Month 3-4: High-Frequency Simulation (20 GHz)

- Scale up the design to operate at 20 GHz.
- Perform detailed simulations using SPICE models for FinFET CMOS, considering parasitics and interconnect effects.
- Investigate the impact of device sizing, transistor stacking, and power supply noise on delay performance.

Month 5-6: Optimization & PVT Variability Analysis

- Optimize the design for delay precision, power efficiency, and low jitter.
- Conduct simulations for PVT variations (process, voltage, temperature) to ensure the circuit's robustness.
- Explore compensation techniques if needed (e.g., adaptive biasing, feedback control).

References:

[1] Maymandi-Nejad, Mohammad & Sachdev, Mishal. (2003). A Digitally Programmable Delay Element: Design and Analysis. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on. 11. 871 - 878. 10.1109/TVLSI.2003.810787.
[2] S. Goyal *et al*., "Design Challenges and Techniques for 5nm FinFET CMOS Analog/Mixed-Signal Circuits," *2023 36th International Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID)*, Hyderabad, India, 2023, pp. 98-103, doi: 10.1109/VLSID57277.2023.00033.
[3] Abdulrazzaq, Bilal & Abdul Halin, Izhal & Kawahito, Shoji & Sidek, Roslina & Shafie, Suhaidi & Md Yunus, Nurul. (2016). A review on high-resolution CMOS delay lines: towards sub-picosecond jitter performance. SpringerPlus. 5. 10.1186/s40064-016-2090-z.
[4] Behzad Razavi, “Design of Integrated Circuits for Optical Communications,” Wiley, 2012.

By the conclusion of this MSc project, the student will have designed and simulated a high-speed programmable clock delay stage in advanced FinFET CMOS technology, addressing key challenges in modern high-frequency electronics.

SUPERVISORS (Affiliation): According to legislation, this number is limited to 2. If abroad, one supervisor must be internal to FCT NOVA.	João Carlos da Palma Goes (FCT NOVA); Marc Erett (Senior Director (AMD), Cork, Ireland.

VENUE:	AMD, Cork, Ireland.