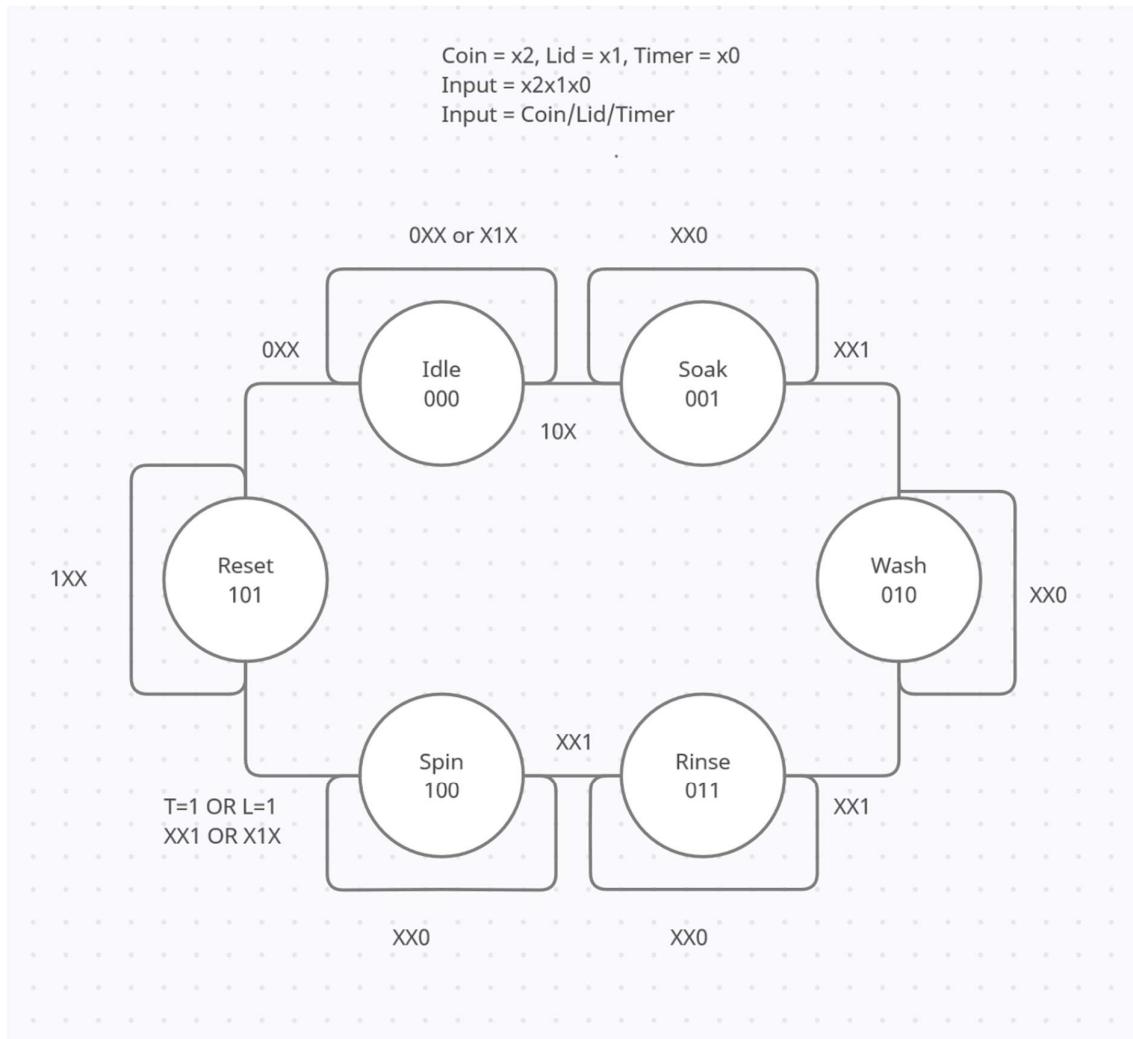


STATE MACHINE BELOW



The Idle state is a state where the User can put their laundry in and insert a coin to start the machine – It requires the door to be closed to start the machine. The next stage is Soak.

The Soak stage first soaks the laundry with water and will continue to the next stage once the timer has clocked. The next stage is Wash.

The Wash stage washes the laundry for the same amount of time as the previous stage – waiting for the timer to clock. The next stage is Rinse.

The Rinse stage will rinse and drain the water in the machine and transition to the next stage when the timer has clocked. The next stage is Spin.

The Spin stage is the final stage and will spin until the Lid is opened or the Timer is clocked. It will then transition to the Reset stage.

The Reset stage is crucial for two reasons. It will act as an idle stage for the machine when the Lid is opened or the Timer is clocked and will only transition to the next stage once the coin has reset. This is so that, if Spin went to Idle immediately, the machine could potentially start again into the

Soak stage if the Lid were opened/Timer clocked and the coin sensor had bugged and produced a reading. The reset stage will prevent that from happening. The reset stage will continue to the Idle stage once the coin sensor does not sense anything i.e., resets.

ASSUMPTIONS:

The CLK and Timer of the implementations can be taken control of in the Simulation rather than have it the Timer dependant on the CLK and the CLK at 100 MHz. This will make it easier to test the FSM.

Each FF will use AND, OR and Inverters – choice of implementation. The only NAND used is for the Structural Verilog code because I did not know what the inverter function was called. Instead I used a NAND as an inverter.

FSM table and minimization and assignment

State Table

Present State	Next State							
	$X_0X_1X_2$ (CLT)							
ABC	000	001	010	011	100	101	110	111
S_0 (Idle)	S_0 (Idle)	S_0 (Idle)	S_0 (Idle)	S_0 (Idle)	S_1 (Soak)	S_1 (Soak)	S_0 (Idle)	S_0 (Idle)
S_1 (Soak)	S_1 (Soak)	S_2 (Wash)	S_1 (Soak)	S_2 (Wash)	S_1 (Soak)	S_2 (Wash)	S_1 (Soak)	S_2 (Wash)
S_2 (Wash)	S_1 (Wash)	S_3 (Rinse)	S_2 (Wash)	S_3 (Rinse)	S_2 (Wash)	S_3 (Rinse)	S_2 (Wash)	S_3 (Rinse)
S_3 (Rinse)	S_2 (Rinse)	S_4 (Spin)	S_3 (Rinse)	S_4 (Spin)	S_3 (Rinse)	S_4 (Spin)	S_3 (Rinse)	S_4 (Spin)
S_4 (Spin)	S_3 (Spin)	S_5 (Reset)						
S_5 (Reset)	S_0 (Idle)	S_0 (Idle)	S_0 (Idle)	S_0 (Idle)	S_5 (Reset)	S_5 (Reset)	S_5 (Reset)	S_5 (Reset)

Minimization

S_1 (Soak)	$S_0=S_1, S_0=S_2, S_1=S_2$							
S_2 (Wash)	$S_0=S_2, S_0=S_3, S_1=S_3, S_1=S_2$	$S_1=S_2, S_2=S_3$						
S_3 (Rinse)	$S_0=S_3, S_0=S_4, S_1=S_4, S_1=S_3$	$S_1=S_3, S_2=S_4$	$S_2=S_3, S_3=S_4$					
S_4 (Spin)	$S_0=S_4, S_0=S_5, S_1=S_5, S_1=S_4$	$S_1=S_4, S_2=S_5, S_1=S_5$	$S_2=S_4, S_3=S_5, S_2=S_5$	$S_3=S_4, S_4=S_5, S_3=S_5$				
S_5 (Reset)	$S_0=S_5, S_1=S_5$	$S_1=S_0, S_2=S_0, S_1=S_5, S_2=S_5$	$S_2=S_0, S_3=S_0, S_2=S_5, S_3=S_5$	$S_3=S_0, S_4=S_0, S_3=S_5, S_4=S_5$	$S_4=S_0, S_5=S_0, S_4=S_5$			
	S_0 (Idle)	S_1 (Soak)	S_2 (Wash)	S_3 (Rinse)	S_4 (Spin)			

No state minimization can occur because no dependency is satisfied i.e. not one state is equal to another.

State Assignment

Present State	Next State							
	$X_0X_1X_2$ (CLT)							
ABC	000	001	010	011	100	101	110	111
000 (Idle)	000 (Idle)	000 (Idle)	000 (Idle)	000 (Idle)	001 (Soak)	001 (Soak)	000 (Idle)	000 (Idle)
001 (Soak)	001 (Soak)	010 (Wash)	001 (Soak)	010 (Wash)	001 (Soak)	010 (Wash)	001 (Soak)	010 (Wash)
010 (Wash)	010 (Wash)	011 (Rinse)	010 (Wash)	011 (Rinse)	010 (Wash)	011 (Rinse)	010 (Wash)	011 (Rinse)
011 (Rinse)	011 (Rinse)	100 (Spin)	011 (Rinse)	100 (Spin)	011 (Rinse)	100 (Spin)	011 (Rinse)	100 (Spin)
100 (Spin)	100 (Spin)	101 (Reset)	101 (Reset)	101 (Reset)	100 (Spin)	101 (Reset)	101 (Reset)	101 (Reset)
101 (Reset)	000 (Idle)	000 (Idle)	000 (Idle)	000 (Idle)	101 (Reset)	101 (Reset)	101 (Reset)	101 (Reset)

D-FF Implementation

Truth Table

A	B	C	D	E	F	X	Y	Z	C	L	T	X(t+1)	Y(t+1)	Z(t+1)	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
2	0	0	0	0	1	0	0	0	0	1	0	0	0	0	2
3	0	0	0	0	1	1	0	0	0	1	1	0	0	0	3
4	0	0	0	1	0	0	0	0	0	0	0	0	0	1	4
5	0	0	0	1	0	1	0	0	0	1	0	0	0	1	5
6	0	0	0	1	1	1	0	0	0	0	0	0	0	0	6
7	0	0	0	1	1	1	1	0	0	0	1	0	0	0	7
8	0	0	1	0	0	0	0	0	0	0	0	0	0	1	8
9	0	0	1	0	0	0	0	1	0	0	1	0	0	0	9
10	0	0	1	0	1	0	0	0	0	1	0	0	1	0	10
11	0	0	1	0	1	1	0	1	0	1	1	0	1	0	11
12	0	0	1	1	0	0	0	0	0	0	0	0	1	0	12
13	0	0	1	1	0	0	0	1	0	0	1	0	1	0	13
14	0	0	1	1	1	0	0	0	0	0	0	0	0	1	14
15	0	0	1	1	1	1	0	1	0	1	1	0	1	0	15
16	0	1	0	0	0	0	0	0	0	0	0	0	1	0	16
17	0	1	0	0	0	0	0	1	0	0	1	0	1	1	17
18	0	1	0	0	1	0	0	0	0	1	0	0	1	0	18
19	0	1	0	0	1	1	0	1	0	1	1	0	1	1	19
20	0	1	0	1	0	0	0	0	0	1	0	0	1	0	20
21	0	1	0	1	0	0	0	1	0	1	0	0	1	1	21
22	0	1	0	1	1	0	0	0	0	0	1	0	1	0	22
23	0	1	0	1	1	1	0	1	0	1	1	0	1	1	23
24	0	1	1	0	0	0	0	0	0	0	0	0	1	1	24
25	0	1	1	0	0	0	0	1	0	1	0	0	0	0	25
26	0	1	1	0	0	1	0	0	0	0	1	1	1	1	26
27	0	1	1	0	1	0	0	1	0	1	1	0	0	0	27
28	0	1	1	1	0	0	0	0	0	0	1	0	1	1	28
29	0	1	1	1	0	0	0	1	0	1	0	0	0	0	29
30	0	1	1	1	1	0	0	0	0	0	1	1	1	1	30
31	0	1	1	1	1	1	0	1	0	1	1	0	0	0	31
32	1	0	0	0	0	0	0	0	1	0	0	0	0	0	32
33	1	0	0	0	0	0	0	1	1	0	1	0	1	1	33
34	1	0	0	0	1	0	0	0	1	0	0	1	0	1	34
35	1	0	0	0	1	1	0	1	1	0	0	1	0	1	35
36	1	0	0	1	0	0	0	0	1	0	0	0	0	0	36
37	1	0	0	1	0	0	0	1	1	0	0	1	0	1	37
38	1	0	0	1	1	0	0	0	1	0	0	1	0	1	38
39	1	0	0	1	1	1	0	1	1	0	0	1	0	1	39
40	1	0	1	0	0	0	0	0	0	0	0	0	0	0	40
41	1	0	1	0	0	0	0	1	0	0	0	0	0	0	41
42	1	0	1	0	1	0	0	0	0	0	0	0	0	0	42
43	1	0	1	0	1	1	0	1	0	0	0	0	0	0	43
44	1	0	1	1	0	0	0	0	1	0	0	1	0	0	44
45	1	0	1	1	0	0	0	1	1	0	0	1	0	1	45
46	1	0	1	1	1	0	0	0	1	0	0	1	0	1	46
47	1	0	1	1	1	1	0	1	1	0	0	1	0	1	47
48	1	1	0	0	0	0	0	0	X	X	X	X	X	X	48
49	1	1	0	0	0	0	0	1	X	X	X	X	X	X	49
50	1	1	0	0	0	1	0	0	X	X	X	X	X	X	50
51	1	1	0	0	0	1	1	0	X	X	X	X	X	X	51
52	1	1	0	1	0	0	0	0	X	X	X	X	X	X	52
53	1	1	0	1	0	0	1	0	X	X	X	X	X	X	53
54	1	1	0	1	1	0	0	0	X	X	X	X	X	X	54
55	1	1	0	1	1	1	0	1	X	X	X	X	X	X	55
56	1	1	1	0	0	0	0	0	X	X	X	X	X	X	56
57	1	1	1	0	0	0	0	1	X	X	X	X	X	X	57
58	1	1	1	0	1	0	0	0	X	X	X	X	X	X	58
59	1	1	1	0	1	0	1	0	X	X	X	X	X	X	59
60	1	1	1	1	0	0	0	0	X	X	X	X	X	X	60
61	1	1	1	1	0	0	1	0	X	X	X	X	X	X	61
62	1	1	1	1	1	0	0	0	X	X	X	X	X	X	62
63	1	1	1	1	1	1	0	1	X	X	X	X	X	X	63

K-Map for Da, Dx or X(T+1).

Map							
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.\bar{F}$	$D.E.F$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C$	0	0	0	0	0	0	0
$\bar{A}.B.C$	0	1	1	0	0	1	1
$A.B.\bar{C}$	0	0	0	0	0	0	0
$A.\bar{B}.\bar{C}$	1	1	1	1	1	1	1
$A.\bar{B}.C$	0	0	0	0	1	1	1
$A.B.C$	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(AC')

(AD)

(BCF)

$$X(t+1) = AC' + AD + BCF$$

K-Map for Db, Dy or Y(T+1).

Map							
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.\bar{F}$	$D.E.F$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C$	0	1	1	0	0	1	1
$\bar{A}.B.C$	1	0	0	1	1	0	0
$A.B.\bar{C}$	1	1	1	1	1	1	1
$A.\bar{B}.\bar{C}$	0	0	0	0	0	0	0
$A.\bar{B}.C$	0	0	0	0	0	0	0
$A.B.C$	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(BC')

(BF')

(A'B'CF)

$$Y(t+1) = BC' + BF' + A'B'CF$$

	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}EF$	$\bar{D}E\bar{F}$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$	$D\bar{E}\bar{F}$
$\bar{A}\bar{B}\bar{C}$	0	0	0	0	1	1	0	0
$\bar{A}\bar{B}C$	1	0	0	1	1	0	0	1
$\bar{A}BC$	1	0	0	1	1	0	0	1
$A\bar{B}\bar{C}$	0	1	1	0	0	1	1	0
$A\bar{B}\bar{C}$	0	1	1	1	0	1	1	1
$A\bar{B}C$	0	0	0	0	1	1	1	1
ABC	x	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	x	x	x	x	x	x	x	x

Prime Implicants include:

(A'CF') - Essential Prime Implicant

(CDF')

(BC'F - Essential Prime Implicant

(BCF')

(AC'F) - Essential Prime Implicant

(AC'E) - Essential Prime Implicant

(ADF)

(ADE)

(ACD) - Essential Prime Implicant

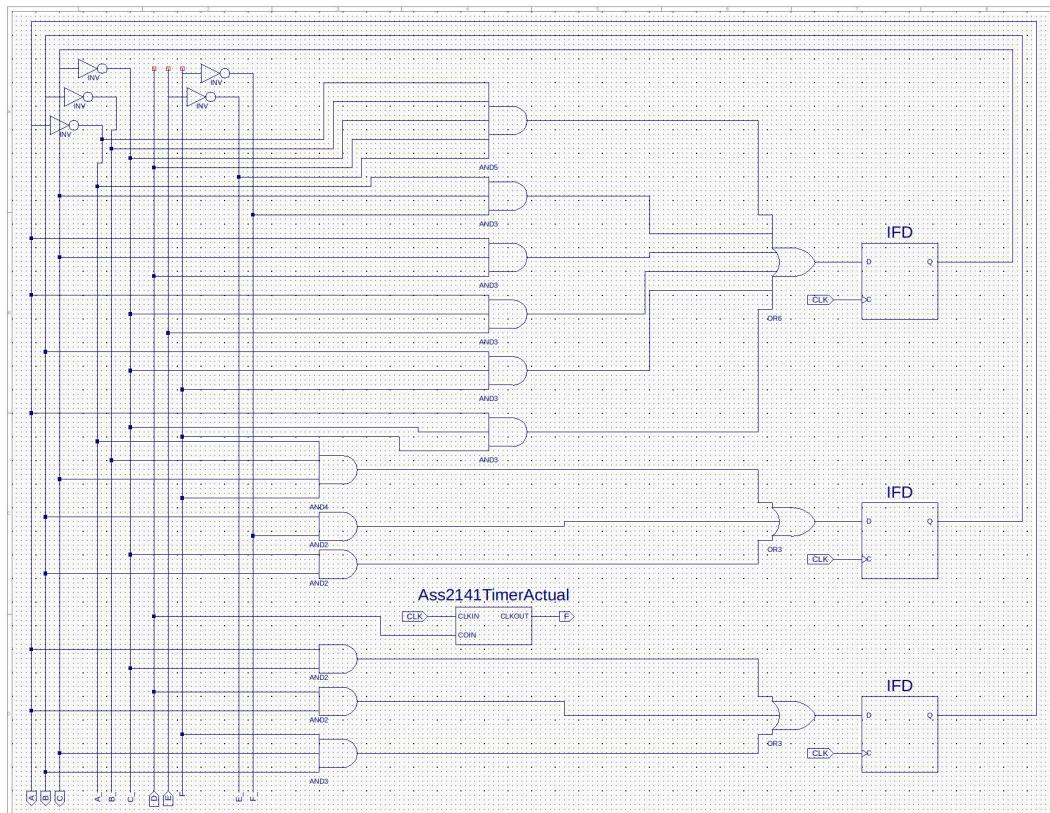
(C'DE'F)

(A'B'C'DE') - Essential Prime Implicant

(A'B'DE'F')

$$Z(t+1) = A'CF' + ACD + AC'E + BC'F + AC'F + A'B'C'DE'$$

D-Flip Flop Logic Diagram/Schematic



```
1 timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 04:07:51 04/15/2021
7 // Design Name:
8 // Module Name: Ass2141TimerActual
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module Ass2141TimerActual(
22     input CLKIN,
23     input COIN,
24     output reg CLKOUT
25 );
26
27 reg [28:0] counter;
28
29 parameter C0 = 29'd400000000;
30
31 always@(posedge CLKIN) begin
32     if(COIN == 1)begin
33
34         if(CLKOUT == 1)begin
35             CLKOUT <= ~CLKOUT;
36         end
37
38         counter <= counter + 1;
39
40         if(counter == C0)begin
41             CLKOUT <= ~CLKOUT;
42             counter <= 0;
43         end
44     end
45
46
47     else begin
48         counter <= 0;
49     end
50
51 end
52
53 endmodule
54
```

GIC = 3+2+5+3+3+3+3+4+2+2+2+2+3+3+3+6 = 52 from above schematic

T-FF Implementation

Present State			Input	Next State			Flip-Flop Inputs			
A	B	C	DEF	A(t+1)	B(t+1)	C(t+1)	T _a	T _b	T _c	
0	0	0	000	0	0	0	0	0	0	0
1	0	0	001	0	0	0	0	0	0	1
2	0	0	010	0	0	0	0	0	0	2
3	0	0	011	0	0	0	0	0	0	3
4	0	0	100	0	0	1	0	0	1	4
5	0	0	101	0	0	1	0	0	1	5
6	0	0	110	0	0	0	0	0	0	6
7	0	0	111	0	0	0	0	0	0	7
8	0	1	000	0	0	1	0	0	0	8
9	0	1	001	0	1	0	0	1	1	9
10	0	1	010	0	0	1	0	0	0	10
11	0	1	011	0	1	0	0	1	1	11
12	0	1	100	0	0	1	0	0	0	12
13	0	1	101	0	1	0	0	1	1	13
14	0	1	110	0	0	1	0	0	0	14
15	0	1	111	0	1	0	0	1	1	15
16	1	0	000	0	1	0	0	0	0	16
17	1	0	001	0	1	1	0	0	1	17
18	1	0	010	0	1	0	0	0	0	18
19	1	0	011	0	1	1	0	0	1	19
20	1	0	100	0	1	0	0	0	0	20
21	1	0	101	0	1	1	0	0	1	21
22	1	0	110	0	1	0	0	0	0	22
23	1	0	111	0	1	1	0	0	1	23
24	1	1	000	0	1	1	0	0	0	24
25	1	1	001	1	0	0	1	1	1	25
26	1	1	010	0	1	1	0	0	0	26
27	1	1	011	1	0	0	1	1	1	27
28	1	1	100	0	1	1	0	0	0	28
29	1	1	101	1	0	0	1	1	1	29
30	1	1	110	0	1	1	0	0	0	30
31	1	1	111	1	0	0	1	1	1	31
32	1	0	000	1	0	0	0	0	0	32
33	1	0	001	1	0	1	0	0	1	33
34	1	0	010	1	0	1	0	0	1	34
35	1	0	011	1	0	1	0	0	1	35
36	1	0	100	1	0	0	0	0	0	36
37	1	0	101	1	0	1	0	0	1	37
38	1	0	110	1	0	1	0	0	1	38
39	1	0	111	1	0	1	0	0	1	39
40	1	0	000	0	0	0	1	0	1	40
41	1	0	001	0	0	0	1	0	1	41
42	1	0	010	0	0	0	1	0	1	42
43	1	0	011	0	0	0	1	0	1	43
44	1	0	100	1	0	1	0	0	0	44
45	1	0	101	1	0	1	0	0	0	45
46	1	0	110	1	0	1	0	0	0	46
47	1	0	111	1	0	1	0	0	0	47

K-Map for T_a

Map								
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C$	0	0	0	0	0	0	0	0
$\bar{A}.B.C$	0	1	1	0	0	1	1	0
$\bar{A}.B.\bar{C}$	0	0	0	0	0	0	0	0
$A.\bar{B}.\bar{C}$	0	0	0	0	0	0	0	0
$A.\bar{B}.C$	1	1	1	1	0	0	0	0
$A.B.C$	x	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(BCF)

(ACD')

$$T_a = BCF + ACD'$$

K-Map for T_b

Map								
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	0	0	0	0
$\bar{A}.\bar{B}.C$	0	1	1	0	0	1	1	0
$\bar{A}.B.C$	0	1	1	0	0	1	1	0
$\bar{A}.B.\bar{C}$	0	0	0	0	0	0	0	0
$A.\bar{B}.\bar{C}$	0	0	0	0	0	0	0	0
$A.\bar{B}.C$	0	0	0	0	0	0	0	0
$A.B.C$	x	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x	x

Prime Implicants include:

(A'CF) – Essential Prime Implicant

(BCF)

$$T_b = A'CF$$

K-Map for T_c

Map								
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	1	1	0	0
$\bar{A}.\bar{B}.C$	0	1	1	0	0	1	1	0
$\bar{A}.B.C$	0	1	1	0	0	1	1	0
$A.B.\bar{C}$	0	1	1	0	0	1	1	0
$A.\bar{B}.\bar{C}$	0	1	1	1	0	1	1	1
$A.\bar{B}.C$	1	1	1	1	0	0	0	0
$A.B.C$	x	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x	x

Prime Implicants include:

(BF) – Essential Prime Implicant

(A'CF) – Essential Prime Implicant

(CD'F)

(AC'F) – Essential Prime Implicant

(AD'F)

(AC'E) – Essential Prime Implicant

(AD'E)

(ACD') – Essential Prime Implicant

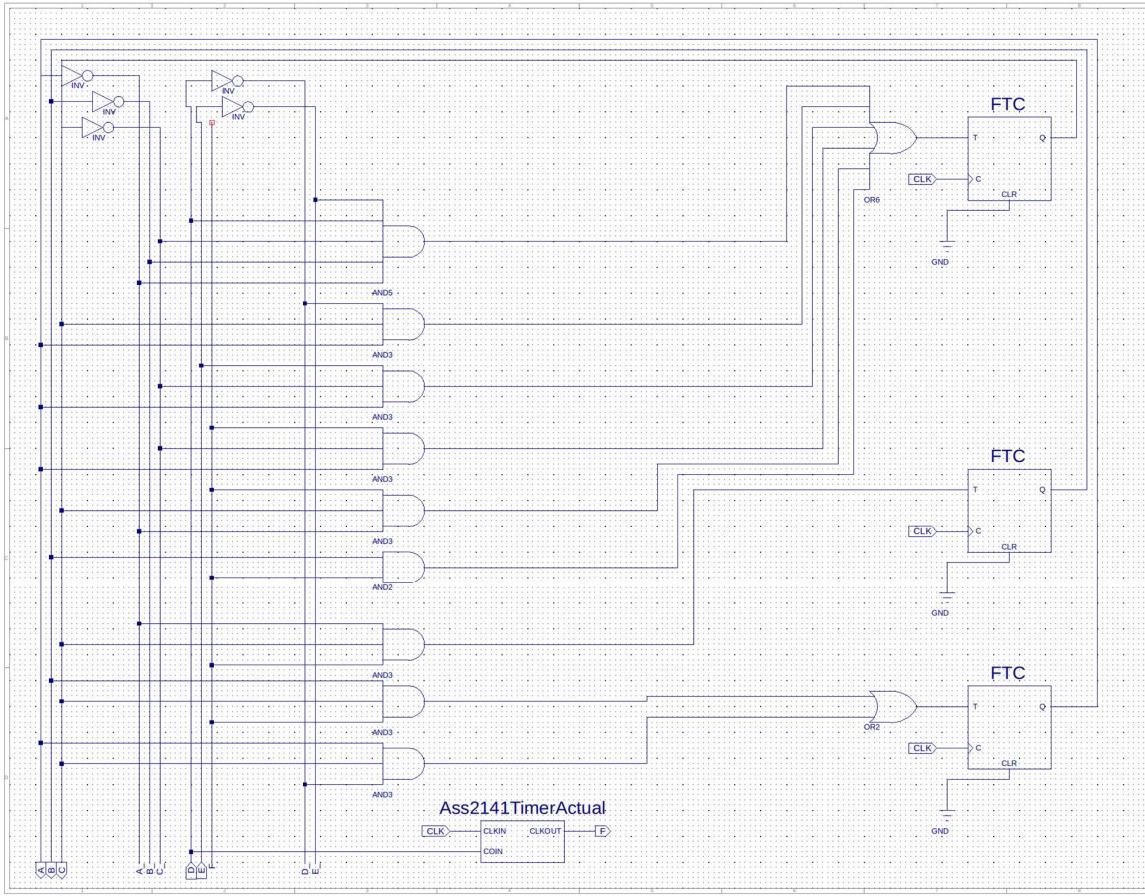
(A'DE'F)

(C'DE'F)

(A'B'C'DE') – Essential Prime Implicant

$$T_c = BF + A'CF + AC'F + AC'E + ACD' + A'B'C'DE'$$

GIC is $3+2+5+3+3+3+2+3+3+3+2+6 = 41$ from below schematic.



```

1  timescale ins / ips
2  ///////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 11:47:51 04/16/2021
7  // Design Name:
8  // Module Name: Ass2141TimerActual
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module Ass2141TimerActual(
22   input CLKIN,
23   input COIN,
24   output reg CLKOUT
25 );
26 reg [28:0] counter;
27
28 parameter C0 = 29'd400000000;
29
30 always@(posedge CLKIN) begin
31   if(COIN == 1) begin
32     if(CLKOUT == 1) begin
33       CLKOUT <= ~CLKOUT;
34     end
35
36     counter <= counter + 1;
37
38     if(counter == C0) begin
39       CLKOUT <= ~CLKOUT;
40       counter <= 0;
41     end
42   end
43
44   else begin
45     counter <= 0;
46   end
47 end
48
49 endmodule

```

J-K-FF Implementation - Verification

J-K State table

Present State			Input	Next State			Flip-Flop Inputs						
A	B	C	DEF	A(t+1)	B(t+1)	C(t+1)	J_a	K_a	J_b	K_b	J_c	K_c	
0	0	0	000	0	0	0	0	X	0	X	0	X	0
1	0	0	001	0	0	0	0	X	0	X	0	X	1
2	0	0	010	0	0	0	0	X	0	X	0	X	2
3	0	0	011	0	0	0	0	X	0	X	0	X	3
4	0	0	100	0	0	1	0	X	0	X	1	X	4
5	0	0	101	0	0	1	0	X	0	X	1	X	5
6	0	0	110	0	0	0	0	X	0	X	0	X	6
7	0	0	111	0	0	0	0	X	0	X	0	X	7
8	0	1	000	0	0	1	0	X	0	X	X	0	8
9	0	1	001	0	1	0	0	X	1	X	X	1	9
10	0	1	010	0	0	1	0	X	0	X	X	0	10
11	0	1	011	0	1	0	0	X	1	X	X	1	11
12	0	1	100	0	0	1	0	X	0	X	X	0	12
13	0	1	101	0	1	0	0	X	1	X	X	1	13
14	0	1	110	0	0	1	0	X	0	X	X	0	14
15	0	1	111	0	1	0	0	X	1	X	X	1	15
16	1	0	000	0	1	0	0	X	X	0	0	X	16
17	1	0	001	0	1	1	0	X	X	0	1	X	17
18	1	0	010	0	1	0	0	X	X	0	0	X	18
19	1	0	011	0	1	1	0	X	X	0	1	X	19
20	1	0	100	0	1	0	0	X	X	0	0	X	20
21	1	0	101	0	1	1	0	X	X	0	1	X	21
22	1	0	110	0	1	0	0	X	X	0	0	X	22
23	1	0	111	0	1	1	0	X	X	0	1	X	23
24	1	1	000	0	1	1	0	X	X	0	X	0	24
25	1	1	001	1	0	0	1	X	X	1	X	1	25
26	1	1	010	0	1	1	0	X	X	0	X	0	26
27	1	1	011	1	0	0	1	X	X	1	X	1	27
28	1	1	100	0	1	1	0	X	X	0	X	0	28
29	1	1	101	1	0	0	1	X	X	1	X	1	29
30	1	1	110	0	1	1	0	X	X	0	X	0	30
31	1	1	111	1	0	0	1	X	X	1	X	1	31
32	1	0	000	1	0	0	X	0	0	X	0	X	32
33	1	0	001	1	0	1	X	0	0	X	1	X	33
34	1	0	010	1	0	1	X	0	0	X	1	X	34
35	1	0	011	1	0	1	X	0	0	X	1	X	35
36	1	0	100	1	0	0	X	0	0	X	0	X	36
37	1	0	101	1	0	1	X	0	0	X	1	X	37
38	1	0	110	1	0	1	X	0	0	X	1	X	38
39	1	0	111	1	0	1	X	0	0	X	1	X	39
40	1	0	000	0	0	0	X	1	0	X	X	1	40
41	1	0	001	0	0	0	X	1	0	X	X	1	41
42	1	0	010	0	0	0	X	1	0	X	X	1	42
43	1	0	011	0	0	0	X	1	0	X	X	1	43
44	1	0	100	1	0	1	X	0	0	X	X	0	44
45	1	0	101	1	0	1	X	0	0	X	X	0	45
46	1	0	110	1	0	1	X	0	0	X	X	0	46
47	1	0	111	1	0	1	X	0	0	X	X	0	47

K-Map for J_a

Map							
	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}EF$	$\bar{D}E\bar{F}$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$
$\bar{A}\bar{B}\bar{C}$	0	0	0	0	0	0	0
$\bar{A}\bar{B}C$	0	0	0	0	0	0	0
$\bar{A}B\bar{C}$	0	1	1	0	0	1	1
$A\bar{B}\bar{C}$	0	0	0	0	0	0	0
$A\bar{B}\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}C$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(BCF)

$J_a = BCF$

K-Map for K_a

Map							
	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}EF$	$\bar{D}E\bar{F}$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$
$\bar{A}\bar{B}\bar{C}$	x	x	x	x	x	x	x
$\bar{A}\bar{B}C$	x	x	x	x	x	x	x
$\bar{A}B\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	0	0	0	0	0	0	0
$A\bar{B}C$	1	1	1	1	0	0	0
$AB\bar{C}$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(CD')

$K_a = (CD')$

K-Map for J_b

Map							
	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}EF$	$\bar{D}E\bar{F}$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$
$\bar{A}\bar{B}\bar{C}$	0	0	0	0	0	0	0
$\bar{A}\bar{B}C$	0	1	1	0	0	1	1
$\bar{A}B\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	0	0	0	0	0	0	0
$A\bar{B}C$	0	0	0	0	0	0	0
$AB\bar{C}$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(A'CF)

$$J_b = A'CF$$

K-Map for K_b

Map							
	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}EF$	$\bar{D}E\bar{F}$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$
$\bar{A}\bar{B}\bar{C}$	x	x	x	x	x	x	x
$\bar{A}\bar{B}C$	x	x	x	x	x	x	x
$\bar{A}B\bar{C}$	0	1	1	0	0	1	1
$A\bar{B}\bar{C}$	0	0	0	0	0	0	0
$A\bar{B}\bar{C}$	x	x	x	x	x	x	x
$A\bar{B}C$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include – Also the essential Prime Implicants:

(CF)

$$K_b = CF$$

K-Map for J_c

Map								
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	0	0	0	1	1	0	0
$\bar{A}.\bar{B}.C$	x	x	x	x	x	x	x	x
$\bar{A}.B.C$	x	x	x	x	x	x	x	x
$A.B.\bar{C}$	0	1	1	0	0	1	1	0
$A.\bar{B}.\bar{C}$	0	1	1	1	0	1	1	1
$A.\bar{B}.C$	x	x	x	x	x	x	x	x
$A.B.C$	x	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x	x

Prime Implicants include:

(BF) - Essential Prime Implicant

(AF) - Essential Prime Implicant

(AE) - Essential Prime Implicant

(DE'F)

(A'B'DE') - Essential Prime Implicant

$$J_c = BF + AF + AE + A'B'DE'$$

K-Map for K_c

Map							
	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$D.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$
$\bar{A}.\bar{B}.\bar{C}$	x	x	x	x	x	x	x
$\bar{A}.\bar{B}.C$	0	1	1	0	0	1	1
$\bar{A}.B.C$	0	1	1	0	0	1	1
$A.B.\bar{C}$	x	x	x	x	x	x	x
$A.\bar{B}.\bar{C}$	x	x	x	x	x	x	x
$A.\bar{B}.C$	1	1	1	1	0	0	0
$A.B.C$	x	x	x	x	x	x	x
$A.B.\bar{C}$	x	x	x	x	x	x	x

Prime Implicants include:

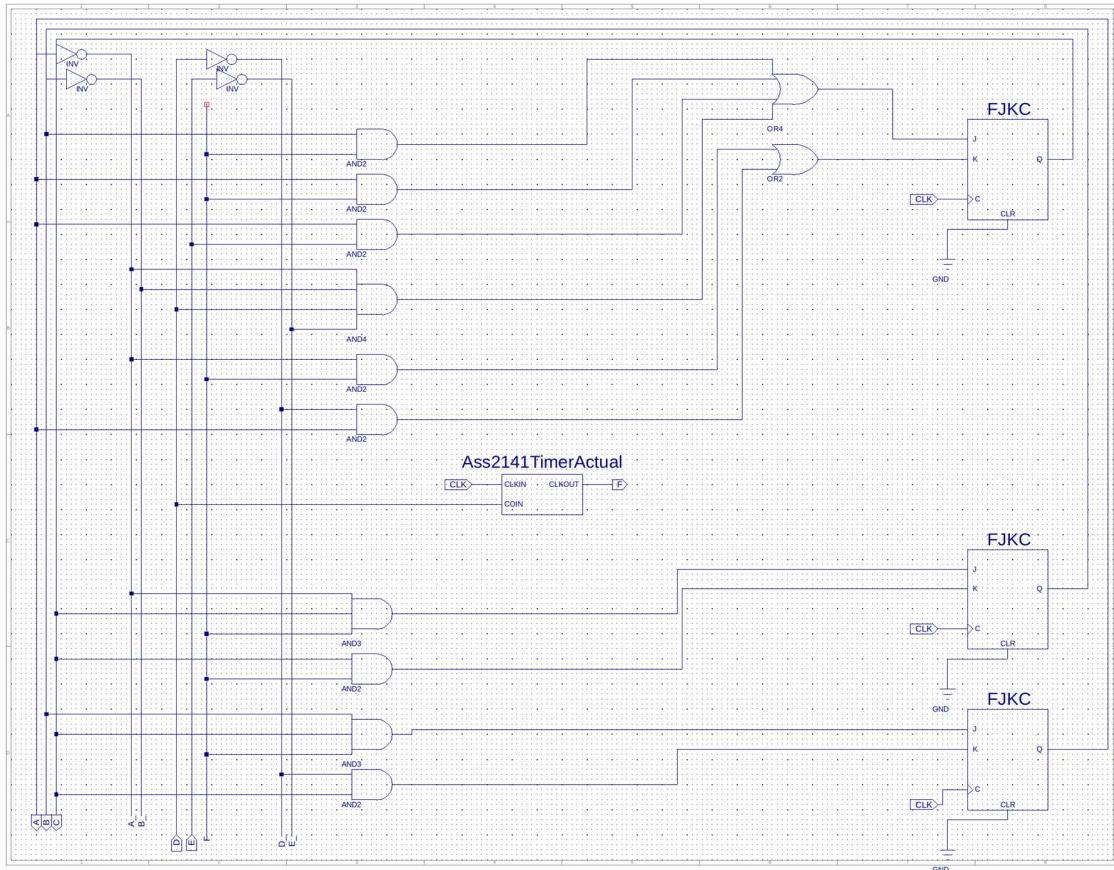
(A'F) - Essential Prime Implicant

(D'F)

(BF)

(AD') - Essential Prime Implicant

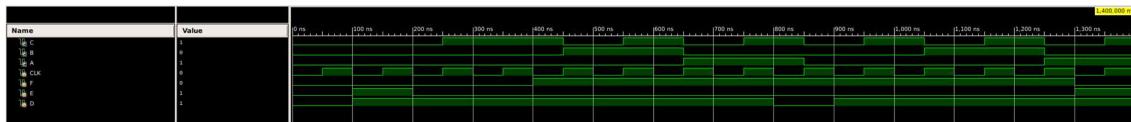
$$K_c = A'F + AD'$$



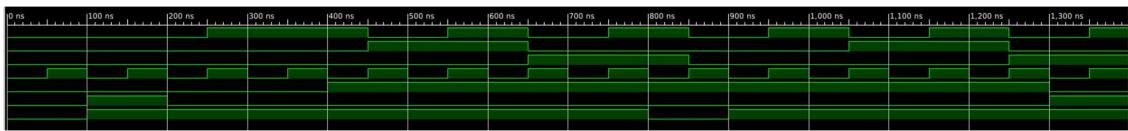
```

1  timescale ins / ips
2  ///////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    12:50:18 04/16/2021
7  // Design Name:
8  // Module Name:   Ass2141TimerActual
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module Ass2141timerActual(
22     input CLKIN,
23     input COIN,
24     output reg CLKOUT
25 );
26
27 reg [28:0] counter;
28
29 parameter C0 = 29'd400000000;
30
31 always@(posedge CLKIN) begin
32     if(COIN == 1) begin
33         if(CLKOUT == 1) begin
34             CLKOUT <= ~CLKOUT;
35         end
36         counter <= counter + 1;
37
38         if(counter == C0) begin
39             CLKOUT <= ~CLKOUT;
40             counter <= 0;
41         end
42     end
43 end
44
45 else begin
46     counter <= 0;
47 end
48 end
49
50 endmodule
51

```

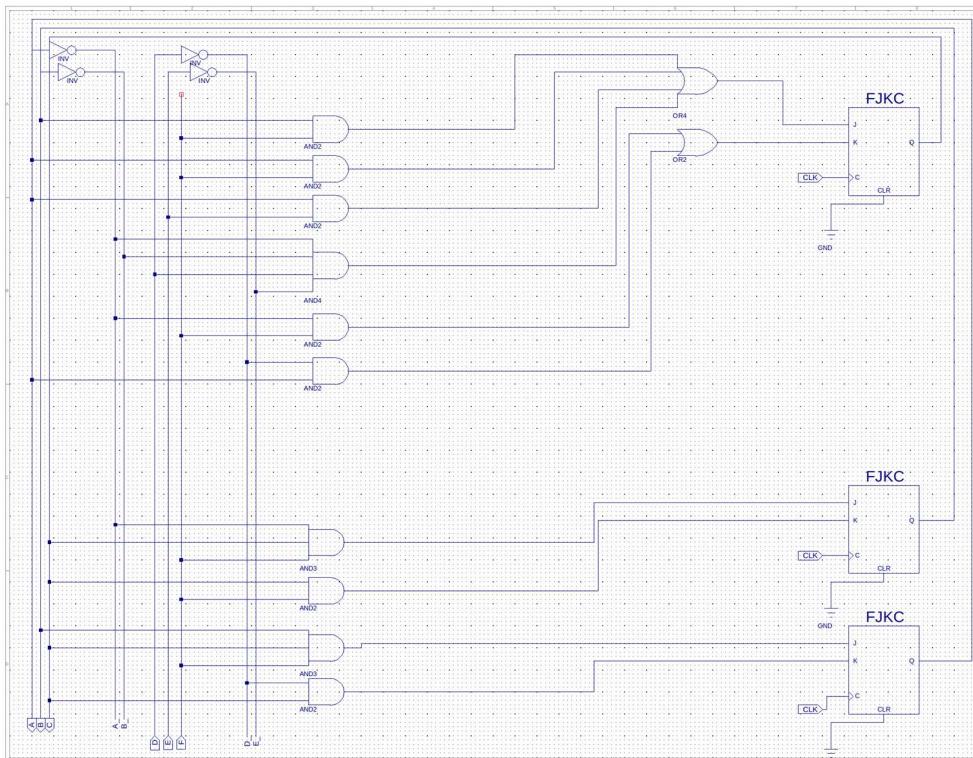


Name	Value
C	1
B	1
A	0
F	0
E	0
D	1



The simulation above is based on the FSM where the Clock and Timer are inputs whereas in the schematic above, they are operated without user input. The reason for this is so that there is more control over the simulation as well as technical issues allowing for both.

The corresponding schematic is below.



The GIC is

$$2+2+2+2+4+2+2+3+2+3+2+2+4 = 34 \text{ from above schematic.}$$

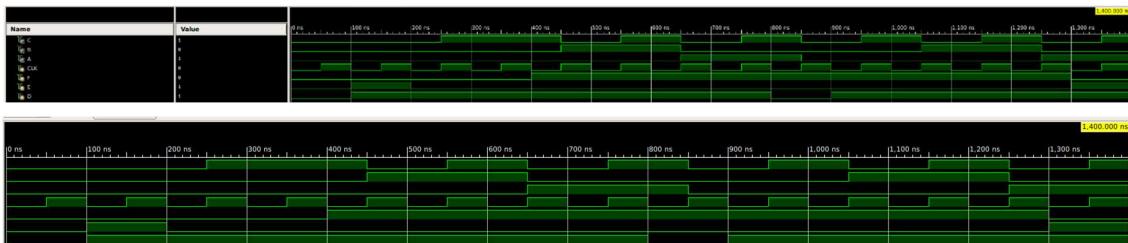
DFF = 52, TFF = 41, JKFF = 34. Best implementation would be JKFF for its low GIC compared to others.

Verilog Behavioural

```

1  timescale 1ns / 1ps
2 ///////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 21:00:15 04/16/2021
7 // Design Name:
8 // Module Name: Ass2141Behaviour
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module Ass2141Behaviour(
22   output C,
23   output B,
24   output A,
25   input CLK,
26   input F,
27   input E,
28   input D
29 );
30
31 reg A = 1'b0;
32 reg B = 1'b0;
33 reg C = 1'b0;
34
35 always@(posedge CLK) begin
36
37   if(A == 0 && B == 0 && C == 0 && D == 1 && E == 0) begin
38     C <= 1;
39   end
40
41   else if(A == 0 && B == 0 && C == 1 && F == 1) begin
42     B <= 1;
43     C <= 0;
44   end
45
46   else if(A == 0 && B == 1&& C == 0&& F == 1) begin
47     C <= 1;
48   end
49
50   else if(A == 0 && B == 1 && C == 1 && F == 1) begin
51     A <= 1;
52     B <= 0;
53     C <= 0;
54   end
55
56   else if ((A == 1 && B == 0 && C == 0) && (F == 1 || E == 1)) begin
57     A <= 1;
58     B <= 0;
59     C <= 1;
60   end
61
62   else if(A == 1 && B == 0 && C == 1 && D == 0) begin
63     A <= 0;
64     C <= 0;
65   end
66
67 end
68
69 endmodule
70 |

```



The simulation above is using the Verilog HDL (behavioural code) and shows that the schematic has the same function as the Behavioural code. The simulation code used for the Behavioural is the exact same as the Schematic.

Verilog Structural

```
timescale ins / ips
///////////////////////////////
// Company:
// Engineer:
//
// Create Date: 22:06:40 04/16/2021
// Design Name:
// Module Name: Ass2141Structural
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////
module Ass2141Structural(A, B, C, D, E, F, CLK);
    output A, B, C;
    input D, E, F, CLK;

    wire A_;
    wire B_;
    wire D_;
    wire E_;

    wire and2_Jc1;
    wire and2_Jc2;
    wire and2_Jc3;
    wire and4_Jc;

    wire and2_Kc1;
    wire and2_Kc2;

    wire or4_Jc;
    wire or2_Kc;

    wire and3_Jb;
    wire and2_Kb;

    wire and3_Ja;
    wire and2_Ka;

    nand(D_, D, D);
    nand(E_, E, E);

    and(and2_Jc1, B, F);
    and(and2_Jc2, A, F);
    and(and2_Jc3, A, E);
    and(and4_Jc, A_, B, D, E_);

    or(or4_Jc, and2_Jc1, and2_Jc2, and2_Jc3, and4_Jc);

    and(and2_Kc1, A_, F);
    and(and2_Kc2, D_, A);

    or(or2_Kc, and2_Kc1, and2_Kc2);

    and(and3_Jb, A_, C, F);
    and(and2_Kb, C, F);

    and(and3_Ja, B, C, F);
    and(and2_Ka, D_, C);

    JKFF JKCF(or4_Jc, or2_Kc, CLK, C);
    JKFF JKBF(and3_Jb, and2_Kb, CLK, B, B_);
    JKFF JKAF(and3_Ja, and2_Ka, CLK, A, A_);

endmodule

timescale ins / ips
/////////////////////////////
// Company:
// Engineer:
//
// Create Date: 22:01:31 04/16/2021
// Design Name:
// Module Name: JKFF
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////
module JKFF(J, K, CLK, Q, Q_);
    output Q, Q_;
    input J, K, CLK;

    wire nand_out1;
    wire nand_out2;

    nand(nand_out1, J, CLK, Q_);
    nand(nand_out2, K, CLK, Q);
    nand(Q, Q_, nand_out1);
    nand(Q_, Q, nand_out2);

endmodule
```