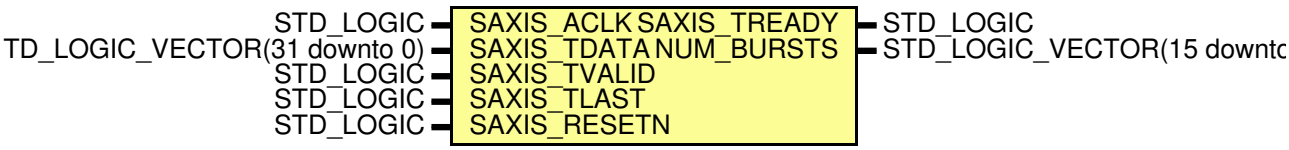
AXI_STREAM_STAT

- **File:** top_level.vhd
- **Author:** Joseph Pierce Vincent (josephpiercevincent@gmail.com)
- **Version:** 0.1
- **Date:** 2021-08-28

Diagram



Description

This module will monitor and ouput the number of bursts in a packet on the AXIS master bus attached to the slave port of this module.

Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
SAXIS_ACLK	in	STD_LOGIC	AXIS Bus Clock
SAXIS_TDATA	in	STD_LOGIC_VECTOR(31 downto 0)	AXIS Data lane
SAXIS_TREADY	out	STD_LOGIC	AXIS TREADY signal (always high indicating the module is always ready to receive data)
SAXIS_TVALID	in	STD_LOGIC	AXIS TVALID signal which indicated incomind data is valid
SAXIS_TLAST	in	STD_LOGIC	AXIS TLAST signal which indicates the end of an AXIS packet
SAXIS_RESETN	in	STD_LOGIC	Synchronous reset port
NUM_BURSTS	out	STD_LOGIC_VECTOR(15 downto 0)	Output statistic. The number of bursts in an entire transaction (How many TDATA datawords came in before the last TLAST)

Signals, constants and types

Signals

Name	Type	Description
tdata_r	STD_LOGIC_VECTOR(31 downto 0)	

Processes

- **count_dataWords**: ***(SAXIS_ACLK, SAXIS_RESETN)***