Full Adder

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In this lab we designed a Full Adder circuit using the Altera field programmable gate array(FPGA) and downloaded the design onto the chip of the DE2 board to perform the logic of full adder.

A full adder takes input of three one-bit binary (A, B, Cin) numbers and returns two one-bit binary numbers (Cout, Sum). The Cin and Cout are used when the number is longer than one bit, so they carry the extra bit. The Sum represents the addition of the two one-bits A and B.

Figure 1 shows design of Full-Adder

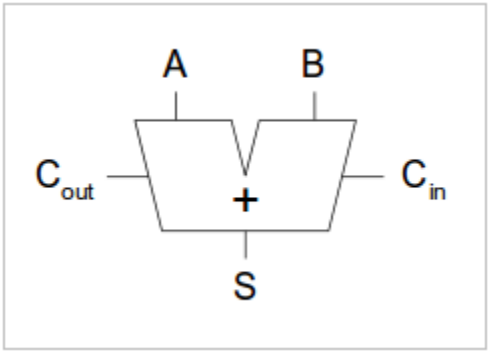

Figure 1

We designed the logic for the full adder first and then used the logic to build a truth table. Our first attempt failed as according to our logic the truth table that we got was not same as that we expected.

So we designed a new logic and drafted the truth table. This time the result of our truth table was as expected as of the Full Adder. Figure 2 shows the drafted design for Full adder and Table 1 shows the truth table for the drafted design.

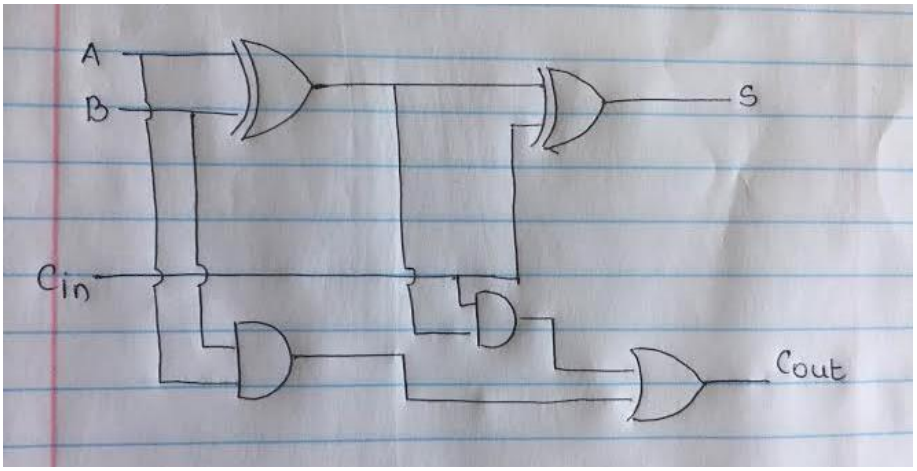

Figure 2

Input			Output	
Cin	B	A	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1

Once we finalized the design of our full adder we started to design our logic on the FPGA the Simulated our logic using Verilog and then implemented it on the DE2 board.

Figure 3 show the schematic of our Sum logic in Quartus.

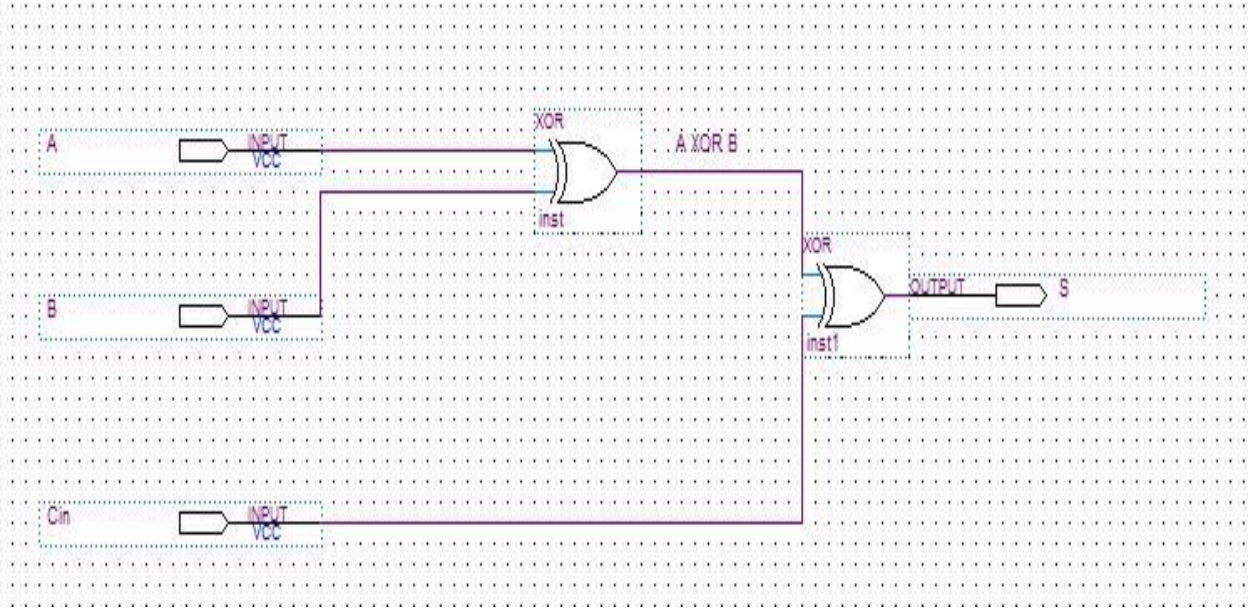

Figure 3

Figure 4 shows the schematic of our Full Adder designed in Quartus.

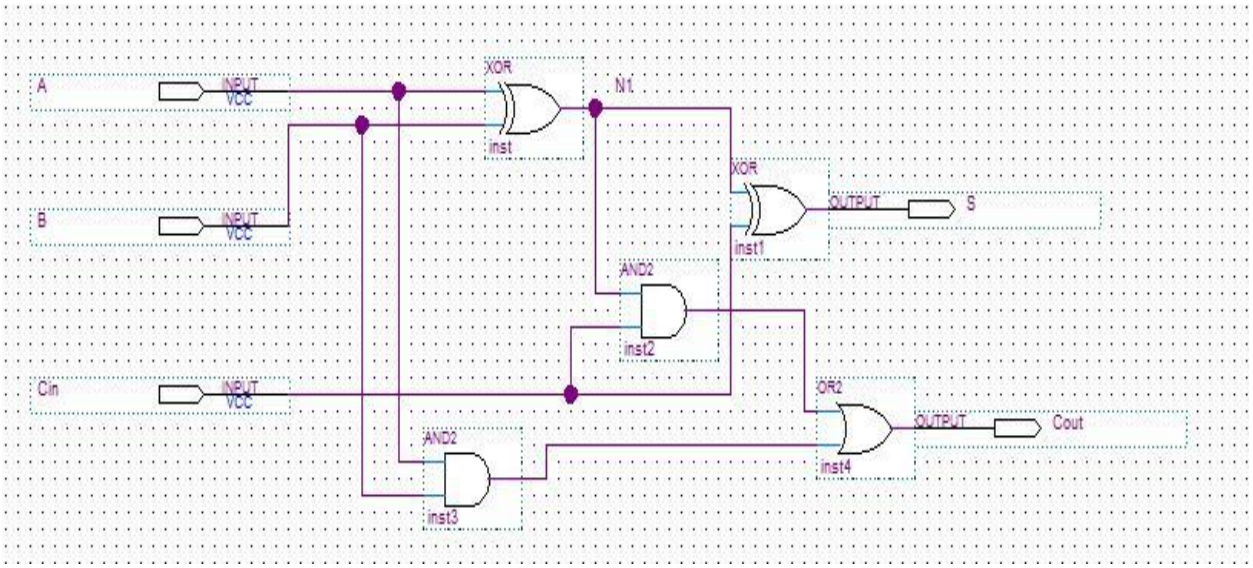

Figure 4

Figure 5 shows the Wave form from Verilog for 8 patterns of input

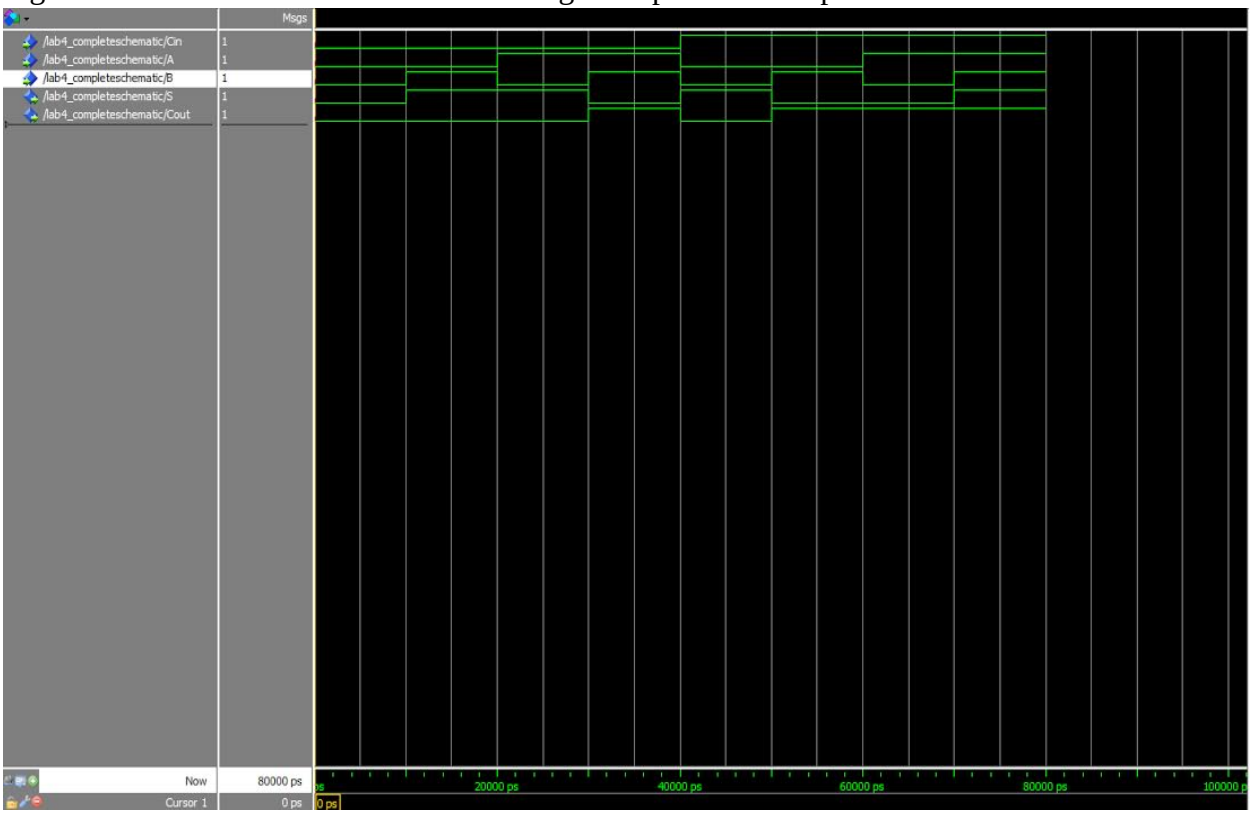

Figure 5

After generating the wave from we downloaded our circuit on the DE2 board. Providing the inputs to A, B and Cin we were able to see the output of Full Adder.

In the table 2 below I have tried to show the output as of LED's on DE2 board for all the 8 inputs.

A	B	C_{in}	S	C_{out}

	LED ON
	LED OFF

Table 2

To complete the full adder, it took us 2.5 hours.