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Computer Engineering – Mid Term

Answer 1:

1A	1B	Ā/B	1Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Answer 2:

LOAD VALUE	A0	A1	A2	A3	CLK	VALUE
0	1	0	1	1	0	(unknown)
0	1	0	1	1	1	(unknown)
1	1	0	1	1	0	(unknown)
1	1	0	1	1	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	1
1	1	0	1	1	0	1

Answer 3:

```
entity Shift_Register is
    port (
        A:         in std_logic_vector(3 downto 0);
        LOADVALUE: in std_logic;
        CLK:       in std_logic;
        VALUE:     out std_logic
         );
end entity;

architecture sr of Shift_Register is
       signal t:std_logic; -- signal to hold the third bit
       signal Q:std_logic_vector(3 downto 0); -- state of four flip-flops
begin
    process (A, LOADVALUE, CLK) begin
       if (LOADVALUE = '0') then
              Q(3 downto 0) <=A(3 downto 0);
       elsif(CLK'event and CLK='1')then
              t<=Q(3)
              Q(3 downto 1) <=Q(3 downto 1);
              Q(0)<='0';
       Endif;
    end process;
VALUE<=t;
end;
```