Observation of the Behavior of an Flip-Flop Devices

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Abstract

In this lab, we will explore the behavior of a Flip Flop devices. We will review the NAND flip flop and observe properties of JK flip flops. We will confirm the JK flip flop table and observe the behavior of a Jk flip flop counter.

1 Preperation

In order to prepare for this lab, we review the behavior of the NAND Gate flip flop from the previous lab and the JK flip flop. As we already know a NAND Gate follows the Boolean function

Not(A and B)

and produces the folowwing truth table.

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: NAND Gate Behavior

For the NAND flip flop, we know the configuration is

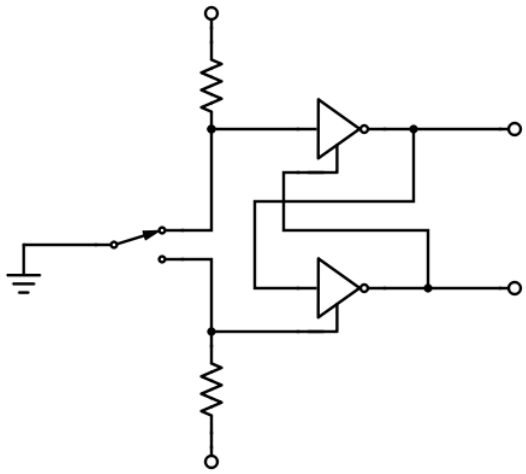

Figure 1: A Flip Flop NAND with resistors.

with the truth table being

S	R	Q_1	Q_2
0	0	?	?
0	1	1	0
1	0	0	1
1	1	$\emptyset$	$\emptyset$

Table 2: NAND Gate Behavior

When both inputs are grounded there is no output as it is not an acceptable state and whenever one is grounded and the other is triggered one of the outputs gives a voltage and does not change until the voltage in the inputs is switched.

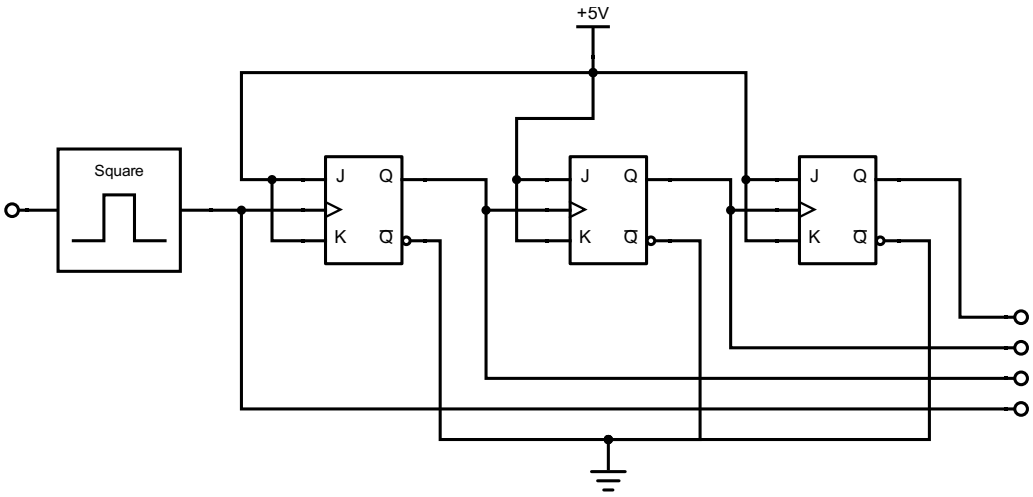

Figure 2: JK Flip-Flop Counter

The JK flip flop is simply a flip flop gate in a single device rather that using multiple logic gates. It is essentially an integrated circuit of AND gates is a flip flop formation. JK flip flops include a clocked input which can alter the output depending on the state of the inputs when the clocked pulse arrives. The truth table for the JK flip flop is

J	K	Q_1	Q_2
0	0	$\emptyset$	$\emptyset$
0	1	1	0
1	0	0	1
1	1	$0 \leftrightarrow 1$	$0 \leftrightarrow 1$

Table 3: JK Flip Flop Behavior

When there are two inputs, the output is dependent on the clock input thus the outputs may be 1 or 0. The $\emptyset$ means that the output is simply what ever it previously was.

2 Lab work

In this lab we simply set up the circuits in Fig 1 and Fig 2. We used 5V for the TRUE input and ground for the FALSE input. For the NAND flip

Q_3	Q_2	Q_1	Value
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 4: Caption

flop gate and JK flip flop gate we observed the results as expected in Table 1 and 2. In order to test the counter each of the output was connected to LEDs as represented by the ports in Fig 2. The LED would respond to the outputs while the LED connected to the oscillator simply oscillated on and off. As the oscilation occured the LED would turn on in sequence as floows.

3 Summary and conclusions

In this lab, we have reviewed the NAND flip flop and saw how a JK flip flop operates on its own and as a counter. We confirmed the the truth table for the NAND flip flop and JK flip flop. We saw how the JK flip flop counter could count to 7 in binary with the rate at which is counted being dependent on the frequency of the gien input wave.