PROPORTIONAL INTEGRAL CONTROLLER 2.5.2

MANUAL

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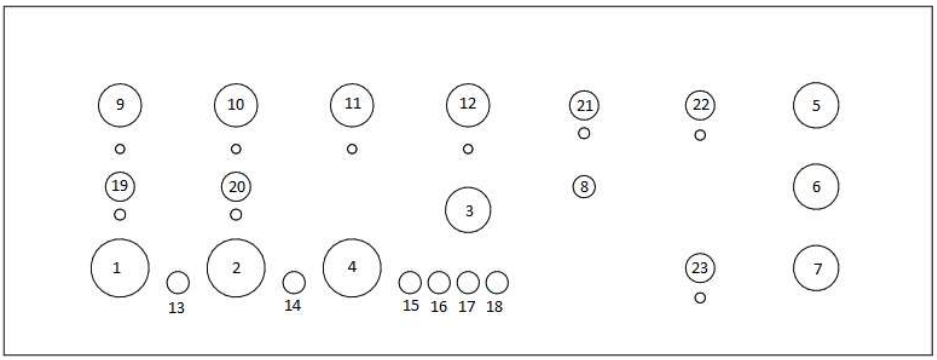
Front Panel



Inputs

1. IN1 - Positive input (±10V, 1MΩ input impedance)
2. IN2 - Negative input (±10V, 1MΩ input impedance)
3. SWP_EXT - External sweep input (±10V, 10kΩ Input Impedance)

Outputs

4. OUT - PI filtered output signal (50Ω output impedance)
5. IN_MON - Monitor selected input voltage IN1/IN2
6. ERR_MON - Monitor error voltage
7. OUT_MON - Monitor output voltage

$$OUT = OUT\_MON \times \frac{R_{load}}{50\Omega + R_{load}}$$

Indicator

8. LED - lock indicator (Green/Red)

Controls

Potentiometer Knobs

9. I_GAIN - Integral gain control (Gain Range:0→10 with Dial: 20→80)
10. P_GAIN - Proportional gain control (Gain Range:0→10 with Dial: 20→80)
11. OUT_OFFSET - Output offset voltage control (±10.0V)
12. SWP_AMP - Sweep amplitude control

Front Panel Trimmer Potentiometers

13. IN_OFFSET - Input offset voltage control (±5.0V)
14. LO_LIMIT - Low limit of OUT (±10V)
15. HI_LIMIT - High limit of OUT (±10V)
16. ERR_DET - Absolute limit detection of error signal (Range: ±0→±1.5V)
17. LO_DET - Low limit detection of OUT
18. HI_DET - High limit detection of OUT

Switches

19. Unused switch (Fine input offset switch in version 2.4.1)
20. IN_MON_SEL (2 Positions) - Select to monitor IN1 (up) or IN2 (down)
21. LOCK/LFGL/UNLOCK (3 Positions) - Select filter mode
22. IUGC (9 Positions) - Select integral unity gain cutoff frequency
23. LFGL (9 Positions) - Select integral gain limit in LFGL mode

Controls

Integral

I_GAIN

Continuous integral gain setting (I_GAIN: 0→10 with Dial: 20→80)
In typical usage, I_GAIN should be set at 10 or as high as possible.

IUGC (Integral Unity Gain Cutoff)

Select setting for integral unity gain cutoff

IUGC	Unity Gain Cutoff frequency = $\frac{I_{GAIN}}{2\pi R}$ (I_GAIN=3→10)
1*	34 Hz → 100 Hz
2*	100 Hz → 340 Hz
3*	340 Hz → 1 kHz
4*	1 kHz → 3.4 kHz
5	3.4 kHz → 10 kHz
6	10 kHz → 34 kHz
7	34 kHz → 100 kHz
8	100 kHz → 340 kHz
9†	340 kHz → 1 MHz

* Proportional gain must be turned off
† Proportional gain must be turned on

LFGL (Low Frequency Gain Limit)

Select setting for Low Frequency Gain Limit.

Position	LFGL = $20\ \mathrm{Log}_{10}(\frac{I_{GAIN}R_{LFGL}}{10000\Omega})$ (I_GAIN=3→10)
1	-10dB → 0dB
2	0dB → 10dB
3	10dB → 20dB
4	20dB → 30dB
5	30 dB → 40dB
6	40dB → 50dB
7	50 dB → 60dB
8	60 dB → 70dB
9	70 dB → 80dB

Determine Suitable Integral Settings

In negative feedback control scheme, high gain is required to make system signal close to equal the reference signal. Fast signal response is also desired to make system signal follow reference signal as fast as possible. However, if the gain of the feedback system is too high and too fast (gain higher than 0dB at 0 degree phase margin), the feedback system will become unstable and oscillate.

To find suitable Integral setting, first, try locking the system with the following setting I_GAIN=10, IUGC=8, LFGL=9, P_GAIN=0.

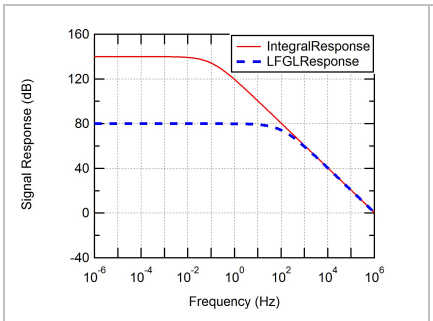
If the system oscillate with this setting, try the following

1. Set mode to LFGL and reduce LFGL setting.
2. Use lower IUGC setting and repeat 1.
3. Use lower I_GAIN setting (I_GAIN lower than 3 is not recommended)

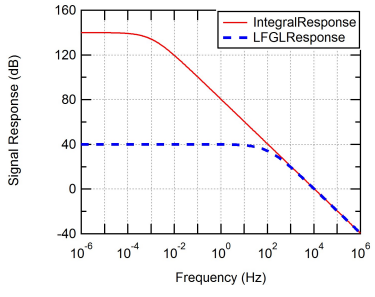
If the system cannot be locked with the setting I_GAIN=1, IUGC=1, LFGL=1, P_GAIN=0, the system may be too slow to be locked with this controller.

Bode Plot of Integral Signal Response

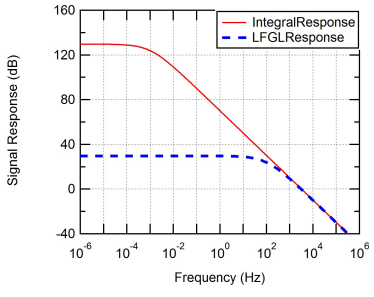
The following are examples integral response at different settings. The interactive plotting code (Igor pro) can be found at \Documents\PI_BodePlot.pxt



I_GAIN=10,
IUGC(9)=1MHz, LFGL(9)=80dB



I_GAIN=10,
IUGC(5)= 10kHz, LFGL(5)=40dB



I_GAIN=3,
IUGC(5)= 3kHz, LFGL(5)=30dB

Proportional

P_GAIN

Continuous proportional gain setting (P_GAIN: 0→10 with Dial: 20→80)

While the integral signal has unity gain bandwidth up to 1 MHz, the proportional signal has unity gain bandwidth between 1 kHz to 10 MHz. Due to high speed nature of Proportional signal, if P_GAIN is too high (P_GAIN*SYSTEM_GAIN > 0dB), it may cause an oscillation on system that has response bandwidth less than 20MHz.

To find suitable P_GAIN setting, first, set P_GAIN=0 and lock the system using only the integral signal. Then, slowly increase P_GAIN until OUT start to oscillate. The suitable setting for P_GAIN is 90-95% of P_GAIN that makes OUT oscillate.

Operation Mode

UNLOCK: Switch Down

OUT is set by OUT_OFFSET, SWP_EXT, and SWP_AMP.
Output scan is active

LFGL: Switch Middle

Output scan is active.
PI filter is active with limited low frequency gain

LOCK: Switch Up

Output scan is inactive.
PI filter is active with 120dB + I_GAIN[dB] low frequency gain.

Operation Formula

$$ERR = IN1 - IN2 + IN\_OFFSET$$
$$SWP = SWP\_AMP \times SWP\_EXT$$
$$P = P\_GAIN \times (IN1 - IN2) \mid \text{for signal frequency 100 Hz to 10MHz}$$

UNLOCK: $OUT = OUT\_OFFSET + SWP$
LFGL: $OUT = OUT\_OFFSET + SWP + P + LFGL[I\_GAIN \times ERR]$
LOCK: $OUT = OUT\_OFFSET + P + INT[I\_GAIN \times ERR]$

LFGL is the integration with limited gain
INT is the open-loop integration

Miscellaneous Setting

LO_LIMIT/HI_LIMIT

The trim potentiometers set the low/high limit of OUT signal.

To set the output range:

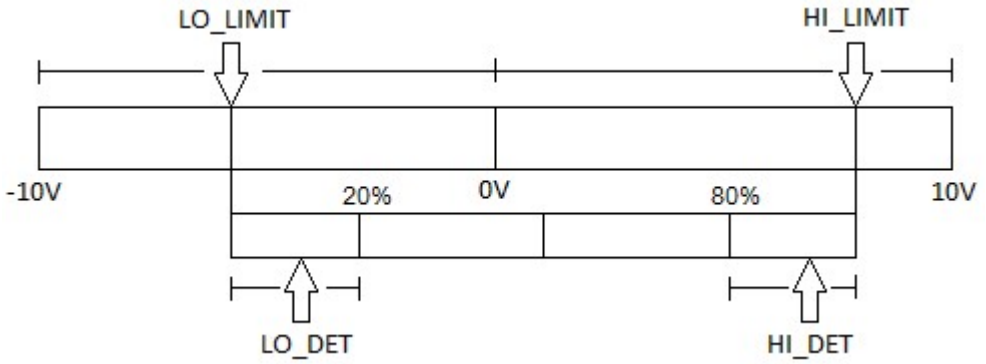
1. Disconnect IN1 and IN2, Monitor voltage value of OUT
2. Set filter mode to LOCK
3. Turn IN_OFFSET clockwise until OUT increases to high limit
4. Adjust HI_LIMIT to desire level
5. Turn IN_OFFSET counter-clockwise until OUT decreased to low limit
6. Adjust LO_LIMIT to desire level

ERR_DET

The LED indicator will become red if the value of ERR_MON is outside the range of ERR_DET (Variable Range: ±0→±4V).

LO_DET/HI_DET

The LED indicator will become red if the signal OUT is greater than HI_DET or lower than LO_DET. HI_DET can be set from 80% to 100% of output range. LO_DET can be set from 0% to 20% of output range.

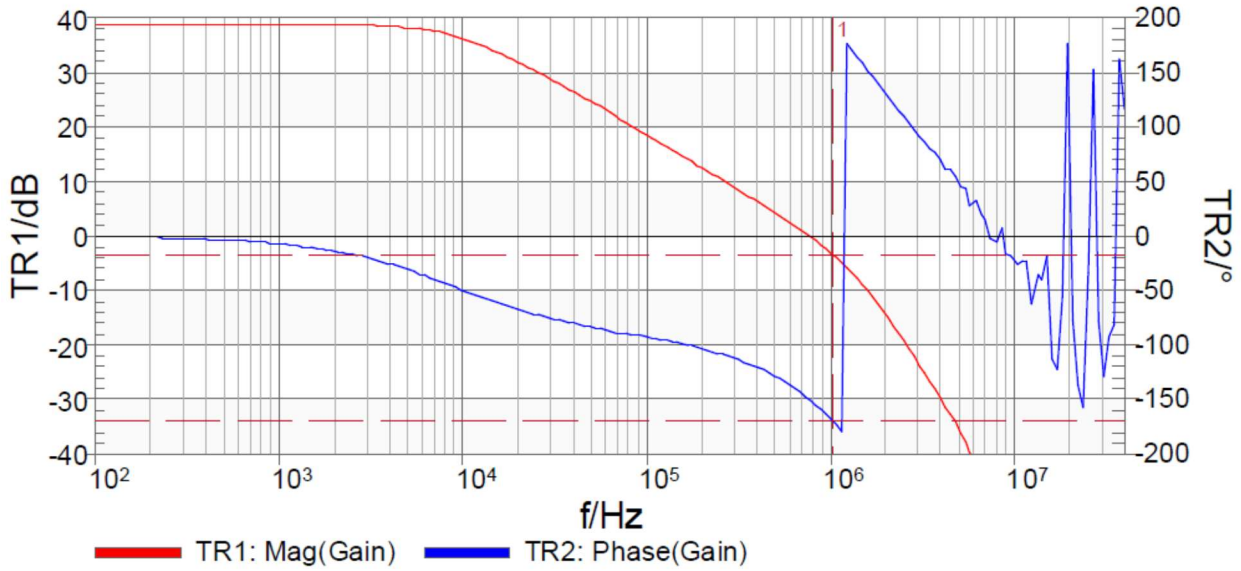


Performance

Raw data can be found at \Documents\TestResults2.5.1Mod\

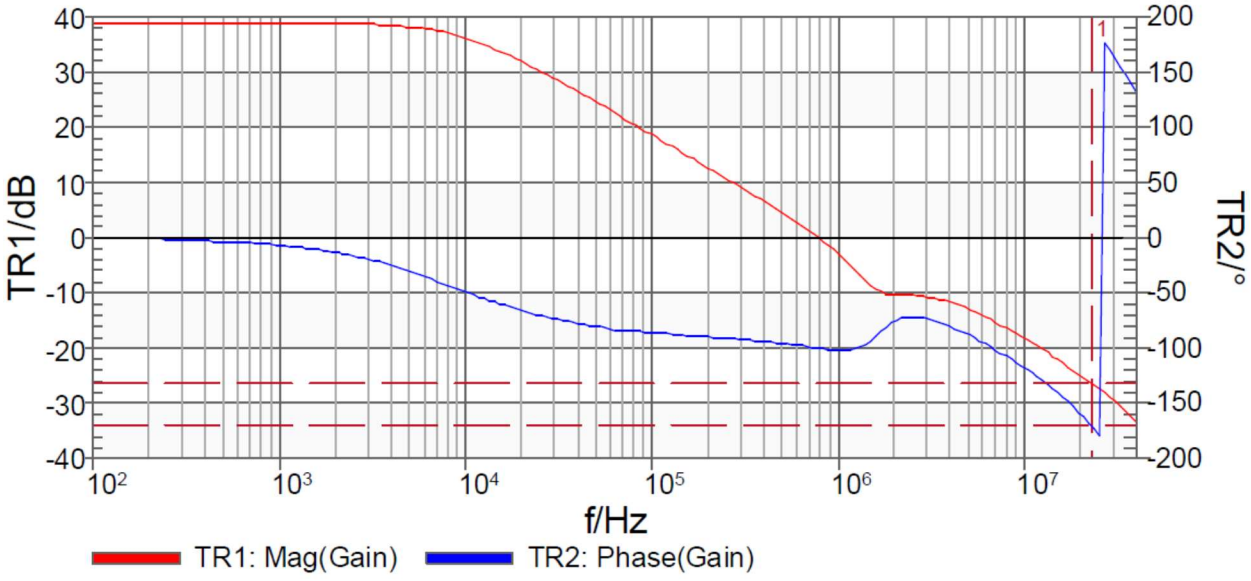
Bode Plots

Settings1: I_GAIN=20dB, P_GAIN=-60dB, IUGC(9)=1MHz, LFGL(5)=40dB, Open-loop

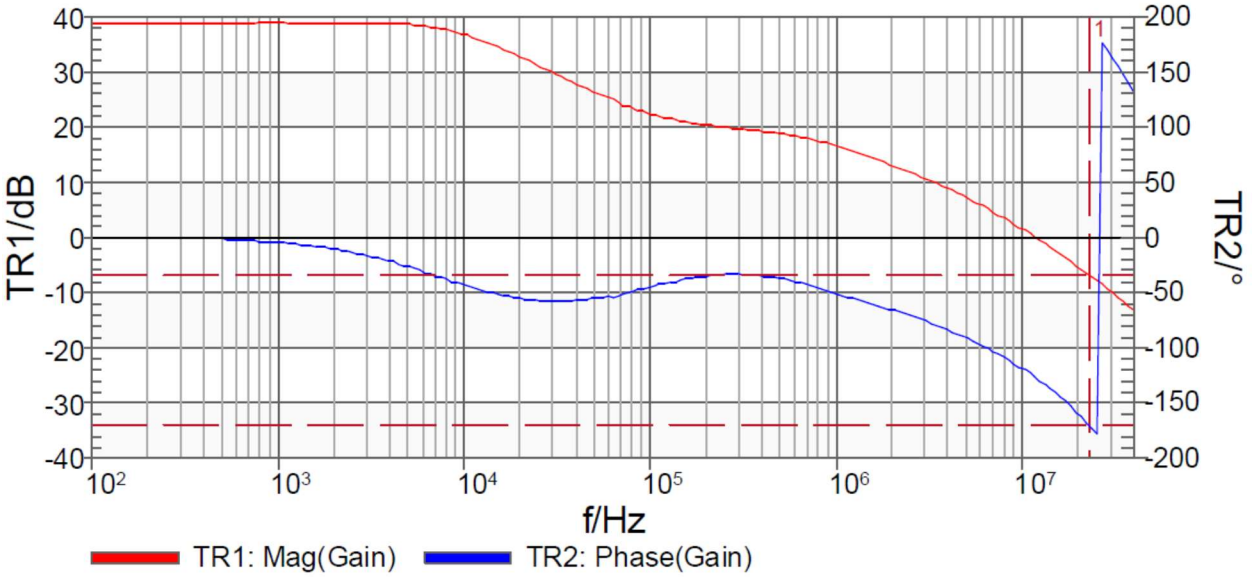


The integration setting IUGC(9)=1MHz should be used with proportional signal to improve phase margin as shown in Setting2

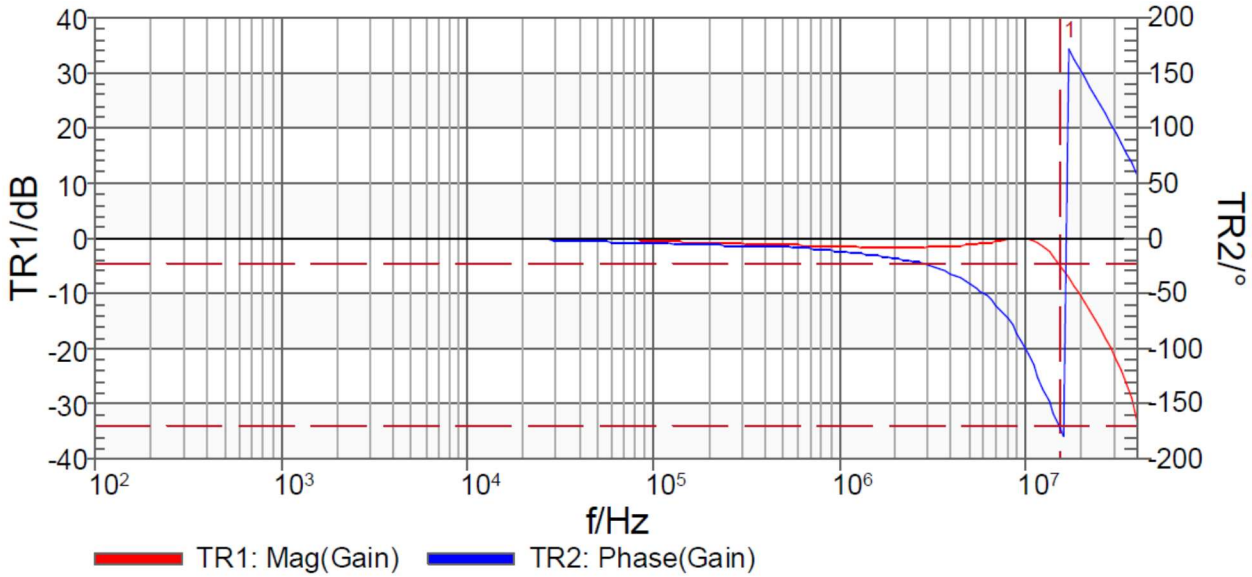
Settings2: I_GAIN=20dB, P_GAIN=0dB, IUGC(9)=1MHz, LFGL(5)=40dB, Open-loop



Settings3: I_GAIN=20dB, P_GAIN=20dB, IUGC(9)=1MHz, LFGL(5)=40dB, Open-loop



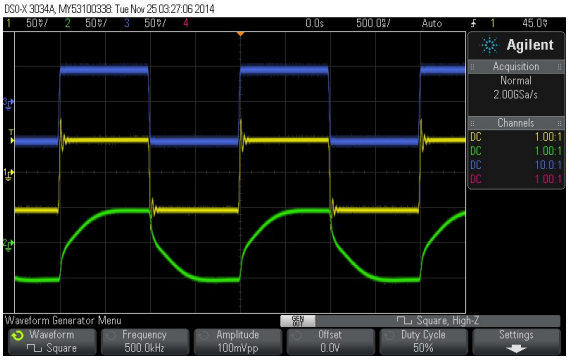
Settings4: I_GAIN=20dB, P_GAIN=15dB, IUGC(9)=1MHz, Self-lock (OUT→IN2)



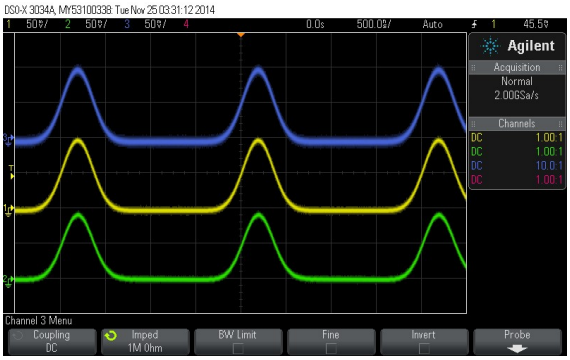
Self-Lock to Changing Reference

Use settings: I_GAIN=20dB, P_GAIN=10-20dB, IUGC(9)=1MHz, Self-lock (OUT→IN2)

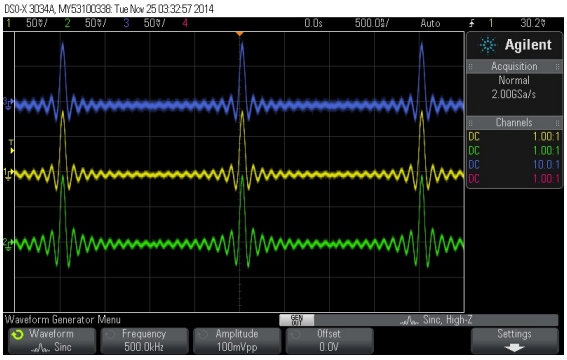
Blue: Reference signal (IN1)
Yellow: Reference Input monitor signal (IN1_MON)
Green: Output monitor signal (OUT_MON)



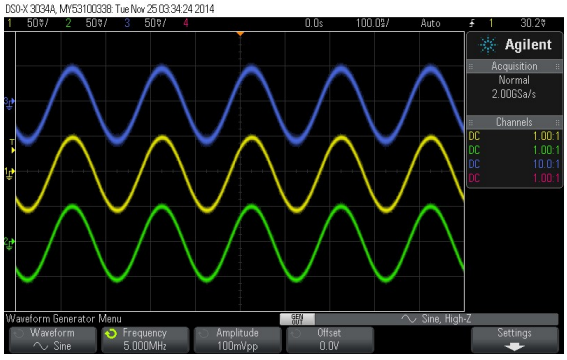
X-axis=500ns/div Y-axis=50mV/div



X-axis=500ns/div Y-axis=50mV/div

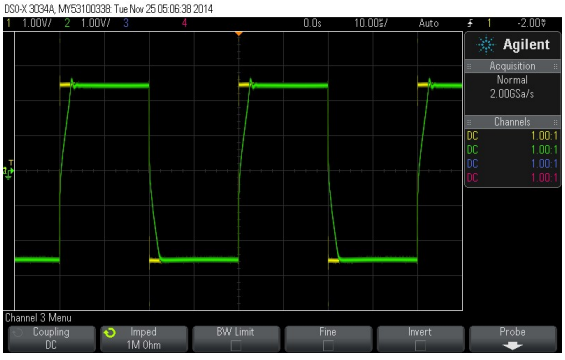


X-axis=500ns/div Y-axis: 50mV/div



X-axis=100ns/div Y-axis: 50mV/div

Test with large change in reference (±2.5V)
Yellow: Reference Input monitor signal (IN1_MON)
Green: Output monitor signal (OUT_MON)



X-axis=10us/div Y-axis: 1V/div

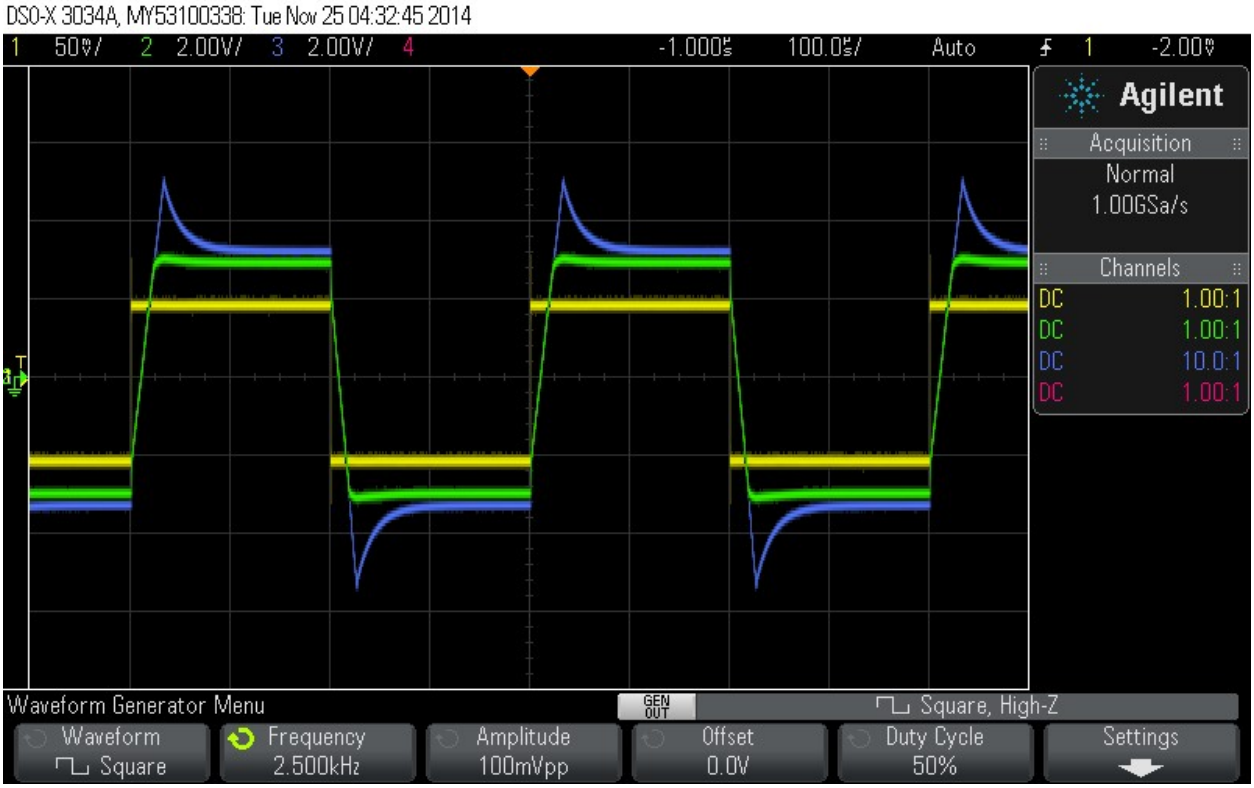
Integral Limiter and Output Limiter

Use settings: I_GAIN=20dB, P_GAIN=0dB, IUGC(9)=1MHz, LFGL(5)=40dB, Open-loop
Set output high limit to +3V and output low limit to -3V

Yellow: Error monitor signal (ERR_MON)
Green: Output monitor signal (OUT_MON)
Blue: Output detection signal (OUT_DET)

OUT_DET is the output signal before output limiter; this signal is used for integral limiter.

When OUT_DET passes the output limits, it activates integral limiter that will stop the integrator from integrating signal further away from output limit. The output signal always stay inside the limit. However, OUT_DET may overshoot pass the output limit and recover back to stay slightly outside the output limit.



Assembly

Front Panel Connection

RefDes	Front Panel Function
J1	External Sweep
J4	Input Monitor
J5	Error Monitor
J6	Output Monitor
LED1	Red/Green LED 1 = GREEN P-doped (Anode) 2 = RED P-doped (Anode)
POT7	Sweep Amplitude
POT8	Output Offset
POT9	Integral Gain
POT10	Proportional Gain
S6	Input Monitor Select 2→1 (D) = Monitor Input2 2→3 (U) = Monitor Input1
S4	IUGC setting 1→2 = IUGC1 1→3 = IUGC2 1→4 = IUGC3 1→5 = IUGC4 1→6 = IUGC5 1→7 = IUGC6 1→8 = IUGC7 1→9 = IUGC8 1→10 = IUGC9
S5	LFGL setting 1→2 = LFGL1 1→3 = LFGL2 1→4 = LFGL3 1→5 = LFGL4 1→6 = LFGL5 1→7 = LFGL6 1→8 = LFGL7 1→9 = LFGL8 1→10 = LFGL9
S7	Unlock/LowFrequencyGainLimit/Lock SP3T Connections: Pin1→1, Pin2→2, Pin3→Pin5, Pin4→3 2→ (U) = Lock 2→3 (M) = LFGL 2→1 (D) = Unlock

Initial Calibrations and Tests

Power up:

1. Connect all front panel controls to the board
2. Connect OUT_MON to oscilloscope to monitor output voltage for initial testing
3. Turn on power supply to the board
4. The board should use around 300mA from +15V and 260mA from -15V. If you use test power supply, set the current limit to 800mA to both +15V and -15V.
5. Change OUT_OFFSET to set OUT_MON to 0V.

Setup HI_LIMIT and LO_LIMIT:

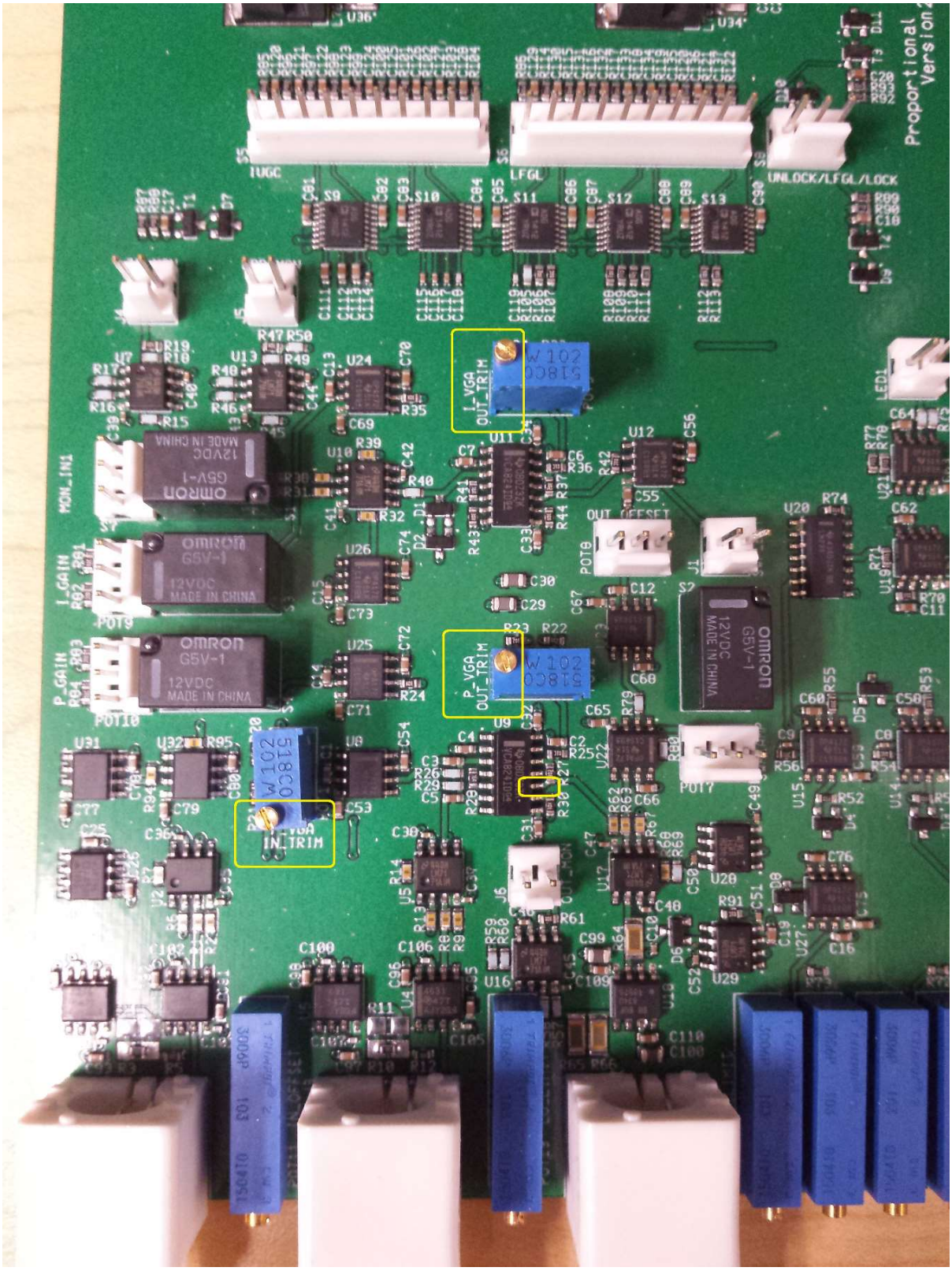
6. Set mode to LOCK.
    a. If OUT_MON decrease after set mode to LOCK, OUT_MON is at LO_LIMIT
    b. If OUT_MON increase after set mode to LOCK, adjust IN_OFFSET CCW until OUT_MON decrease to LO_LIMIT
7. Change LO_LIMIT to set OUT_MON to -6V
8. Adjust IN_OFFSET CW until OUT_MON increase to HI_LIMIT
9. Change HI_LIMIT to set OUT_MON to +6V

Proportional VGA calibration: See picture next page

10. Set mode to UNLOCK
11. Use probe to measure the output pin (U9—Pin10)
12. Adjust the output of the VGA (U9—Pin10) to 0V with P_VGA_OUT_TRIM (POT2)
13. Set mode to LOCK, Set P_GAIN to maximum
14. Adjust the output of the VGA (U9—Pin10) to 0V with P_VGA_IN_TRIM (POT1)

Integral VGA calibration:

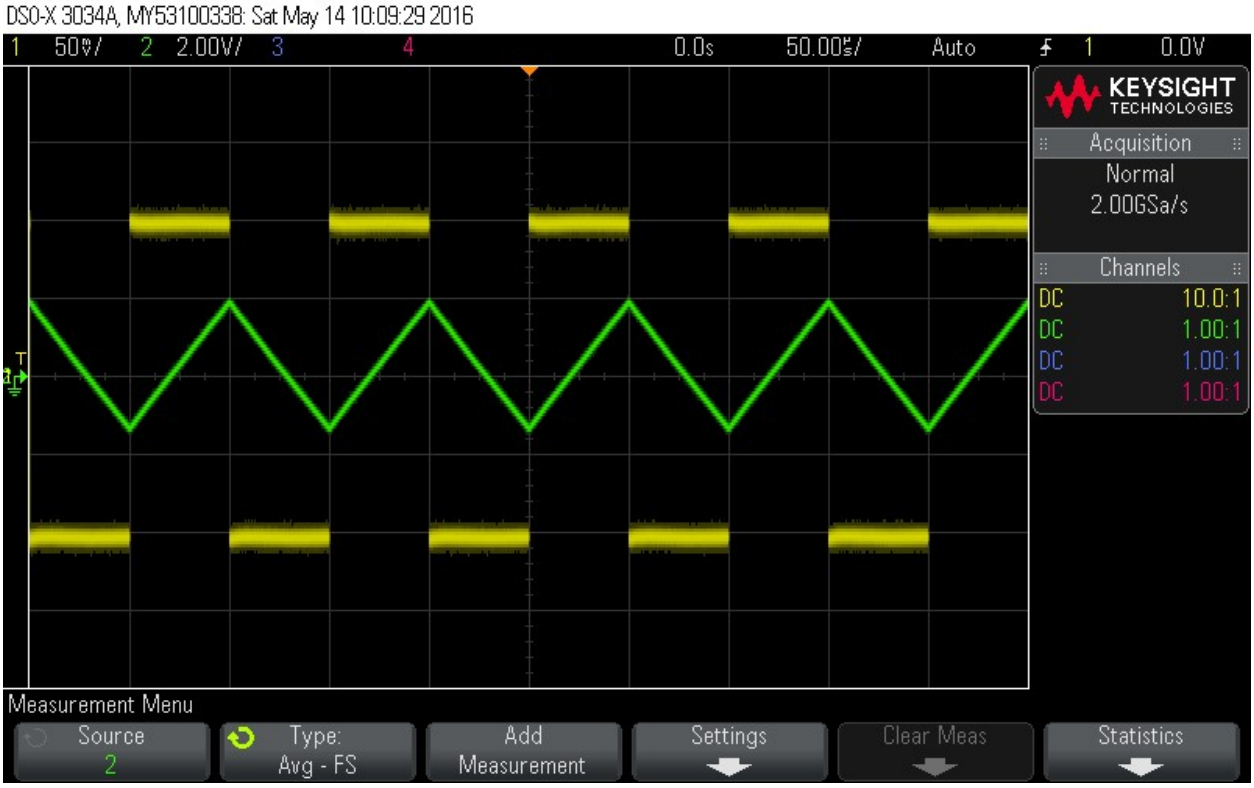
15. Measure OUT_MON voltage
16. Set mode to LFGL with this setting I_GAIN = 0, P_GAIN = 0, IUGC(7), LFGL(5)
17. Adjust OUT_MON to 0V with I_VGA_OUT_TRIM (POT3)


I_VGA OUT_TRIM
P_VGA OUT_TRIM
I_GAIN
P_GAIN
MON_IN1
LFGL
UNLOCK/LFGL/LOCK
Proportional Version
OUT OFFSET
omron G5V-1 12VDC MADE IN CHINA

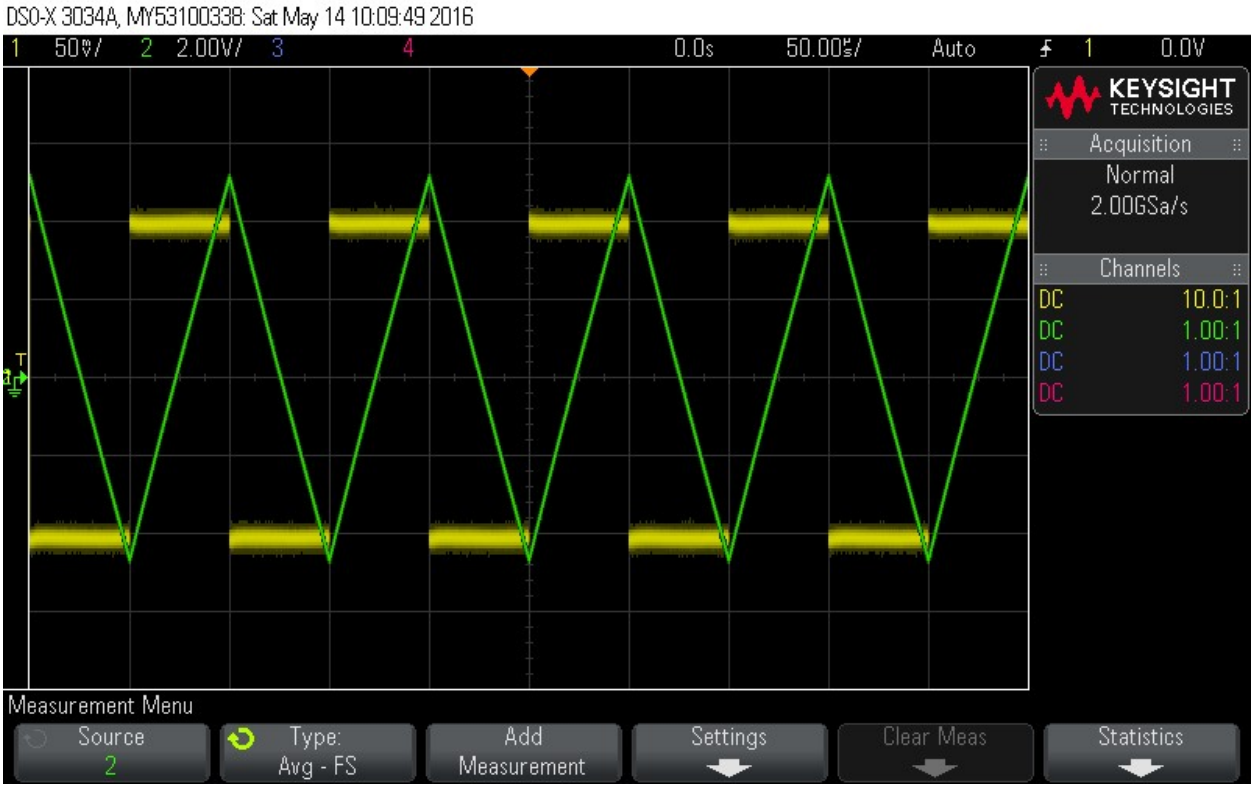
Square wave reference test:

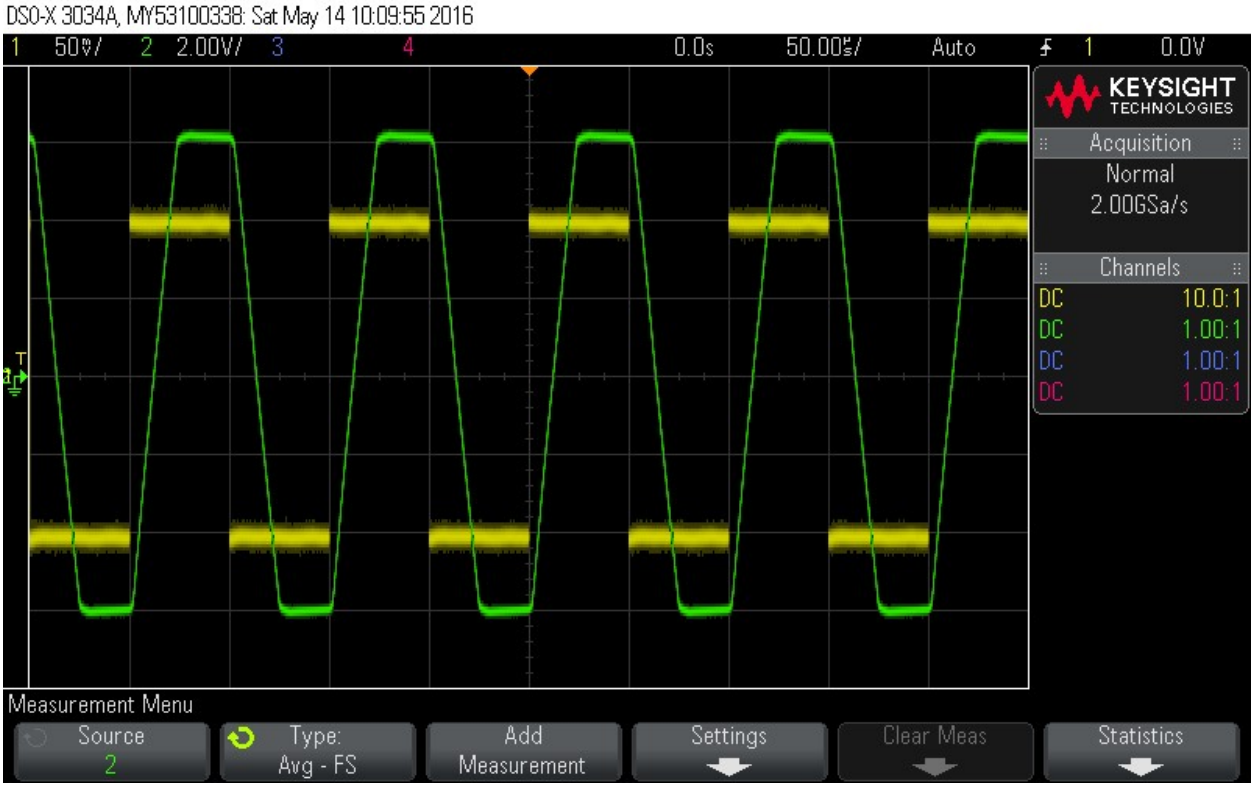
18. Generate a 10kHz square wave 0.2Vpp (reference signal)
19. Send the reference signal to IN1 (Positive input)
20. Connect IN_MON to oscilloscope to monitor IN1
21. Set mode to LFGL with this setting I_GAIN = Max, P_GAIN = 0, IUGC(7), LFGL(7)
22. OUT_MON should show triangle wave (integral of square wave)
    a. Yellow = reference signal
    b. Green = OUT_MON
    c. Output may be clipped at output limit

23. Adjust IN_OFFSET to set the OUT_MON to center at 0V

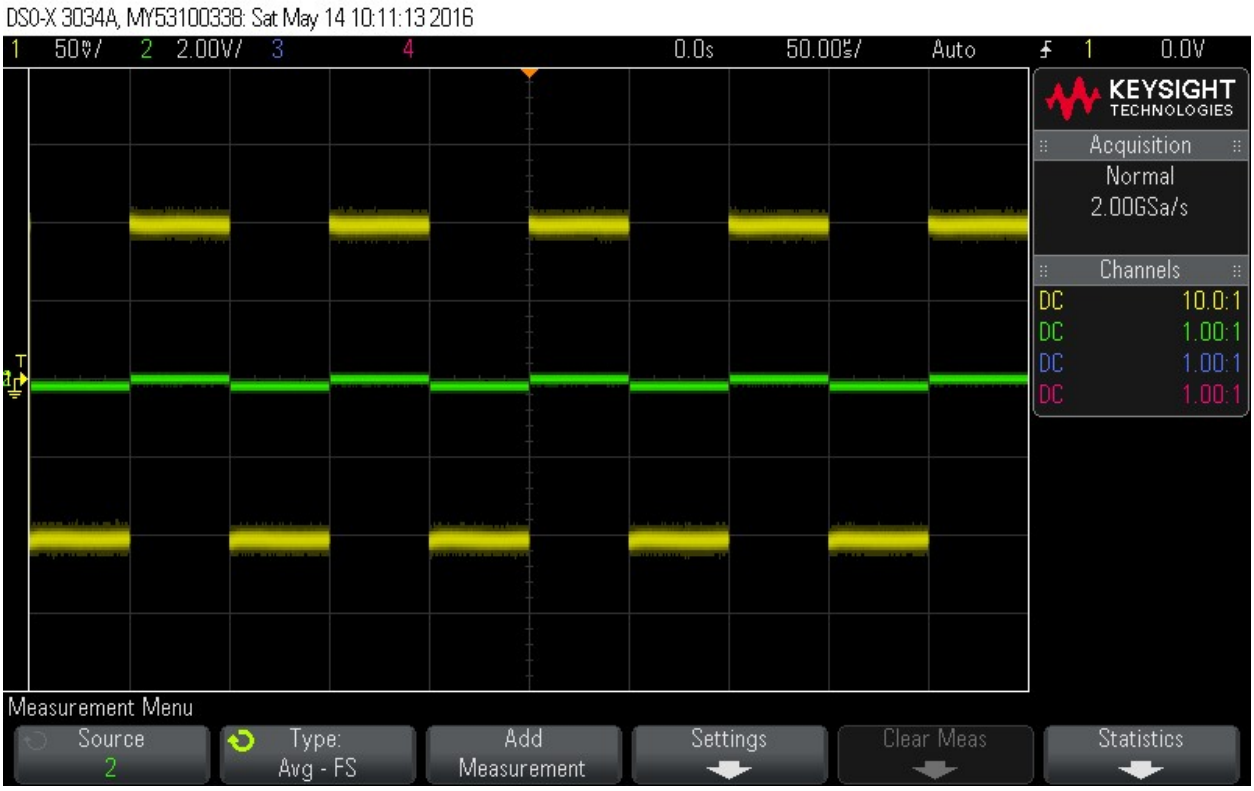


24. Change IUGC setting to IUGC(8) and IUGC(9) to observe faster integration and output limiting capability

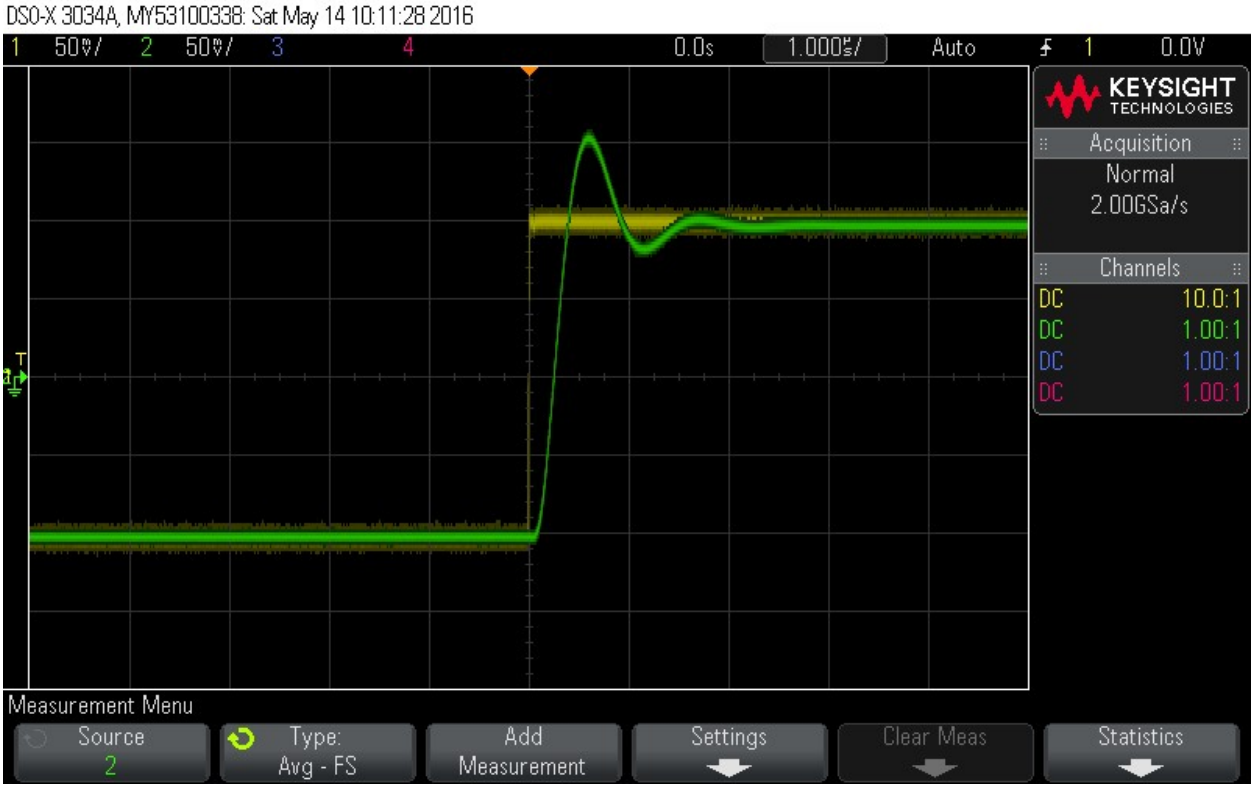




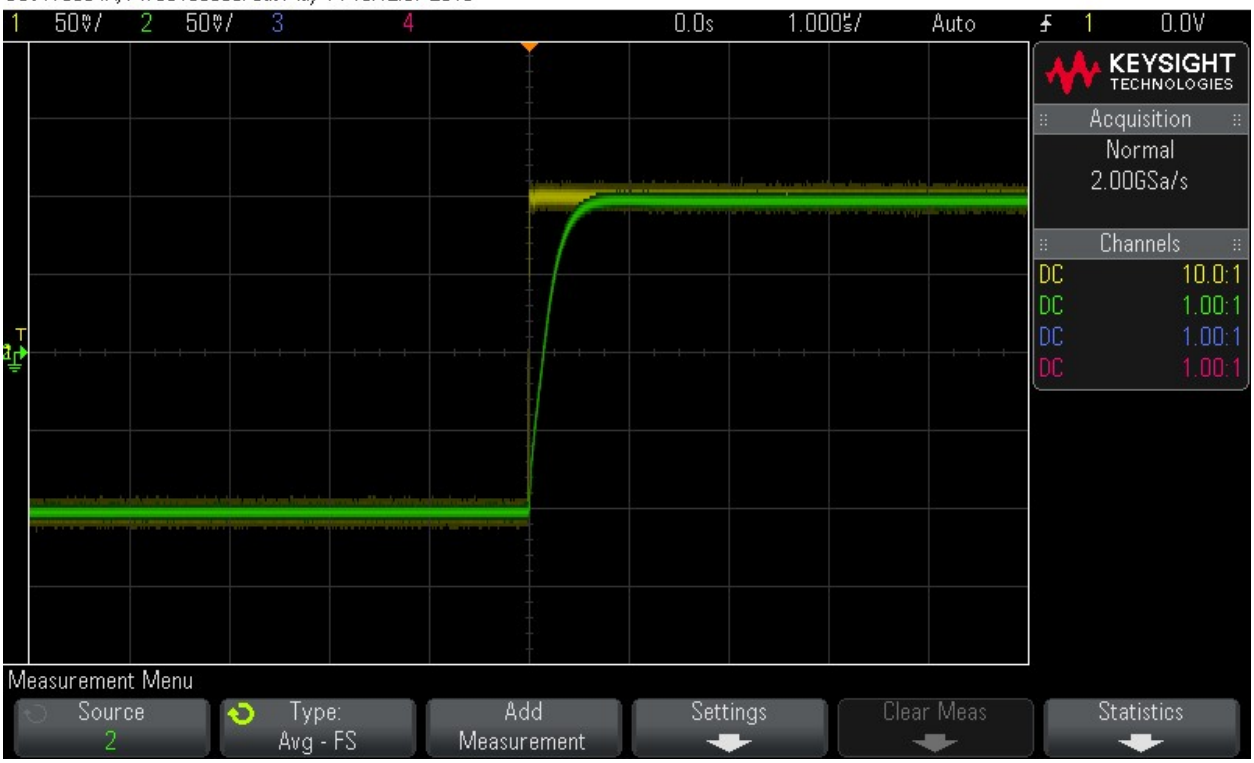
25. Set mode to LFGL with setting I_GAIN = Max, P_GAIN = 0, IUGC(9), LFGL(7)
26. Connect cable from OUT to IN2 (Self-Lock)
27. OUT_MON now should follow the reference square wave



28. Zoom in to see the transition edge.



29. Increase P_GAIN to achieve a good transition response.



Pin note

Potentiometer Pin
2
|
V
(CCW) 1------3 (CW)

SPDT Switch positions (key down):
DOWN (2—1), UP (2—3)
SP3T Switch positions (key down):
ON-ON-ON DP contact form (6Legs) (Part#7211P3YZQE)
DOWN (L2→L1, L5→L4), MID (L2→L3, L5→L4), UP (L2→L3, L5→L6)

Upgrade from version 2.4.1

Version 2.5.2 can use enclosure of version 2.4.1 with a minor wiring modification. All 3 pins of control potentiometer knob #9 (see Front Panel) must be connected to 3-pin plug, which will be plugged to P_GAIN on the board. (PotPin1→PlugPin1, PotPin2→PlugPin2, PotPin3→PlugPin3)

Panel Cutout

3 BNCs: IN1, IN2, OUT
Diameter = 0.50 in.
Position:
From Left = 0.5+LeftSpace, +1.00, +1.00 in.
From Bottom = 0.375 in. + Standoff Length (Minimum 0.3 in.)

6 Trim pots: IN_OFFSET, LO_LIMIT, HI_LIMIT, ERR_DET, LO_DET, HI_DET
Diameter = 0.125 in.
Position:
From Left = LeftSpace+1.00, +1.00, +1.00, +0.25, +0.25, +0.25 in.
From Bottom = 0.25 in. + Standoff Length

4 Pots: FINE_OFFSET, OUT_OFFSET, GAIN, SWP_AMP
Hole Diameter = 0.37 in.
Key Diameter = 0.078 in., Offset 0.375 in.
Knob Diameter = 0.875 in.

4 BNC: IN_MON, ERR_MON, OUT_MON, EXT_SWP
Hole Diameter = 0.39 in.

2 Rotary Switches: PI_CORNER, LFGL_LEVEL
Hole Diameter = 0.25 in.
Key Diameter = 0.087 in., offset 0.256 in.
Knob Diameter = 0.75 in

1 SPDT Toggle Switches: MON_IN1
1 SP3T Toggle Switch: UNLOCK/LFGL/LOCK
Diameter = 0.25 in.
Key Diameter = 0.094 in., offset 0.24 in.

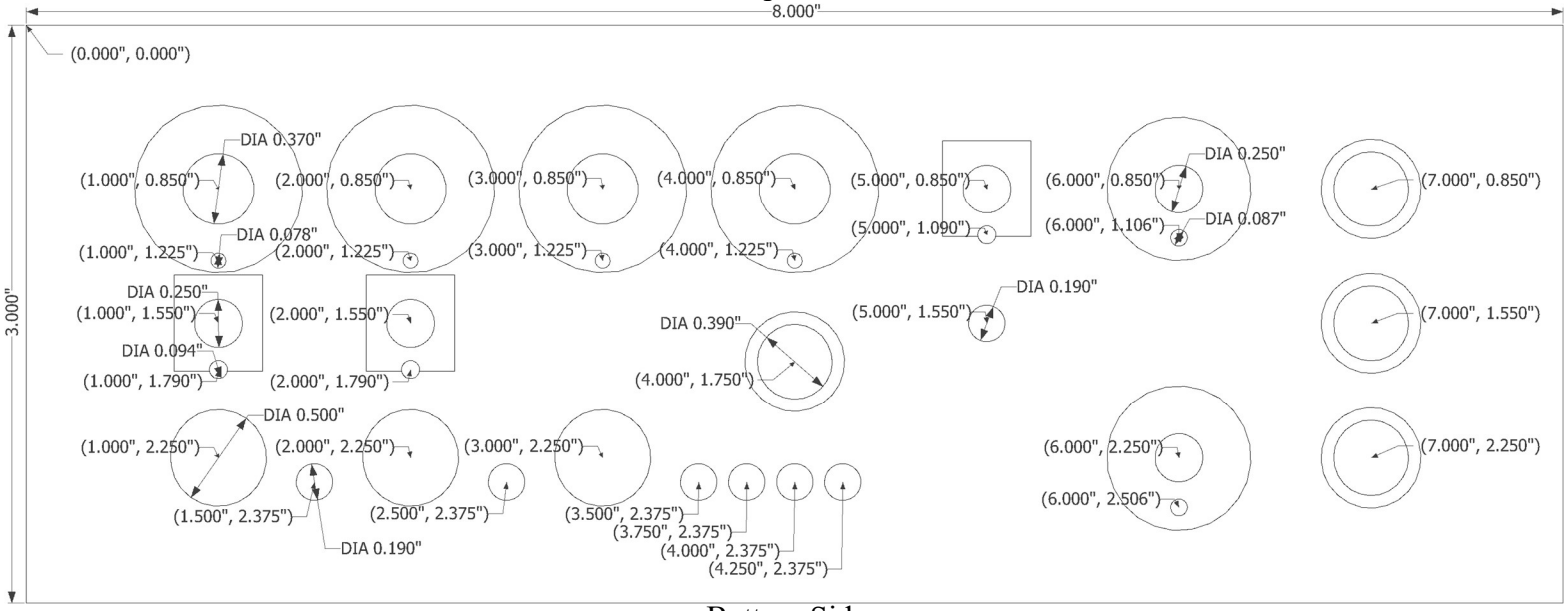
1 LED Dual color R/G
Diameter = 0.19 in.
Front view pin down: Left = RED p-doped (anode)
Right = GREEN p-doped (anode)

1 Power Entry Module:
1 Rectangular 1.94 x 1.17 in. + 2 screw holes separated by 2.20in. 0.135 in. diameter

Front panel design files: PI_FPC.skp, PI_BPC.skp (SketchUp)

Front Panel (Front View)

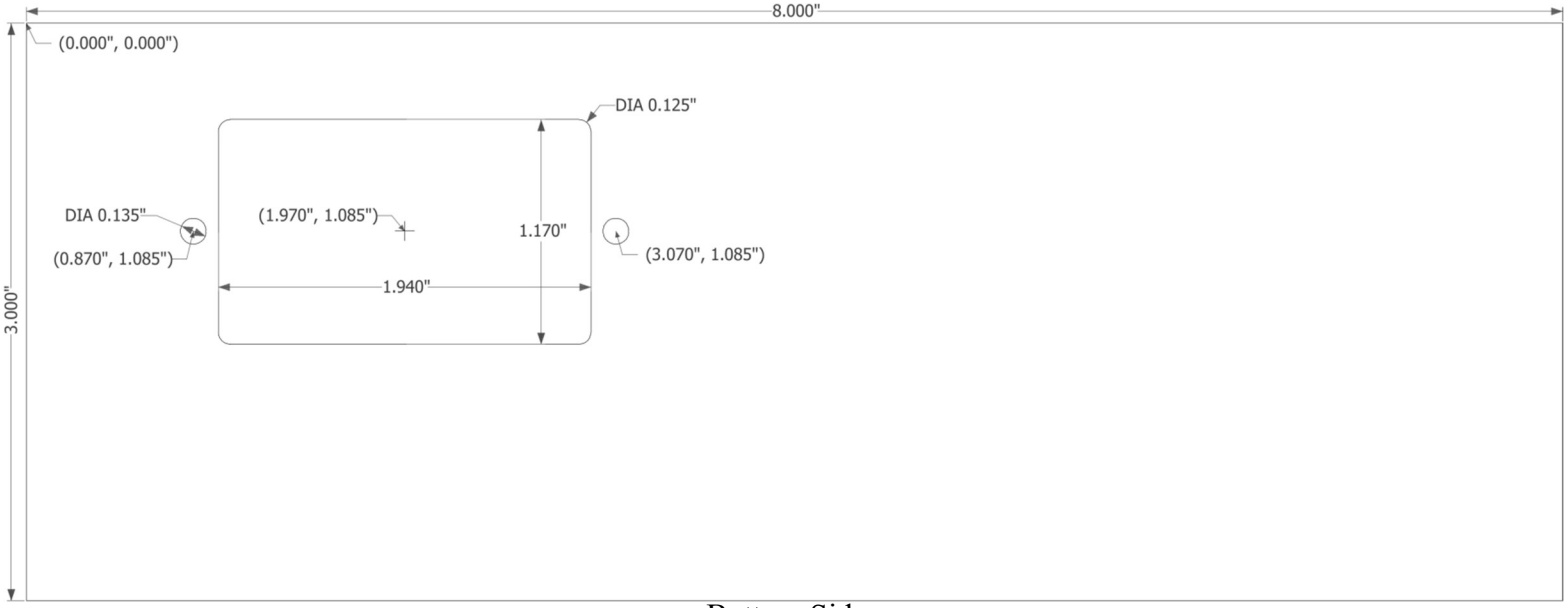
Top Side



Bottom Side

Back Panel (Back View)

Top Side



Bottom Side