Weiwen Jiang

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Research Interests and Specialties

- **Quantum Machine Learning:** we are the first to demonstrate the potential quantum advantage in executing neural networks via co-design, and we open-source the quantum neural network framework QFNN at https://jqub.ece.gmu.edu/categories/QF/ [1][6][8][25][26][32].
- **Co-Design of Neural Architecture and Hardware Accelerators:** we are the first to propose co-design frameworks to explore neural architectures and FPGAs, ASICs, and CiM platforms [3][4][27][9][11][12][2][13][33][34][35][36][37][38][39][40].
- **General Embedded System Design and Optimization:** especially for (1) heterogeneous pipelined MPSoCs [5][15][41][42][47]; (2) asynchronous embedded systems [14][17][18][19][43][44][45][46]; (3) NoC-based MPSoCs [20][21][22][50]; (4) emerging devices: [10][12][16][23][24][51].

Employment

George Mason University — AUG 2021 – NOW. VIGINIA, U.S.
- **Assistant Professor in the Electrical and Computer Engineering Department**

University of Notre Dame (PI: Dr. Yiyu Shi) — JUNE 2019 – AUG 2021. NOTRE DAME, U.S.
- **Postdoctoral Researcher in the Department of Computer Science and Engineering**. Focus on the co-exploration of neural architectures and hardware design, including qauntum computer.

University of Notre Dame (Dr. Jay Brockman) — JAN. 2020 – MAY 2020 NOTRE DAME, U.S.
- **Teaching Assisitant**. CSE20221, Logical Design and Sequential Circuit.

East China Normal University — APR. 2019 – APR. 2020 SHANGHAI, CHINA
- **Guest Research Fellows** in Big Data and Intelligent System Lab.

Education

University of Pittsburgh (PI: Dr. Jingtong Hu) — OCT. 2017 – JUNE 2019 PITTSBURGH, U.S.
- **Joint Ph.D. program in the Department of Electrical and Computer Engineering**. Focus on the co-exploration of neural architecture and hardware design.

Chongqing University (Advisor: Dr. Edwin Sha) — SEPT. 2013 – JUNE 2019 CHONGQING, CHINA
- **Ph.D. degree in Computer Science**. Focus on the embedded system design and optimizations: designing high-performance and low-cost heterogeneous pipelining systems.

Nanjing Agriculture University — SEPT. 2008 – JUNE 2012. JIANGSU, CHINA
- **Bachelor degree in Computer Science**. Major in Network Engineering.

Awards

IEEE Transactions on CAD Donald O. Pederson Best Paper Award (1-2 papers/year)	12/2021
First Place at 31st ACM SIGDA University Demonstration (1 out of 11 teams)	12/2021
Hackathon Top Winning Award at IEEE SERVICES 2020 (2 out of 10 teams)	12/2020
Best Paper Nomination at ASP-DAC 2020 (12 out of 263 submissions)	01/2020. BEIJING
Best Paper Nomination at CODES+ISSS 2019 (3 out of 74 submissions)	10/2019. NEW YORK
Best Paper Nomination at DAC 2019 (5 out of 815 submissions)	06/2019. LAS VEGAS
Best Paper Award at ICCD 2017 (5 out of 258 submissions)	11/2017. BOSTON
Best Student Paper at ESTC 2017	11/2017. CHINA
Best Paper Nomination at ASP-DAC 2016	01/2016. MACAO
Best Paper Award at NVMSA 2015	08/2015. HONGKONG
Editor's pick of the year 2016 in IEEE TC	12/2016. USA
China National Scholarship (1% among all postgraduate students)	11/2017. CHINA

Research & Other Grants

- **PI, LANL**, "Intelligent Quantum Sensing with Quantum Neural Networks", Collaborated with Los Alamos National Lab from NSEC, 01/01/2022-12/31/2022, $80,000 (Funded)
- **PI, NSF-I/UCRC**, "Software Defined FPGA Hardware and Co-Exploration for Real-Time Applications", from EdgeCortix Inc. via NSF IUCRC ASIC center, 10/01/19 - 09/30/20, $100,000 (Co-PI: Prof. Yiran Chen)
- **Co-PI, NSF-IIS**, "RAPID: Collaborative Research: Independent Component Analysis Inspired Statistical Neural Networks for 3D CT Scan Based Edge Screening of COVID-19", 07/01/2020 - 06/30/2021, $98,349 (PI: Prof. Yiyu Shi)
- **Co-PI, Facebook Research Funding** - Towards On-Device AI, "Hardware/Software Co-Exploration of Multi-Modal Neural Architectures Targeting AR/VR Glasses", 04/01/20 - 04/01/21, $75,000 (PI: Prof. Yiyu Shi)
- One Alveo U280 Data Center Accelerator ($6,495) from the Xilinx University Program.
- **Co-PI, NSF**, "EFRI BRAID Preliminary Proposal: Computing with Spikes: a Hierarchical and Cross-layer Exploration Approach" (Pending)
- **PI**, "Co-Exploration of Transformer and Resource-Constrained Hardware Accelerator", from EdgeCortix Inc., 01/01/22 - 01/01/23, $50,000 (Pending)
- **PI, IBM-ND**, "Co-Design Neural Network and Quantum Circuit Towards Quantum Advantage", IBM & University of Notre Dame Quantum program, 11/01/19 - 08/01/21, accessing to IBM Q system
- Research Opportunities Week (ROW) at the Technical University of Munich (TUM), 04/20/2020-04/27/2020 (Cancelled due to COVID-19)
- IEEE Council on Electronic Design Automation (CEDA) for ESWEEK'19, $1,000
- Grants from ACM SIGDA to participate in the HALO workshop in ICCAD'19
- Travel grants from ACM to attend FPGA'19
- Scholarship from SIGDA and IEEE CEDA to attend Ph.D. Forum at DAC'18
- Scholarship from SIGDA and Microsoft to participate Student Research Competition at ICCAD'17

Teaching Experience

Hardware Accelerators for Machine Learning (Lecturer, ECE618)	2022. GEORGE MASON UNIV.
Machine Learning for Embedded Systems (Lecturer, ECE499/590)	2021. GEORGE MASON UNIV.
IBM Qiskit Training Course for Quantum Computing (Lecturer for QML)	2021. UNIV. OF NOTRE DAME
Machine Learning for Embedded Systems (TA, CSE60685)	2020. UNIV. OF NOTRE DAME
Logic Design and Sequential Circuits (TA, CSE20221)	2020. UNIV. OF NOTRE DAME
INVESTING NOW summer program (Volunteer)	JULY 2018. UNIV. OF PITTSBURGH.
High-Performance Parallel Computing (TA for Dr. Edwin Sha)	2014 – 2015. CHONGQING UNIV.

Mentor of Students (Current)

- Yi Sheng, 2021-Now. (Ph.D. candidate at George Mason University)
- Zhepeng Wang, 2021-Now. (Ph.D. candidate at George Mason University)
- Zhirui Hu, 2021-Now. (Research Scholar at George Mason University, will join as Ph.D. in 2022)
- Zhding Liang, 2021-Now. (Co-Advised Ph.D. candidate at the Univerity of Notre Dame)
- Yuhong Song, 2020-Now. (Ph.D. student at East China Normal University) [27]

Mentor of Students (Past)

- Panjie Qi, 2020-2021. (Master student at East China Normal University)
- Shan Hao, 2020-2021. (Master student at East China Normal University)
- Zhuorui Zhao, 2020-2021. (Ph.D. candidate at the University of Notre Dame)
- Colin McDonald, 2020-2021. (CS Junior at the University of Notre Dame, Quantum ML)
- Zheyu Yan, 2019-2021. (Ph.D. candidate at the University of Notre Dame) [12][36]
- Matthew Coffey, Nov. 2020-Jan. 2021. (CS Senior at the University of Notre Dame, Quantum ML)
- Qing Lu, 2018-2021. (Ph.D. candidate at the University of Notre Dame) [37][40]
- Hanjing Zhu, Jun. 2020-Sept. 2020. (Undergraduate student at the University of Notre Dame)
- Alicia Hu, Feb. 2018- May 2018. (Undergraduate student at the University of Pittsburgh)
- Xinyi Zhang, 2017-Dec. 2020. (Ph.D. candidate at the University of Pittsburgh) [3][4][39]
- Hailiang Dong (Master at Chongqing University) [5][16][42][47][48], First Employment: Ph.D. Candidate at the University of Texas at Dallas
- Xinchi Li (Master at Chongqing University) [48], First Employment: Tencent in Chengdu
- Yutong Liang (Master at Chongqing University) [49], First Employment: PingCAP Inc. in Beijing
- Zhulin Ma (Ph.D. candidate at Chongqing University) [16]

Publications

Five Representative Papers

[1] **W. Jiang**, J. Xiong, and Y. Shi, "A Co-Design Framework of Neural Networks and Quantum Circuits Towards Quantum Advantage", **Nature Communications**, 12(1): 1-13, 2021.

[2] **W. Jiang**, L. Yang, E. H.-M Sha, Q. Zhuge, S. Gu, S. Dasgupta, Y. Shi and J. Hu, "Hardware/Software Co-Exploration of Neural Architectures", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***)*, Mar. 2020* (**2021 Donald O. Pederson Best Paper Award, 1 of the 2 selected from all the submissions at TCAD in the past 2 years**)

[3] **W. Jiang**, X. Zhang, E. H.-M. Sha, L. Yang, Q. Zhuge, Y. Shi, and J. Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search," *Proc. Design Automation Conference* (***DAC***), Las Vegas, NV, USA, June. 2019. (5 out of 815 submissions, **Best Paper Nomination**)

[4] **W. Jiang**, E. H.-M. Sha, X. Zhang, L. Yang, Q. Zhuge, Y. Shi, and J. Hu, "Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference", International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS@New York), also appears at ACM Transactions on Embedded Computing Systems (TECS), 2019. (3 out of 74 submissions, **Best Paper Nomination**)

[5] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, H. Dong and X. Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints," *IEEE International Conference on Computer Design* (***ICCD@Boston***) and *in IEEE Transactions on Emerging Topics in Computing* (***TETC***), Jan. 2018. (5 out of 258 submissions, **Best Paper Award**)

Under Review and Work-in-Progress Papers

[6] **W. Jiang**, J. Cong, J. Xiong, and Y. Shi, "Is Quantum Computing Ready for Deep Learning?", under review at **Nature Electronics**.

[7] Y. Sheng, J. Yang, Y. Wu, Y. Shi, J. Hu, **W. Jiang**, L. Yang, "The Larger The Fairer? Small Neural Networks Can Achieve Fairness for Edge Devices", under review at DAC'22.

[8] **W. Jiang**, Y. Ding, and Y. Shi, "Universal Approximability of Deep Learning in Hybrid Quantum-Classical Computing", submitted to ACM TQC.

Journal Papers

[9] Y. Ding, **W. Jiang**, Q. Lou, J. Liu, J. Xiong, X. Sharon Hu, X. Xu, and Y. Shi, "The Impact of Neural Networks' Competency-Awareness on Hardware Design", accepted by **Nature Electronics**, Aug. 2020

[10] **W. Jiang**, B. Xie, C-C Liu and Y. Shi, "Integrating Memristors and CMOS for Better AI", accepted by **Nature Electronics**, Sept. 2019

[11] **W. Jiang**, L. Yang, S. Dasgupta, J. Hu, and Y. Shi, "Standing on the Shoulders of Giants: Hardware and Neural Architecture Co-Search with Hot Start", Accepted by International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS), also appear at IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2020. *(acceptance rate 94/375=25.1%)*

[12] **W. Jiang**, Q. Lou, Z. Yan, L. Yang, J. Hu, X. Hu, and Y. Shi, "Device-Circuit-Architecture Co-Exploration for Computing-in-Memory Neural Accelerators", *IEEE Transactions on Computers* (***TC***), *Apr. 2020*.

[13] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *accepted by CASES 2018* (*in ESWEEK*) and *appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***). *(acceptance rate 67/270=24.8%)*

[14] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***), May 2018.

[15] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Yang, L. Zhou and Q. Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems under Timing Constraint," *in IEEE Transactions on Parallel and Distributed Systems* (***TPDS***), 28(9): 2567-2580, 2017.

[16] E. H.-M. Sha, **W. Jiang**, H. Dong, Z. Ma, R. Zhang, X. Chen and Q. Zhuge, "Towards the Design of Efficient and Consistent Index Structure with Minimal Write Activities for Non-Volatile Memory", *in IEEE Transactions on Computers* (***TC***), 67(3): 432-448, 2018.

[17] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and Lin Wu, "Efficient Assignment Algorithms to Minimize Operation Cost for Supply Chain Networks in Agile Manufacturing," *in Computers & Industrial Engineering*, 108: 225-239, 2017.

[18] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Wu and Q. Zhuge, "Synthesizing Distributed Pipelining Systems with Timing Constraints via Optimal Functional Unit Assignment and Communication Selection," *in Journal of Computational Science*, 26: 332-343, 2018.

[19] **W. Jiang**, Q. Zhuge, X. Chen, L. Yang, J. Yi, and E. H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum Throughput," *in Journal of Signal Processing Systems*, 84(1): 123-137, 2016.

[20] W. Liu, L. Yang, **W. Jiang**, L. Feng, N. Guan, W. Zhang, and N. Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *in IEEE Transactions on Computers* (***TC***), 2018.

[21] L. Yang, W. Liu, **W. Jiang**, M. Li, P. Chen and E. H.-M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era," *in IEEE Transactions on Parallel and Distributed Systems*, Dec. 2016. DOI:10.1109/TPDS.2016.2643669.

[22] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization" *IEEE Transactions on Very Large Scale Integration Systems*, 24(10): 3027-3040, Oct. 2016.

[23] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "A New Design of In-Memory File System Based on File Virtual Address Framework," *in IEEE Transactions on Computers*, 65(10):2959-2972, Oct. 2016.

[24] X. Chen, E. H.-M. Sha, Q. Zhuge, C. J. Xue, **W. Jiang** and Y. Wang, "Efficient data placement for improving data access performance on domain-wall memory" *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 24(10): 3094-3104, 2016.

Conference Papers

[25] Z. Wang, Z. Liang, S. Zhou, C. Ding, J. Xiong, Y. Shi, **W. Jiang**, "Exploration of Quantum Neural Architecture by Mixing Quantum Neuron Designs" *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2021 (Invited Paper)

[26] Z. Liang, Z. Wang, J. Yang, L. Yang, J. Xiong, Y. Shi, **W. Jiang**, "Can Noise on Qubits Be Learned in Quantum Neural Network? A Case Study on QuantumFlow" *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2021 (Invited Paper)

[27] Y. Song, **W. Jiang**, B. Li, Q. Zhuge, E. H.-M. Sha, S. Dasgupta, Y. Shi, C. Ding, "Dancing along Battery: Enabling Transformer with Run-time Reconfigurability", *Proc. Design Automation Conference* ***DAC-21***.

[28] S. Chang, Y. Li, M. Sun, **W. Jiang**, S. Liu, Y. Wang, and X. Lin, "RMSMP: A Novel Deep Neural Network Quantization Framework with Row-wise Mixed Schemes and Multiple Precisions" *Proc. 2021 IEEE/CVF International Conference on Computer Vision* (*ICCV*)

[29] D. Manu, Y. Sheng, J. Yang, J. Deng, T. Geng, A. Li, C. Ding, **W. Jiang**, L. Yang, "FL-DISCO: Federated Generative Adversarial Network for Graph-based Molecule Drug Discovery", *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2021 (Invited Paper)

[30] H. Peng, S. Chen, Z. Wang, J. Yang, S. A. Weitze, T. Geng, A. Li, J. Bi, M. Song, **W. Jiang**, H. Liu, C. Ding, "Optimizing FPGA-based Accelerator Design for Large-Scale Molecular Similarity Search", *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2021 (Invited Paper)

[31] Y. Zhang, Y. Fu, **W. Jiang**, C. Li, H. You, M. Li, V. Chandra, and Y. Lin, "DIAN: Differentiable Accelerator-Network Co-Search Towards Maximal DNN Efficiency", Proc. of ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)

[32] **W. Jiang**, J. Xiong and Y. Shi, "When Machine Learning Meets Quantum Computers: A Case Study," *Proc. of IEEE/ACM Asia and South Pacific Design Automation Conference* (***ASP-DAC***)), 2021 (Invited Paper)

[33] D. Zeng, **W. Jiang**, T. Wang, X. Xu, H. Yuan, M. Huang, J. Zhuang, J. Hu, and Y. Shi, "Towards Cardiac Intervention Assistance: Hardware-Aware Neural Architecture Exploration for Real-Time 3D Cardiac Cine MRI Segmentation," *Proc. of IEEE/ACM International Conference on Computer-Aided Design* (***ICCAD***), 2020 (Invited Paper)

[34] S. Bian, X. Xu, **W. Jiang**, Y. Shi and T. Sato, "BUNET: Blind Medical Image Segmentation Based on Secure UNET", *Proc. Medical Image Computing and Computer Assisted Interventions* (***MICCAI***), Lima, Peru, 2020
(acceptance rate 30%)

[35] X. Yan, **W. Jiang**, Y. Shi and C. Zhuo, "MS-NAS: Multi-Scale Neural Architecture Search for Medical Image Segmentation", *Proc. Medical Image Computing and Computer Assisted Interventions* (***MICCAI***), Lima, Peru, 2020
(acceptance rate 30%)

[36] L. Yang, Z. Yan, M. Li, H. Kwon, L. Lai, T. Krishna, V. Chandra, **W. Jiang**, Y. Shi, "Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *Proc. Design Automation Conference* (***DAC***), San Francisco, July 19-23.
(acceptance rate 228/992=23.0%)

[37] S. Bian, **W. Jiang**, Q. Lu, Y. Shi, and T. Sato, "NASS: Optimizing Secure Inference via Neural Architecture Search", *24th European Conference on Artificial Intelligence* (***ECAI'20***)
(acceptance rate 365/1363=26.8%)

[38] L. Yang, **W. Jiang**, W. Liu, E. H.-M. Sha, Y. Shi, and J. Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence," *Proc. Asia and South Pacific Design Automation Conference* (***ASP-DAC***), Beijing, Jan. 2020. (12 out of 263 submissions, **Best Paper Nomination**)

[39] X. Zhang, **W. Jiang**, Y. Shi and J. Hu, "When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design," *Proc. IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI*), Miami, Florida, USA, Aug. 2019. (Invited Paper)

[40] Q. Lu, **W. Jiang**, X. Xiao, J. Hu and Y. Shi, "On Neural Architecture Search for Resource-Constrained Hardware Platforms," *Proc. IEEE/ACM International Conference On Computer-Aided Design* (*ICCAD*), Westminster, CO, 2019. (Invited paper)

[41] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and X. Chen, "Optimal Functional-Unit Assignment and Buffer Placement for Probabilistic Pipelines," *Proc. International Conference on Hardware/Software Co-design and System Synthesis* (***CODES+ISSS***), Pittsburgh, PA, USA, Oct. 2016.
(acceptance rate 21/80=26.3%)

[42] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, H. Dong, and X. Chen, "Optimal Functional Unit Assignment and Voltage Selection for Pipelined MPSoC with Guaranteed Probability on Time Performance," *Proc. Languages, Compilers, and Tools for Embedded Systems* (***LCTES***), Barcelona, Spain, June 2017.
(acceptance rate 13/51=25.5%)

[43] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, L. Yang and X. Chen, "On the Design of High-Performance and Energy-Efficient Probabilistic Self-Timed Systems," *Proc. High Performance Computing and Communications* (***HPCC***), NewYork, NY, USA, Aug. 2015.

[44] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "Prevent Deadlock and Remove Blocking for Self-Timed Systems," *Proc. International Conference on Algorithms and Architectures for Parallel Processing* (***ICA3PP***), Zhangjiajie, China, Nov. 2015.

[45] **W. Jiang**, E. H.-M. Sha, X. Chen, Q. Zhuge and L. Wu, "Optimal Functional Assignment and Communication Selection under Timing Constraint for Self-Timed Pipelines," *Proc. IEEE International Conference on Embedded Software and Systems* (***ICESS***), Chengdu, China, Aug. 2016.

[46] **W. Jiang**, Q. Zhuge, J. Yi, L. Yang and E. H.-M. Sha, "On self-timed ring for consistent mapping and maximum throughput," *Proc. Embedded and Real-Time Computing Systems and Applications* (***RTCSA***), Chongqing, China, Aug. 2014.

[47] E. H.-M. Sha, H. Dong, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "On the Design of Reliable Heterogeneous Systems via Checkpoint Placement and Core Assignment," *Proc. Great Lakes Symposium on VLSI* (*GLSVLSI*), Chicago, IL, USA, May 2018.

[48] X. Li, Q. Zhuge, **W. Jiang**, H. Dong, W. Lin, X. Chen and E. H.-M. Sha, "A Research of Reducing Write Activities in Multi-table Join for Non-Volatile Memories," *Proc. 15th CCF Annual Conference on Embedded Systems* (*ESTC*), Shenyang, China, Nov. 2017. (**Best Student Paper Award**)

[49] E. H.-M. Sha, Y. Liang, **W. Jiang**, X. Chen and Q. Zhuge, "Optimizing Data Placement of MapReduce on Ceph-Based Framework under Load-Balancing Constraint," *Proc. International Conference on Parallel and Distributed Systems* (***ICPADS***), Wuhan, China, Dec. 2016.

[50] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H.-M. Sha, "FoToNoC: A hierarchical management strategy based on folded lorus-like Network-on-Chip for dark silicon many-core systems," *Proc. 2016 21st Asia and South Pacific Design Automation Conference* (***ASP-DAC***), Macao, Jan. 2016. (**Best Paper Nomination**)

[51] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "Designing an Efficient Persistent In-Memory File System," *Proc. the 4th IEEE Non-Volatile Memory System and Applications Symposium* (***NVMSA***), Hongkong, Aug. 2015. (**Best Paper Award**)

Book

[1] **W. Jiang**, J. Hu, and Y. Shi, "Software/Hardware Co-Design for Deep Learning Accelerators," *Springer Nature* (*Pass the new book proposal*)

Invited Talks (not include job talk)

- Invited Talk in Road4NN workshop at DAC'21
- Villanova University (host: Prof. Xun Jiao)
- ICCAD Special Session.
- Indiana University (host: Prof. Lei Jiang)
- IEEE QuantumWeek'21 for QuantumFlow Tutorial.
- ESWEEK'21 for QuantumFlow Tutorial.
- University of Delaware (host: Prof. Chenmo Yang), May. 12, 2021
- tinyML talks webcast, Dec. 8, 2020
- Southeastern University (host: Prof. Qi Zhu), Dec. 2020
- Rice University (host: Prof. Yingyan Lin), Nov. 2020
- University of New Mexico (host: Prof. Lei Yang), Nov. 2020
- tinyML Asia talk, Nov. 19, 2020
- Zhejiang University (host: Prof. Chen Zhuo), Oct. 2020
- University of Science and Technology of China (host: Prof. Yu-Chun Wu), Oct. 2020
- IBM Quantum Summit, Sept. 2020
- Workshop on Research Open Automatic Design for Neural Networks (ROAD4NN), July 2020

- Workshop on Hardware and Algorithms for Learning On-a-chip (HALO), Nov. 2019
- Northeastern University (host: Prof. Yanzhi Wang), Oct. 2019
- Technical Webinar of NSF IUCRC for ASIC, Aug. 2019

Professional Services

Journal Editor:

- Associate Editor for IEEE Transactions on Circuits and Systems II: Express Briefs
- Guest Editor for Electronics on Special Issue "Quantum Machine Learning: Theory, Methods and Applications"
- Guest Editor for IEEE Transactions on Circuits and Systems II: Express Briefs on ISICAS 2021 Special Session

Conference Technical Program Committee:

- Design Automation Conference (DAC 2021, 2022)
- Design, Automation and Test in Europe Conference (DATE 2022)
- International Conference On Computer Aided Design (ICCAD 2021)
- Asia and South Pacific Design Automation Conference (ASP-DAC 2021, 2022)
- IEEE Computer Society Annual Symposium on VLSI (ISLVLSI 2020)
- ACM Great Lakes Symposium on VLSI (GLSVLSI 2020,2021)
- ACM/SIGAPP Symposium On Applied Computing (SAC 2020,2021)
- IEEE International System-on-Chip Conference (IEEE SOCC 2020)
- Late Break Results in Design Automation Conference (LBR-DAC 2020)
- Student Research Forum at Asia and South Pacific Design Automation Conference (ASP-DAC 2020,2021)
- IEEE Real-Time Systems Symposium (RTSS 2019, Artifact Evaluation Committee)

Journal Reviewer

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration (TVLSI)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
- IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)
- IEEE Embedded System Letter (ELS)
- IEEE Access
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Journal on Emerging Technologies in Computing (JETC)
- Journal of Parallel and Distributed Computing (JPDC)
- Journal of Computer Science and Technology (JCST)
- Communications in Statistics - Simulation and Computation

- Microprocessors and Microsystems (MICPRO)
- SPRINGER Journal of Signal Processing Systems (JSPS)
- HINDAWI Complexity (Complexity)
- Mathematics

Internal Services

Distinguish Speaker Committee:

- Invited Robert Wille for a talk on Quantum Computing in ECE