Abstract : This presentation describes the More Than Moore, Beyond CMOS technology, which have long been expected to be key technologies for realizing high value-added semiconductor integrated circuits toward the upcoming 2030.

The latter part addresses the impact of delays caused by parasitic RCs that designers need to overcome and the overview of LDE (Layout Dependence Effects) will be summarized. As an additional topic, the layout techniques for designing high-speed transistors that can overcome aforementioned RC delays and surpass More Than Moore is introduced in the presentation.