 A screenshot of a computer

AI-generated content may be incorrect.

**Answer to “Are these models passing with a 1 ns clock constraint?”**  
No. With the “Default Clock Constraints” (around 1 ns period / 1 GHz), all four corners show **negative slack** in the table (e.g.\ −1.188 ns, −1.305 ns, etc.), indicating the design **fails** timing at 1 ns.

**Updated Results and Observations**  
From the “Updated Clock Constraints” table, you can see that the *Fmax* has dropped from around 457 MHz–433 MHz down to about 317 MHz–313 MHz in the slow corners. This is **why** the slack turned positive: the clock period is now relaxed enough that the design meets timing. The setup time numbers have become much larger (e.g., 16.8 ns to 18 ns) because there is more clock period available in the new, slower constraint.

1. **Why is the Fmax different?**  
   Because we have relaxed the clock constraint (a longer clock period), the design can now meet timing, but at a lower maximum frequency (317 MHz instead of 457 MHz).
2. **What about the setup time?**  
   The reported “setup time” in the timing tool is now larger (on the order of 16–18 ns) because the clock period is longer. Effectively, the circuit has more time to settle data before the latch edge.

**New Slack for the Previously Failing Path**  
Looking at the failing path under “Slow 1100 mV 85 °C” (which had −1.188 ns slack before), the updated report shows:

* **Slack**: +17.776 ns
* **Clock Delay**: 4.111 ns
* **Data Delay**: 1.937 ns

Yes, it is now passing. Comparing to the original numbers (4.112 ns clock delay, 1.947 ns data delay, −1.188 ns slack), the *clock delay* and *data delay* are almost the same. The big difference is the **clock period** is now much larger, so the path has plenty of margin (hence **+17.776 ns** slack instead of **−1.188 ns**).

