g55_dealer - Pseudo-Random Card Dealer

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1 Circuit Description

The *g55_dealer* circuit is a finite state machine (FSM) that manages other components that together allow for a random card to be drawn from a standard 52 card deck held in a *g55_stack52* circuit. The circuit has four 1-bit inputs (`request_deal`, `RAND_LT_NUM`, `reset`, and `clock`) and two 1-bit outputs (`stack_enable` and `rand_enable`). `request_deal` is high when a random card is needed from the deck, `RAND_LT_NUM` is high if the pseudorandom number is less than the total number of cards in the deck, `reset` is the asynchronous reset, and `clock` is the clock signal for the entire circuit usually at 50 MHz. `stack_enable` is a signal allowing operations to occur on the stack, namely the POP operation to fetch a card. `rand_enable` is the signal to get a new pseudorandom number from *g55_randu*.

A pinout of the circuit is as follows:

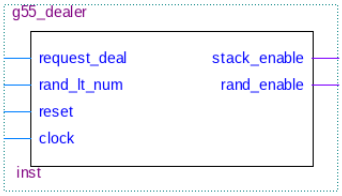

Figure 1: *g55_dealer* Pinout

Table 1: *g55_dealer* Finite State Machine

Inputs		State		Outputs	
request_deal	RAND_LT_NUM	State	Next State	stack_enable	rand_enable
0	X	00	01	0	0
1	X	00	00	0	0
0	X	01	01	0	0
1	X	01	11	0	0
X	0	11	11	0	1
X	1	11	10	0	1
X	X	10	00	1	0

2 Testing

The *g55_dealer* circuit was tested using a testbench and timing simulation. For the timing simulation, the circuit was stepped through the different states by varying the inputs as necessary. The delay in the circuit between a change in inputs and it being reflected in the simulation is clearly shown, and small enough to not cause any problems. The testbench was to test the *g55_dealer* with other components and start putting everything together for the Crazy Eights circuit. Since everything worked together with this basic form of the testbench only containing the stack, random number generator, a comparator circuit, and a seven segment decoder, the *g55_dealer* must be working as intended.

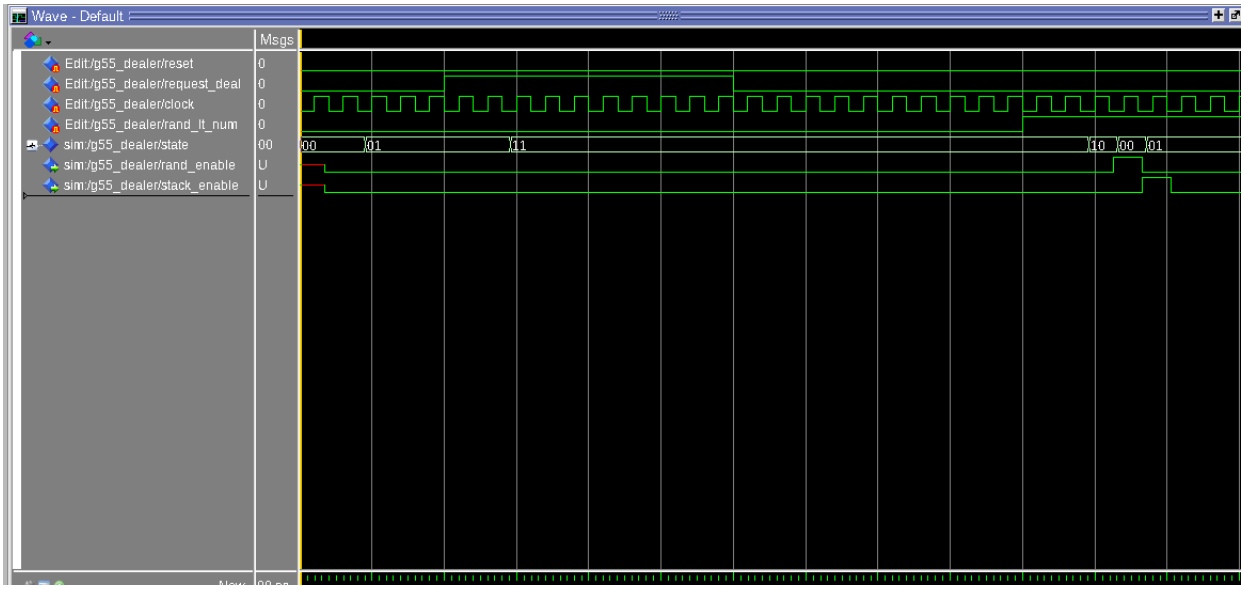

Figure 2: *g55_dealer* Timing Simulation Results

3 FPGA

The *g55_dealer* circuit uses a total of 5 logic elements on the FPGA, 4 combinational functions, and 4 dedicated logic registors according to the Flow Summary generated after compilation. All of these represent a use of less than 1% of FPGA resources. As there are six inputs and outputs, six of the pins must be used. The timing analysis shows positive slack for all connections, meaning signals pass through the system on all paths sufficiently fast for the circuit to work as desired. However the slack is small, so increasing the clock frequency by a significant amount would prevent the circuit from operating as intended.