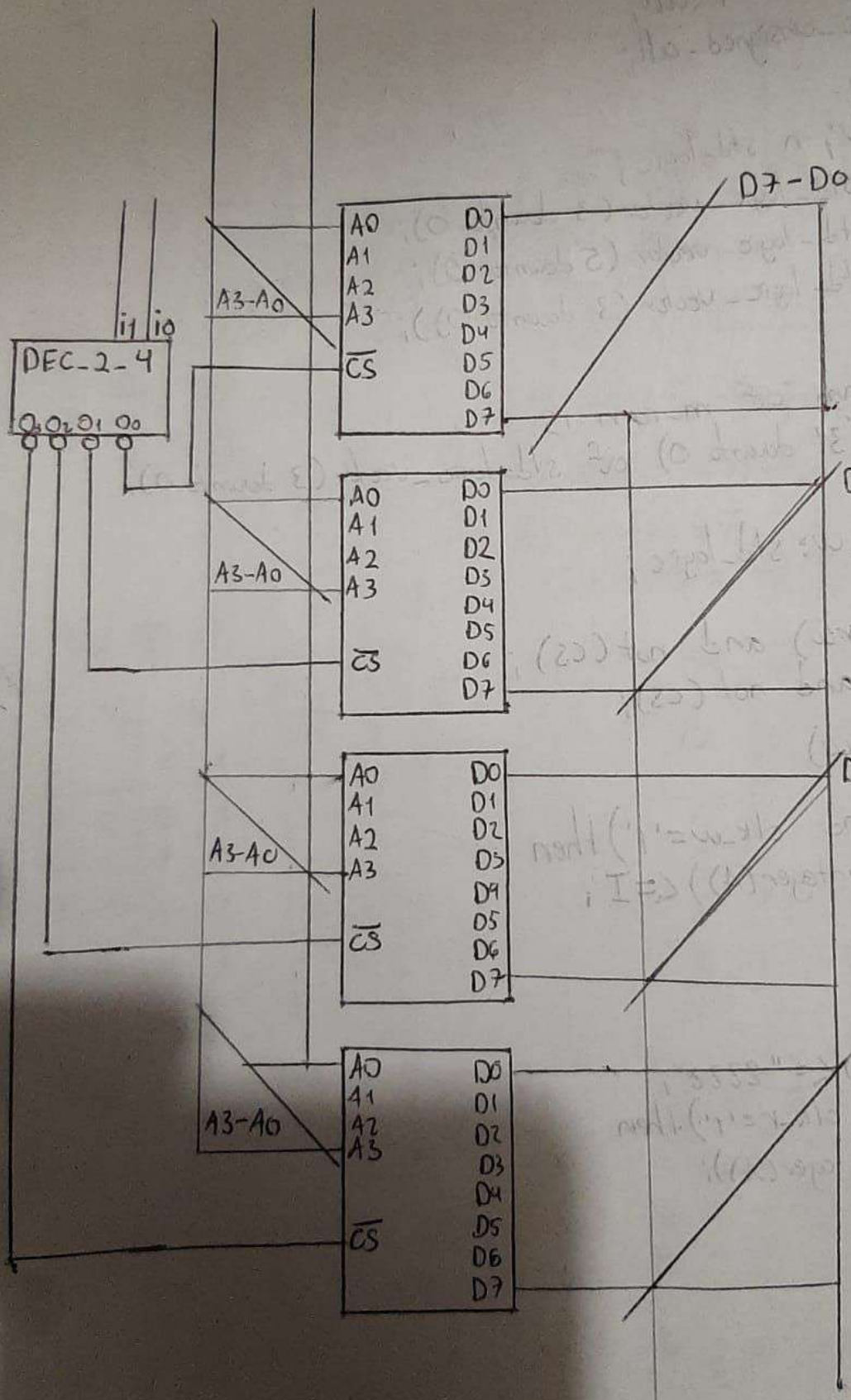
Examen DSD Hernández Sánchez Juan René

1) Dibujar un arreglo de memorias ROM de 64x8 utilizando memorias 16x4



2) Escribir codigo en VHDL Para una memoria RAM de 32x4

```
Library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity m_ram is
    port ( cs, rw: in std_logic;
           I: in std_logic_vector(3 downto 0);
           A: in std_logic_vector (4 downto 0);
           O: out std_logic_vector (3 downto 0));
end m_ram;
architecture mem_ram of m_ram is
type ram is array(31 downto 0) of std_logic_vector(3 downto 0);
Signal dato: ram;
Signal clk_r, clk_w: std_logic;
begin
    clk_w <= not(rw) and not(cs);
    clk_r <= rw and not(cs);
escritura: process (clk_w)
begin
    if(clk_w'event and clk_w='1') then
        dato(conv_integer(A)) <= I;
    end if;
end process;
Lectura: process (clk_r)
begin
    if (cs='1') then O <= "ZZZZ";
    elsif(clk_r'event and clk_r='1') then
        O <= dato(conv_integer(A));
    end if;
end process;
end mem_ram;
```

3) A partir del siguiente circuito obtener el Diagrama de estados

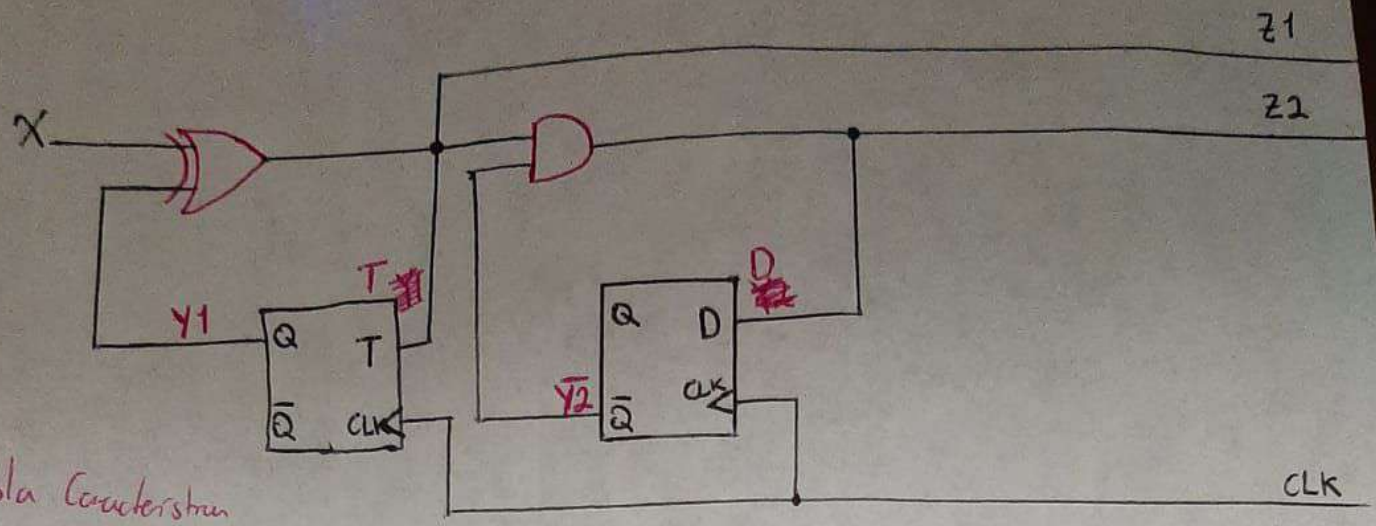


Tabla Característica

T	Q_+	$T Q_+$
0	0	0
0	1	1
1	0	1
1	1	0

$D = (X \oplus Y_1)\bar{Y_2} = (X\bar{Y_1} + \bar{X}Y_1)\bar{Y_2} = X\bar{Y_1}\bar{Y_2} + \bar{X}Y_1\bar{Y_2}$

$T = (X \oplus Y_1) = X\bar{Y_1} + \bar{X}Y_1$

$Z_1 = (X \oplus Y_1) = X\bar{Y_1} + \bar{X}Y_2$

$Z_2 = (X \oplus Y_1)\bar{Y_2} = X\bar{Y_1}\bar{Y_2} + \bar{X}Y_1\bar{Y_2}$

Para T Y1

Y_2	Y_1	X=0	X=1
0	0	0	1
0	1	1	0
1	1	1	0
1	0	0	1

Para Y1

Y_2	Y_1	X=0	X=1
0	0	0	1
0	1	0	1
1	1	0	1
1	0	0	1

Para D Y2

Y_2	Y_1	X=0	X=1
0	0	0	1
0	1	1	0
1	1	0	0
1	0	0	0

	X=0	X=1
A	A/00	C/11
B	D/01	B/10
C	A/00	B/10
D	A/00	B/10

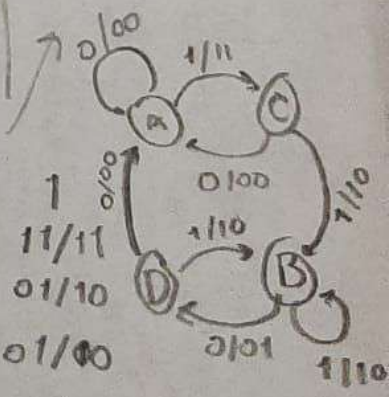
Para Z1

Y_2	Y_1	X=0	X=1
0	0	0	1
0	1	0	1
1	1	0	1
1	0	0	1

Para Z2

Y_2	Y_1	X=0	X=1
0	0	0	1
0	1	1	0
1	1	0	0
1	0	-	0

Para X	0	1
Y_2 Y_1		
A 0 0	00/00	11/11
B 0 1	10/01	01/10
C 1 1	00/00	01/10
D 1 0	00/00	01/10



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