Specimen Class Test

1. Module number	CSN08101
2. Module title	Systems & Services
3. Module leader	Dr A Armitage
4. Tutor with responsibility for this Assessment	*AFA and FG*
5. Assessment	*Specimen class test*
6. Weighting	*50%*
7. Size and/or time limits for assessment	*1 hour.*
8. Deadline of submission	*Not applicable.*
9. Arrangements for submission	*Not applicable.*
10. Assessment Regulations **All assessments are subject to the University Regulations.**	*No exemptions.*
11. The requirements for the assessment	*See below.*
12. Special instructions	*None.*
13. Return of work	*Specimen test only*
14. Assessment criteria	*See Attached.*

Matriculation No :	**Mark Awarded : /50**

INSTRUCTIONS:

Enter your answer in the space provided below each question. If you require additional space for an answer, use the blank space on the reverse side of each question sheet.

- **Answer FIVE questions.**
- **Answer TWO questions from each section and any ONE other.**

Additional Reference Material Provided : Appendix A – System Reference Diagram.

SECTION A

1.	a) A typical PC motherboard will be based round a chipset that can't be changed, except by buying a new board. However many components that can be plugged into the motherboard can be changed. List three items on, or directly connected to, a motherboard that a socket is provided for, with the possibility of using different components in the sockets.	(3)
	b) Explain why the Graphics & Memory Controller Hub (GMCH) on a PC motherboard has to be physically close to the processor (increasingly on the same chip), while the I/O hub can be further away.	(3)
	c) Several methods are being used to speed up the communication between the processor through the GMCH to the rest of the motherboard. Describe one such method.	(4)
	Solution :	

2. (a) Explain the purpose of the flags in a processor such as the Pentium. Give an example of how one of the flags might be used.
 	
(b) Explain what each line of the following Pentium program does:
 	
mov eax, [0x8aa80000]
mov ebx,0xff001234
sub eax,ebx
jnz program_end
	(3)
	
	(7)

Solution : (a)
 	
(b)
mov eax, [0x8aa80000]
 	
mov ebx,0xff001234
 	
sub eax,ebx
 	
jnz program_end
 	
.	

3. a) Describe what an instruction pipeline is and how it speeds up the execution of instructions compared to a processor that does not have a pipeline. b) The ARM series of processors use RISC style instructions. Describe why it is easier to implement an instruction pipeline for this type of processor than it is for a CISC processor such as a Pentium. c) Describe what the Jazelle instruction set is, and give an example of where it is used.	(4) (3) (3)
Solution :	

4. a) More and more PCs are becoming available in 64 bit versions, rather than 32 bits. Explain what this means for the internal organization of the processor and the external buses. b) A typical cache line size might be 32 or 64 bytes. Explain what this means, describe how a line is fetched into the cache from RAM and discuss why this affects the way that DRAM needs to work.	(5) (5)
Solution :	

SECTION B

5. For the generic I/O interface shown in Figure Qu5 : i. Describe the typical functions performed by Status, I/O DATA 2 and DAC aces.	(5)
ii. Describe, as a step-by-step sequence, how the processor reads a byte of data from the ADC register.	(5)

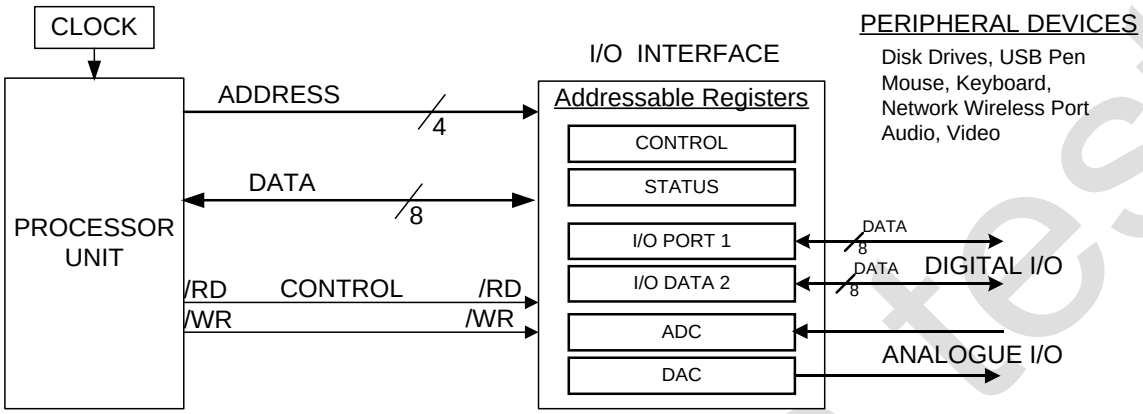


Figure Qu5.

Solution :

6. With reference to the System Diagram in Appendix A describe the sequence of actions that processor takes when it receives a Direct Memory Access request REQ1 on the SERIAL I/O Channel.	(10)
Solution :	

7. Serial Advanced Technology Attachment (SATA) is the latest step in the evolution of disk drive interfaces. Describe the main features of the SATA interface paying particular attention to data transfer speed and connection technology.	(10)
Solution :	

8. Figure Qu8 shows a block schematic for a typical PC Video Capture Card. Give an overview of the capture card operation paying particular attention to the function of the ADC converters, Memory buffer, DMA Controller and PC bus interface. (10)

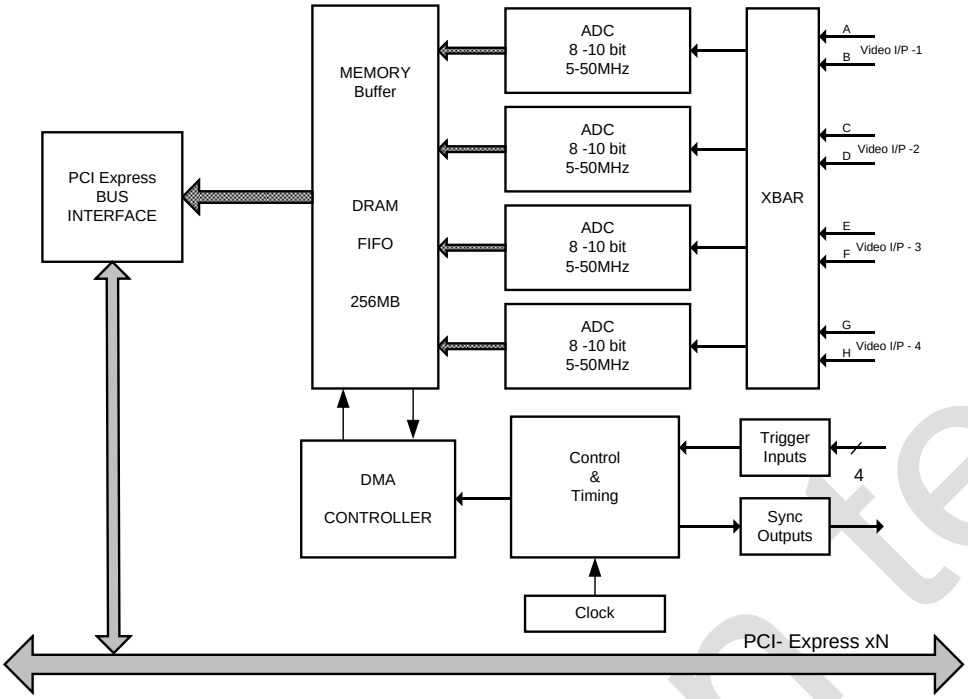


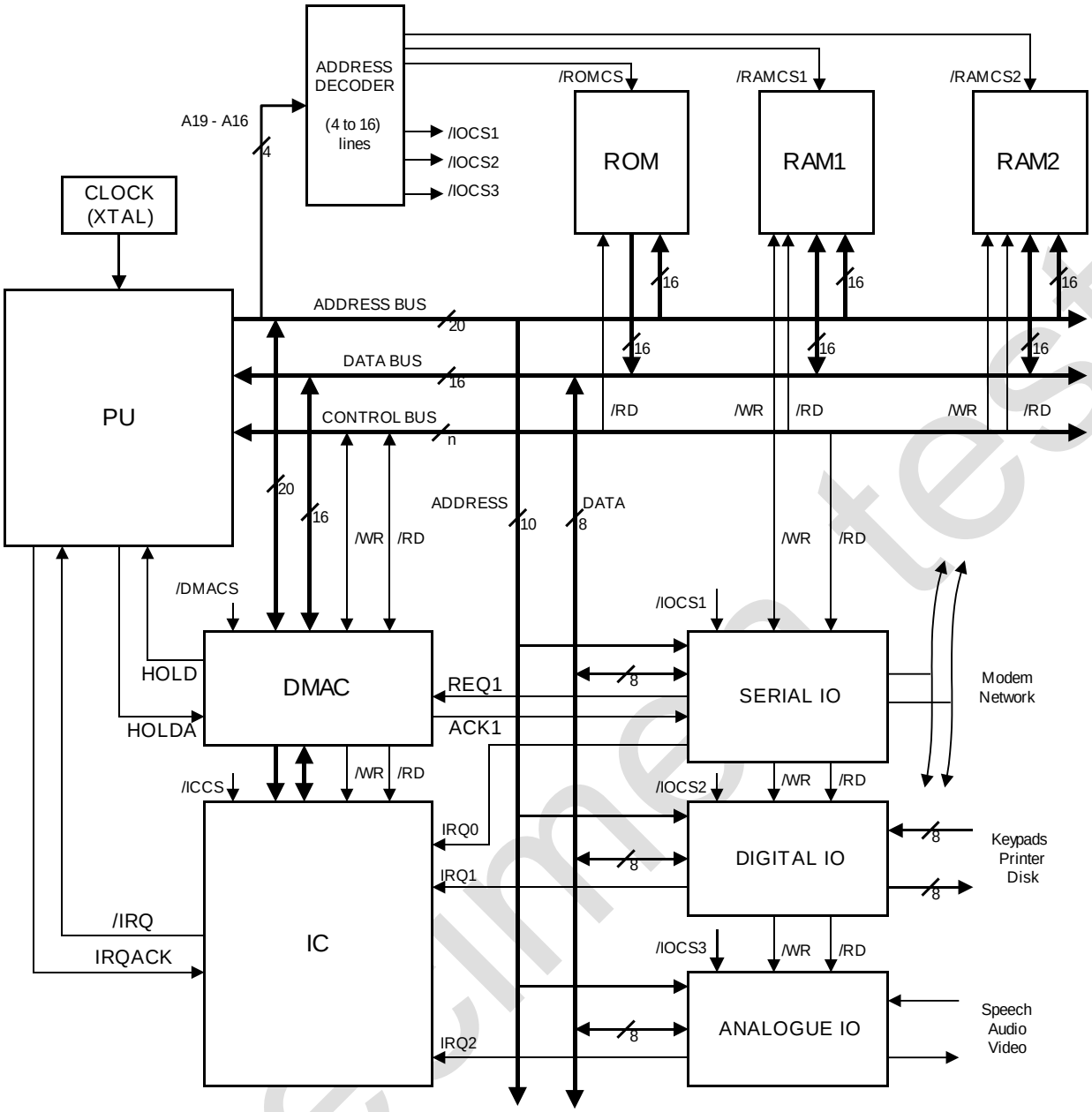
Figure Qu8.

Solution :

EDINBURGH NAPIER UNIVERSITY

SCHOOL OF COMPUTING

APPENDIX A - SYSTEM REFERENCE MODEL



DEVICE DESCRIPTIONS

DEVICE		MEANING
PU	:	Processor Unit
ROM	:	Read-Only Memory
RAM	:	Random Access Memory
IO	:	Input-Output
IC	:	Interrupt Controller
DMAC	:	Direct Memory Controller

SIGNAL DESCRIPTIONS

SIGNAL LINE		MEANING
CS	:	Chip Select
RD	:	READ
WR	:	WRITE
REQ	:	DMA REQuest
ACK	:	Acknowledge
IRQ		Interrupt Request