Revision topics for Computer Architecture block

The following is a summary of the main topics that might feature in the class test for the Computer Architecture section of the Systems & Services module

UNIT 1

Main internal blocks of a processor (e.g. Pentium or 8051 microcontroller)

Fetch Execute cycle & Machine code

Instruction Fetch:

- The address in the PC (Program Counter) is sent out of the processor via the Bus Interface Unit (BIU).
- The contents of that memory location are read from the memory into the BIU.
- The contents pass from the BIU to the IR (Instruction Register).
- The PC is incremented .

Execute: depends on instruction, but typically involves performing arithmetic/logic or fetching storing operands.
Two broad types of instruction: Complex instruction (e.g. Pentium) and Reduced Instruction Set (e.g. Sparc).
Relation between assembly language and object code/machine code.

UNIT 2

PC Architecture

Brief descriptions of:
Hub-based architectures
Chipsets:

- Graphics & Memory Controller
- I/O Chip Hub
- Flash BIOS

Multiple Processor systems
Relative speeds of buses
Trends: GM hub as part of processor/netbook style with single hub

Motherboards

Chip-set
Standard connections: Disk drives, USB
Sockets/slots for:

- processor
- RAM
- Graphics card (PCI-express)
- PCI cards

Things that may be built in:

- LAN, sound system, modem connection, Firewire

Inside the Pentium

Main functional blocks: (Instruction and data caches, memory management unit, decode units, control unit)
Registers (Data, pointer and status). Difference between EAX, AX, AL Pipeline to speed up instruction execution.
Problems with branches. Pentium uses Complex Instruction Set (needs broken down into simpler microcode)

Pentium assembly language

- MOV, ADD, SUB instructions (e.g. add 2 numbers, subtract 2 numbers). Examples would use small hexadecimal numbers with no carry, e.g. 20 + 08 = 28 or 15 -15 = 0
- MOV destination source
- Flags: indicate status after arithmetic/logic
- Zero flag: SET to 1 if result is zero
- Conditional jumps depending on result, e.g. JZ (jump if zero).
- Addressing modes:
  - Registers e.g. MOV EAX, EBX
  - To/from memory either by variable name: MOV Var1, AX
  - Or by reference to address: MOV EAX, [21AF0000]
- Looping using the ECX register as a counter

The ECX register automatically decremented by the LOOP instruction

UNIT 3

RISC

Reduced Instruction Set Computers. Used in, for instance, Sun SPARC stations. Simple instructions, all the same length. Many general purpose registers. Pipelining, and methods of coping with branches. Need for intelligent compilers.

ARM

Typical applications. Main features: Load/store architecture. Registers, Thumb architecture, Jazelle architecture.

Memory

DRAM: dynamic ram (needs refreshed). Row and column address. Memory modules: DIMM. Speed relative to microprocessor. Synchronous (SDRAM) & Double Data Rate (DDR). Clock rate and bandwidth. Latency. Rambus

Cache

Reasons for using: relative speeds of ram and cache and processor. Order of searching cache levels then RAM. Principle of locality. Location: I and D cache for level 1, combined cache for level 2. Cache lines (typically 16-64 bytes). Write policy (write-through vs write-back). Mapping: direct, fully-associative and set-associative (and what these mean).

UNIT 4

Computer Systems Architecture

Device addressing: address decoding and chip selects.

IO data transfers: reading and writing data.

Programmable IO interfaces – registers – IO Port ADC, Status, Control etc

Analogue I/O

Signal digitisation, Sampling rates, ADC resolution. Basic operating principles of ADCs and DACs

I/O Techniques: Software polling

Flag polling. Relatively poor efficiency.

I/O Techniques: Interrupts

Interrupts as hardware signals that interrupt the processor. The sequence of system operations required to handle and process interrupts:

Typical sources of interrupts. Multiple Interrupts. Basic functions of the Interrupt Controller (Interrupt identification, prioritisation and masking), Interrupt Vector Table and Stack memory.

I/O Techniques: Direct Memory Access (DMA)

DMA Controller and DMAC architecture. Source and destination address registers and word count Block burst and cycle steal modes of transfer.

Operating Systems and I/O

Operating Systems levels: kernel and user mode. I/O manager, device drivers, Hardware Abstraction Layer.

UNIT 5

BUS SYSTEMS

The principles of parallel and serial data transfers systems and be able to compare their inherent strengths and weaknesses. The concept of layered interfaces and protocol stacks applied to bus systems, basic operating principles, together with the physical interface, topology, data rate and main features of the common bus systems - PCI Express, USB2.0 and 3.0 and SATA

UNIT 6

Peripheral Interface Devices

Understands the basic architecture of common I/O interface subsystems – sound, video, graphics and network. The features to be described are : the use of signal acquisition elements such as ADC, DAC and Multiplexer; the use of memory and on-board processors; the s