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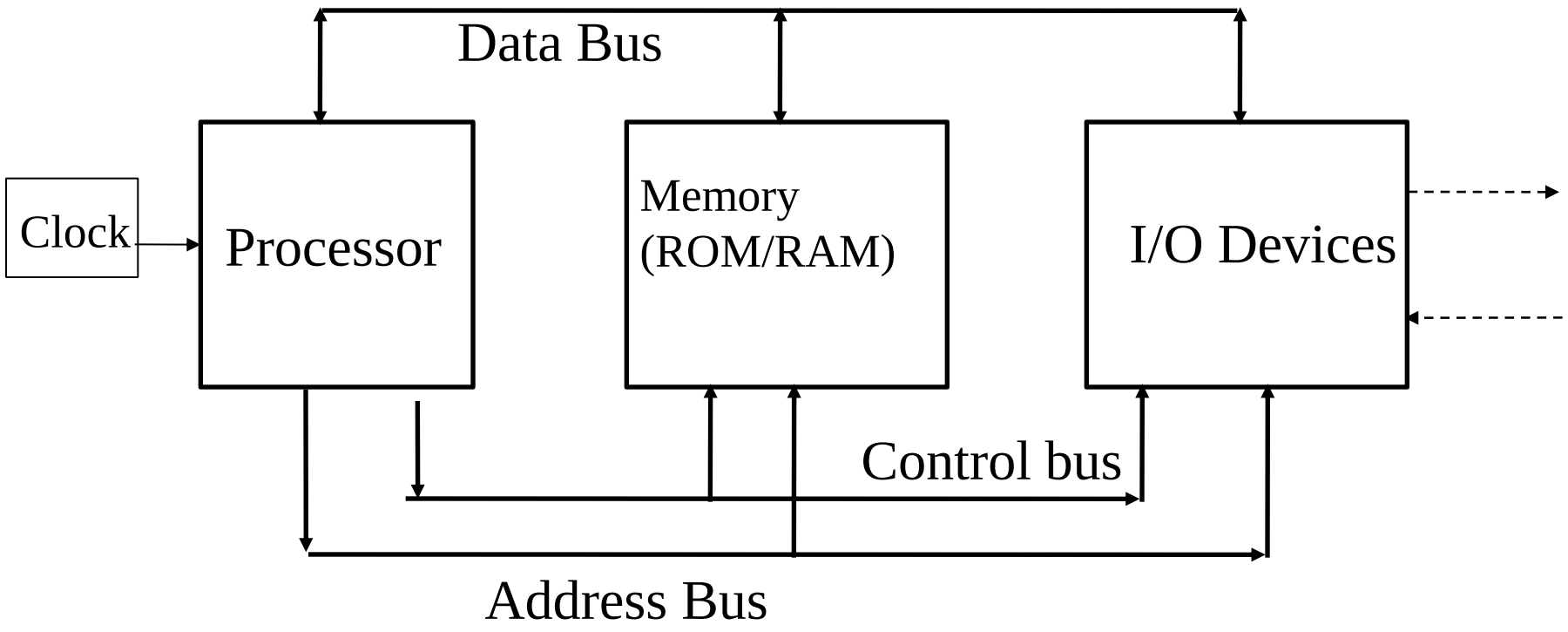
CSN08101: PC System Architecture

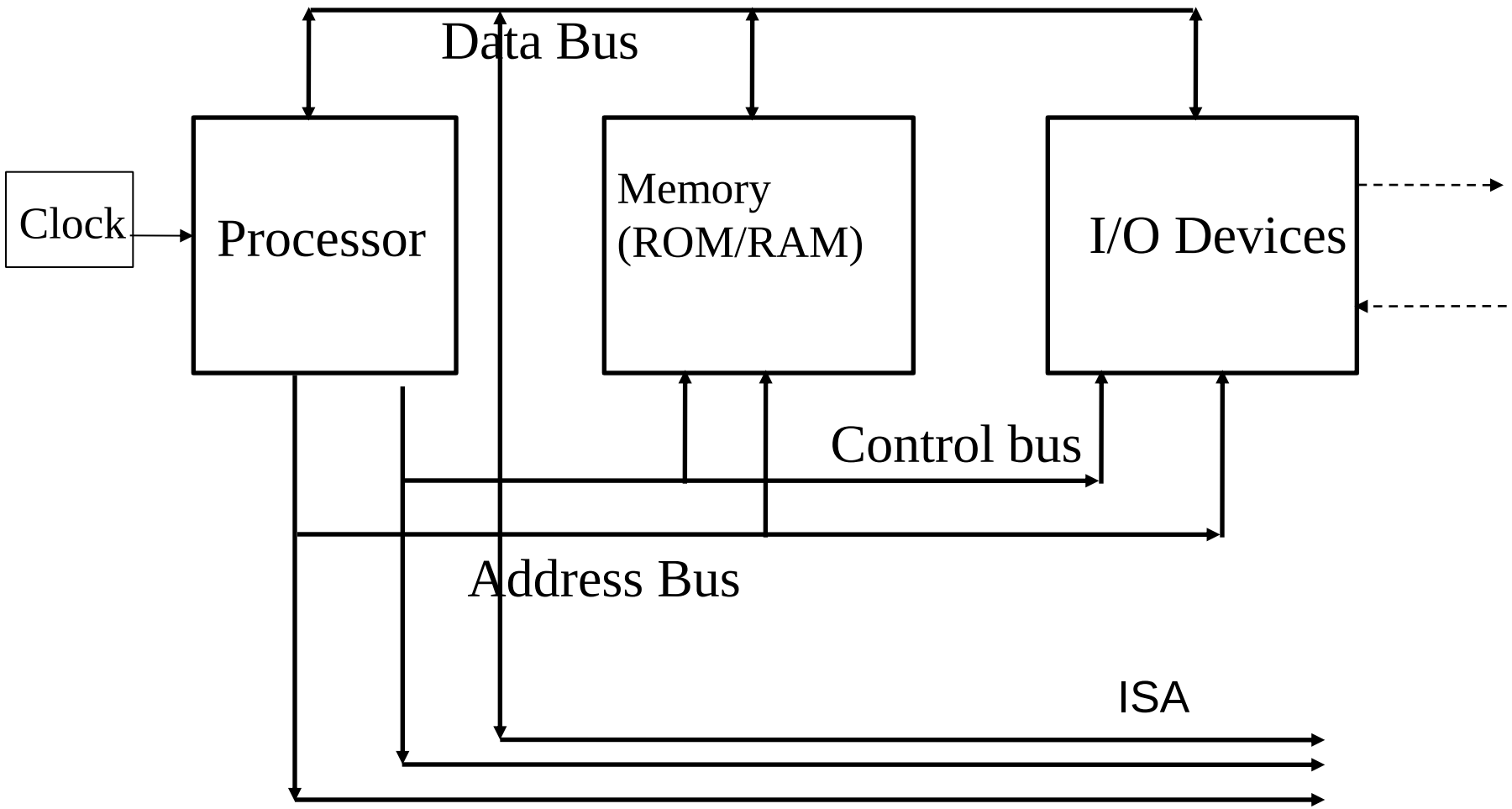
Contents:

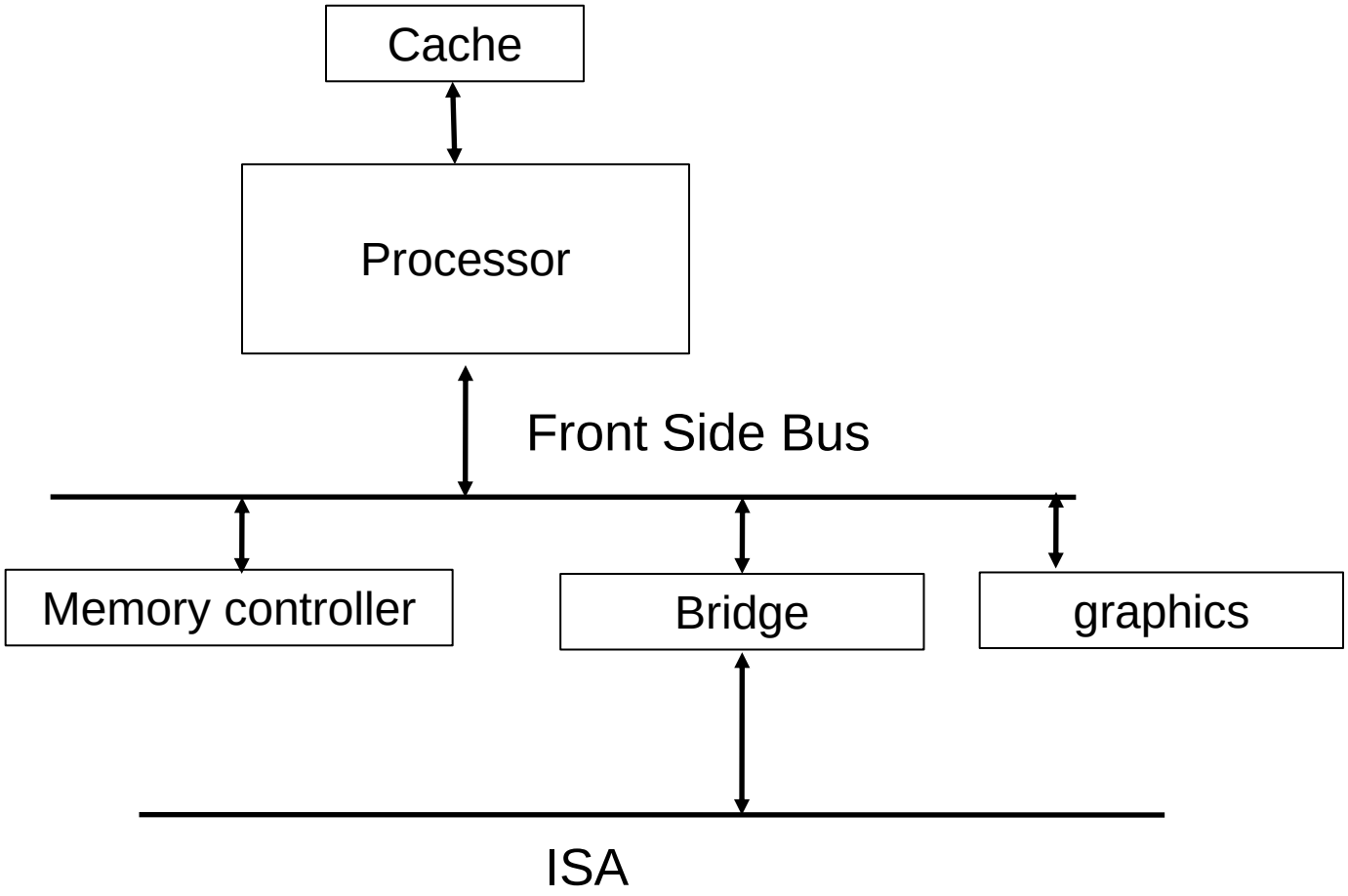
- Hub-based chipsets
- Intel Vs AMD
- Dual & Multiple cores

Early PC

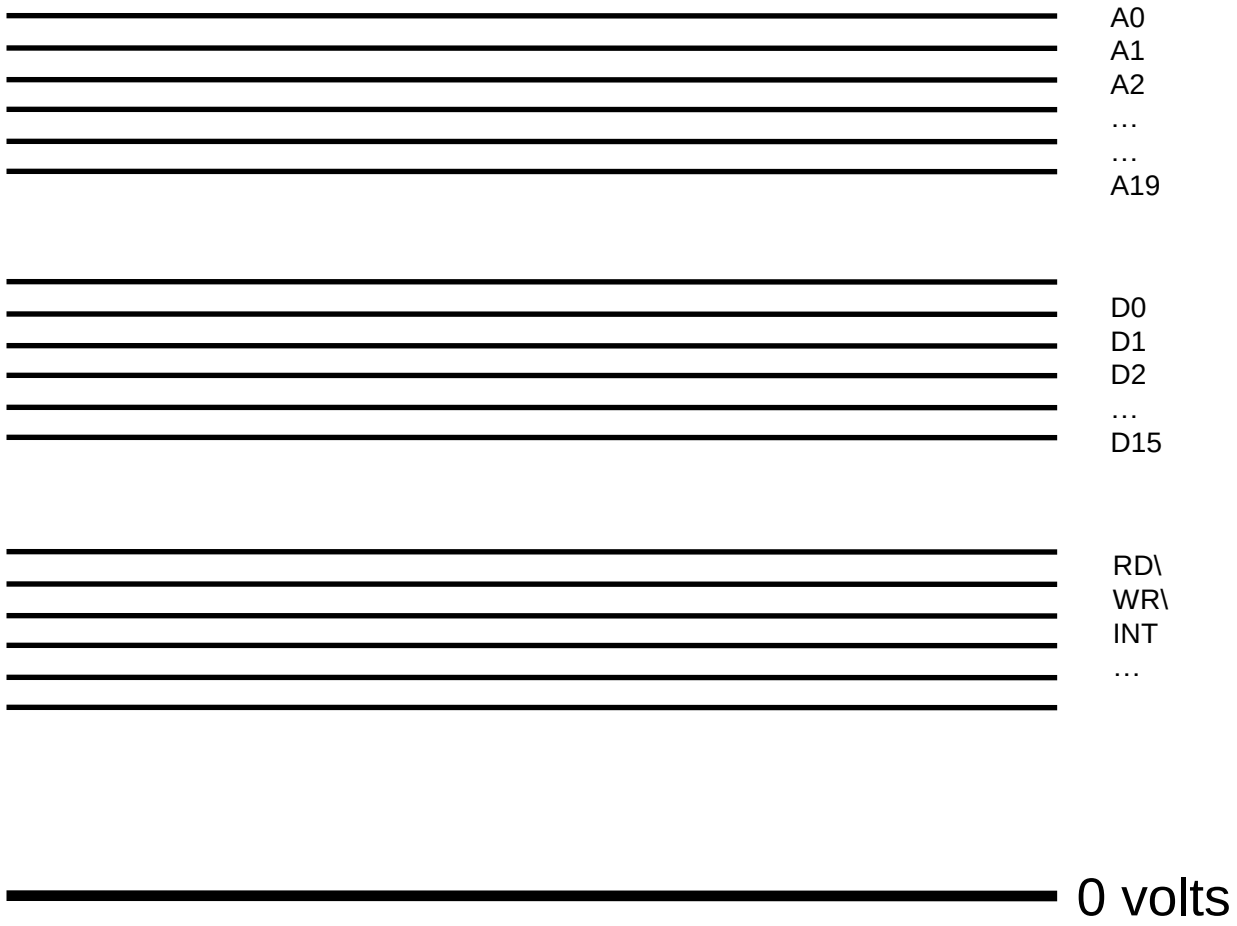

Data Bus
Clock
Processor
Memory
(ROM/RAM)
I/O Devices
Control bus
Address Bus

Standard buses




Cache
Processor
Front Side Bus
Memory controller
Bridge
graphics
ISA

Parallel bus, e.g. ISA, early PCI



Hub-based architectures

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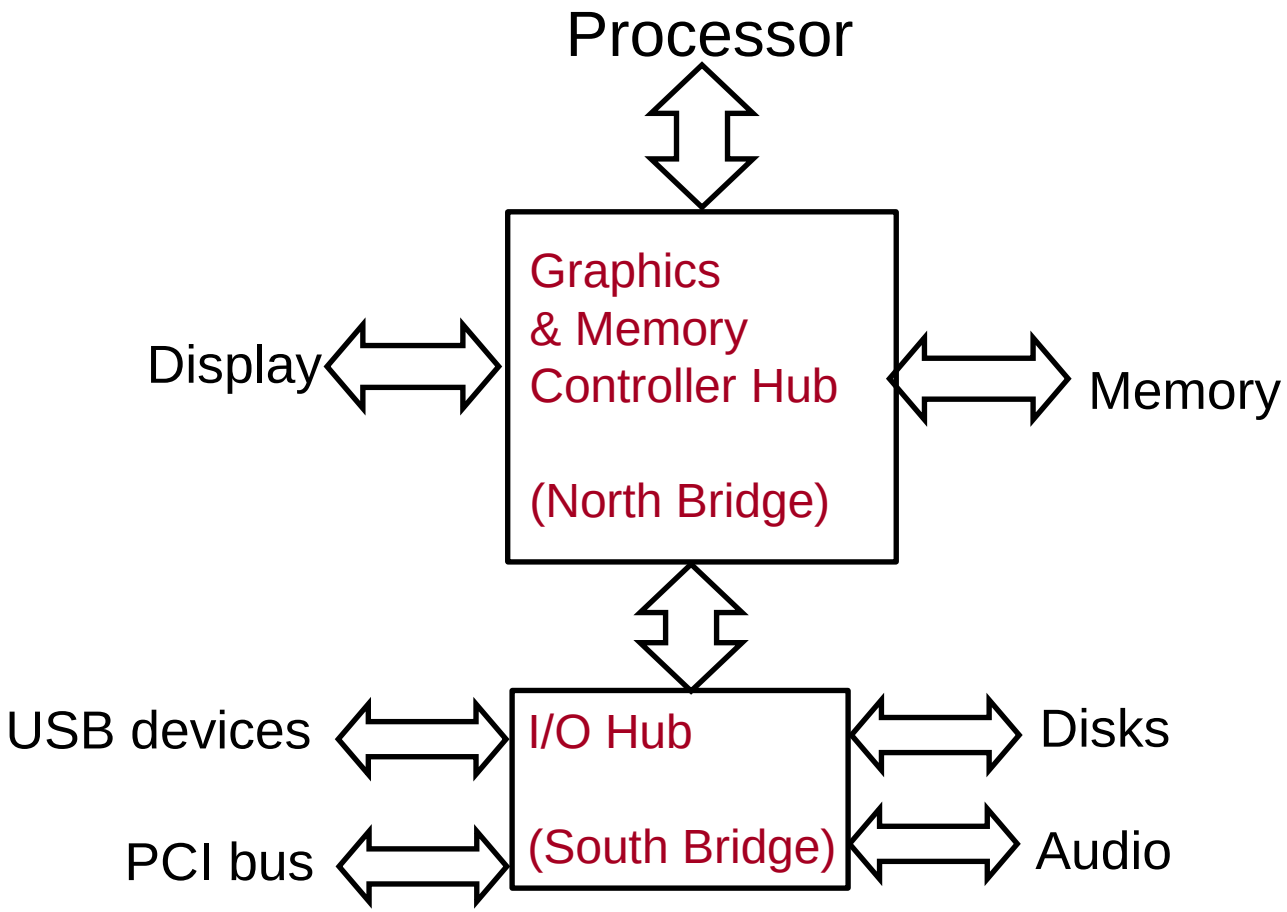
- The key part of the PC is now the chip-set that provides the connections to the buses.
- Initially, these were relatively simple bridges between layers (e.g. PCI to ISA).
- Now they have taken on more functions, become more central to the design, and come in closely coupled sets. These changes have led to what is best described as hub-based systems, such as the Intel G45, X48 & E8500 sets.



Typical Chipset

One/Two/Three-Chip Sets

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- Chip sets vary, but usually have a Memory Controller Hub (MCH) nearest to the processor. It will connect to the main DRAM and perhaps the graphics system (old name: North Bridge).
- Next down is the I/O Controller Hub (ICH). This will provide the disk drive, network and USB/Firewire connections as well as the PCI (old name: South Bridge).
- There may also be a Firmware hub. This may provide some slow connections, but is largely there to hold the Basic I/O System software (BIOS).
- Increasingly, the move is to have one hub, a ‘platform/system controller hub’. This can be done either by incorporating the GMC Hub into the CPU, or by combining the two hubs into one.

Typical chipset (Intel X48)

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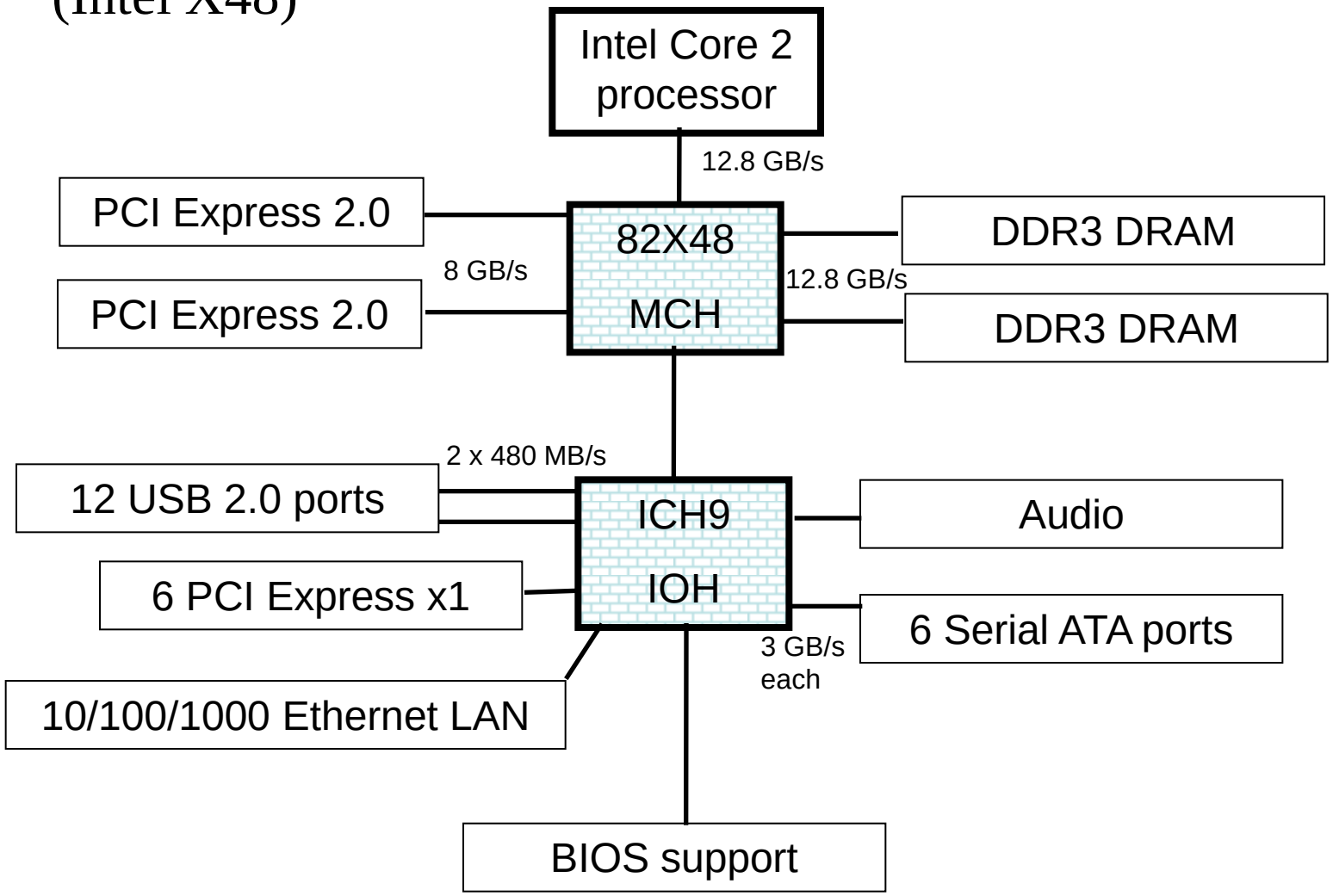

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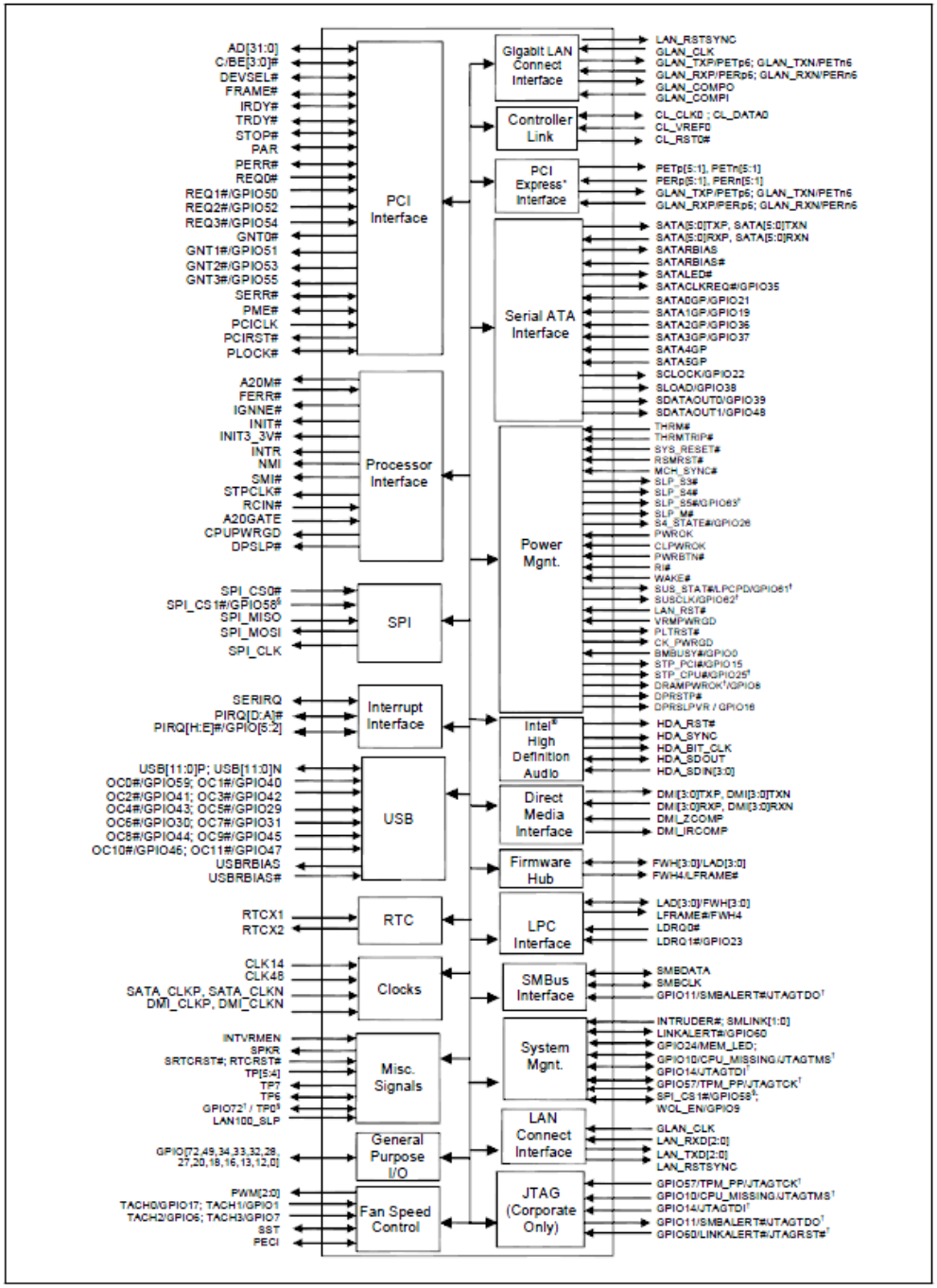
Questions

- Increasingly, the USB 2.0 bus (or Firewire) is taking over from PCI. What are the advantages?
  - *You don't have to open the box!*
  - *There are a limited number of PCI slots, you can plug in a lot of USB devices (hundreds).*

- Why 'Dual-channel' RAM?

The two channels operate in parallel. The throughput can be increased (though the RAM modules usually have to be the same).



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ICH10 I/O Controller Hub

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AMD Motherboards

- AMD pioneered a different approach : the memory controller is built into the CPU, so the North bridge is simpler.
- This has advantages in multiple processor systems: the single North bridge does not become a bottle-neck. However, with multiple core processors, the cores still share a memory controller.

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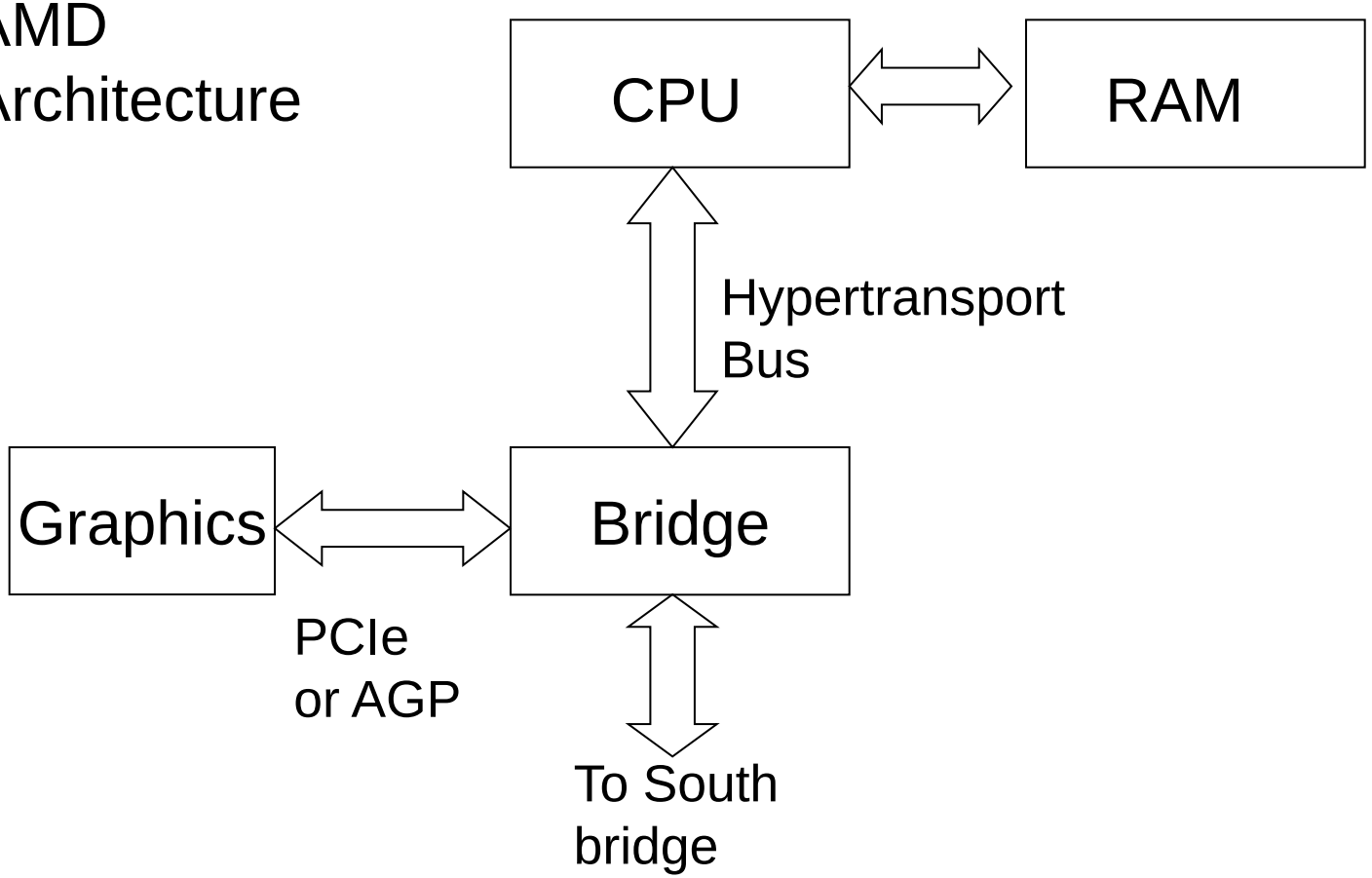
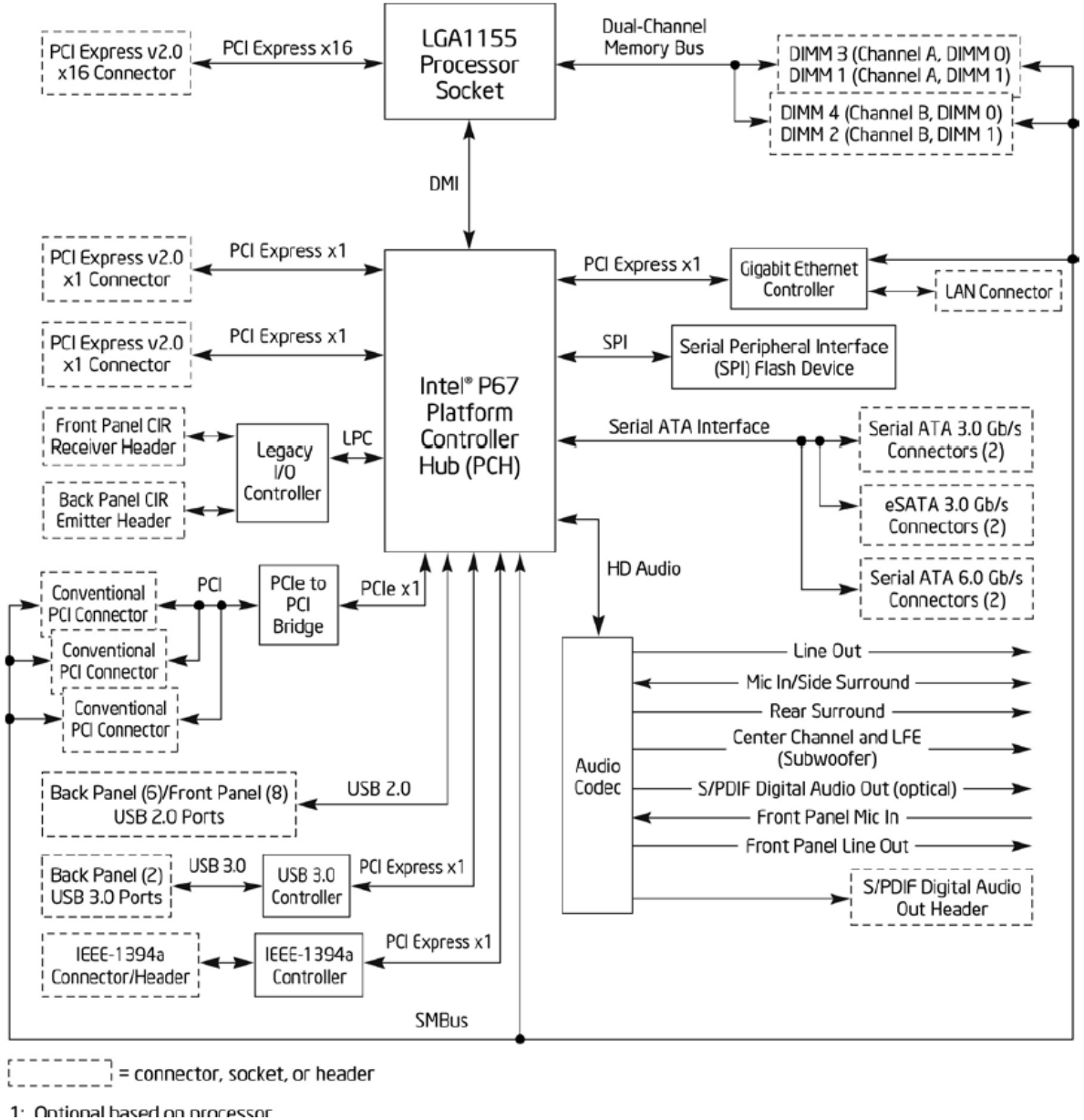
AMD Architecture



- By incorporating the whole of the GMC Hub into the processor, some recent Intel processors achieve a similar architecture to the AMD style: the memory is connected directly to the processor.
- In the old system, where the processor communicated to the GMC Hub (Northbridge), a wide variety of Front Side Buses (FSB) were used.
- The processor can use the DMI bus, developed for communication between the two hub chips.



DP67BA motherboard (page 19)

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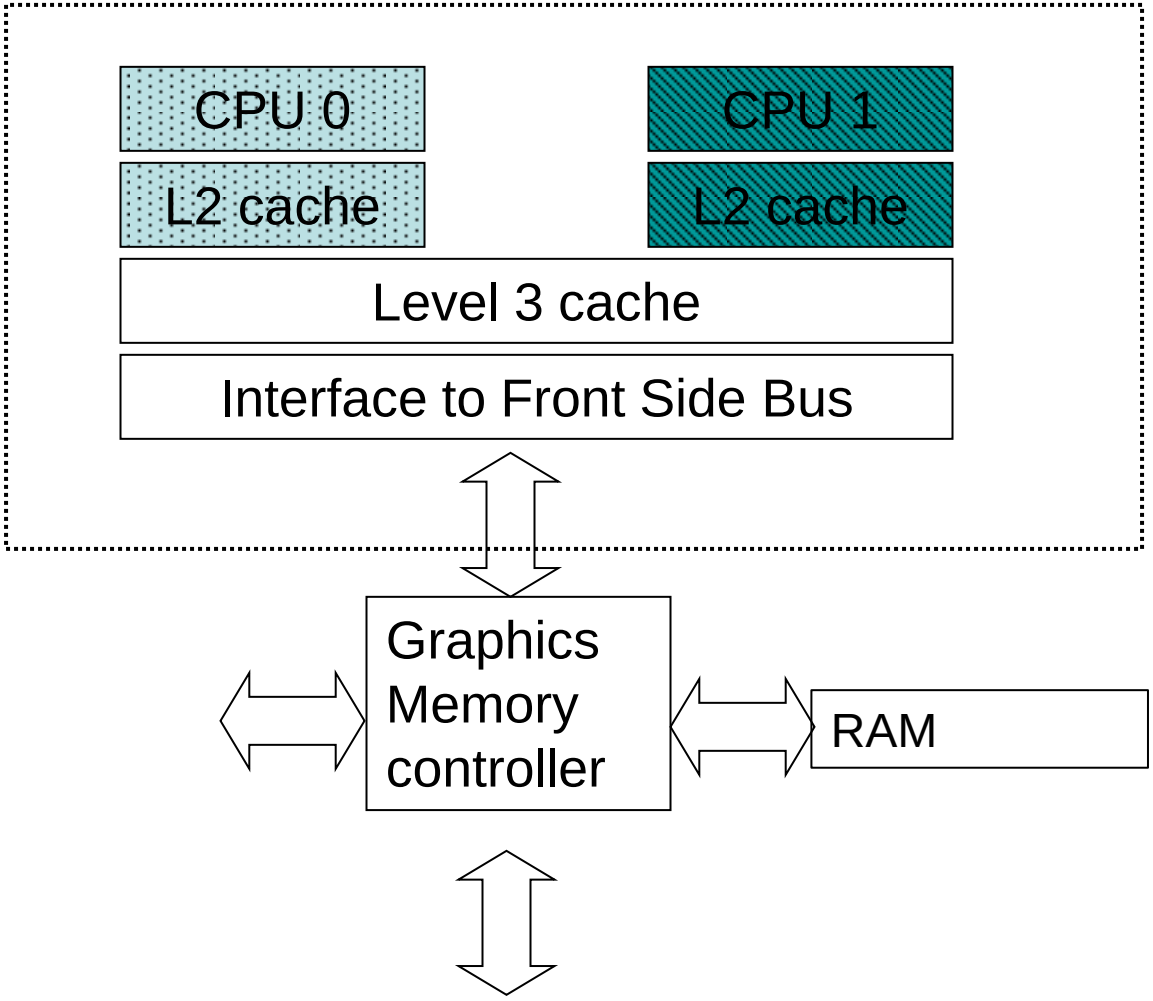
Multiple cores



A single processor chip can now contain 2, 4 or 6 cores. Note that the connection off the chip can become the bottleneck. However, most of the time, the cores will communicate with cache, not the external RAM.

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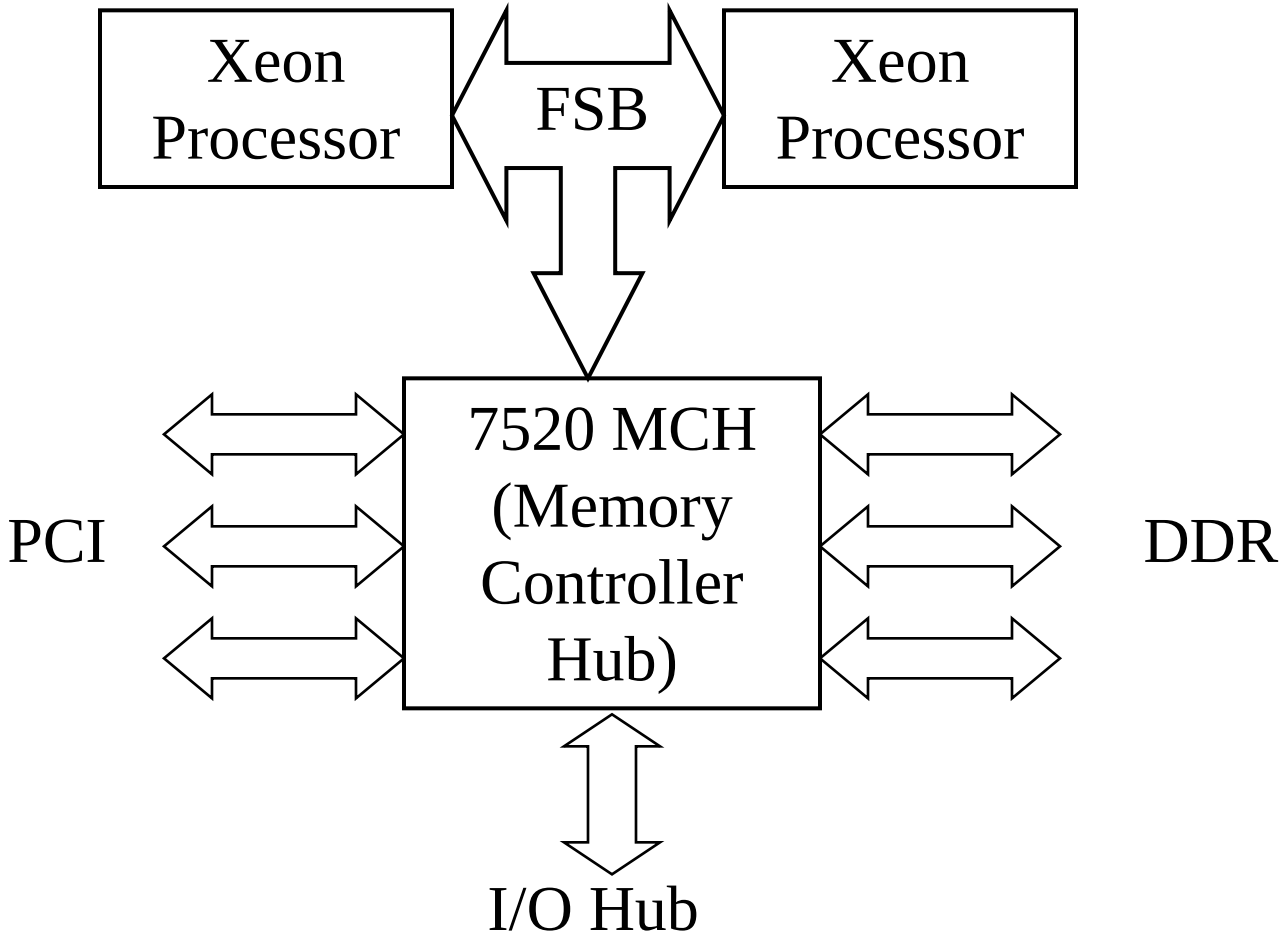
Multiple Processor systems: Intel

- For better performance, it may be effective to use larger numbers of processors.
- In this case, the hub chips act like switches. They will connect one of a number of processors to one of a number of banks of RAM or I/O buses.
- The Pentium family can be connected together like this, but the number that can be connected depend on the model, and the Operating System used.
- The Itanium and Xeon families are designed to work well in multiple processor systems.

7520 MCH & dual Xeon processors



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Can you spot a problem with this sort of shared bus?

- The processors may be slowed down by having to share the one bus.
- A few years ago, Intel introduced the ‘Dual Independent Bus’ to reduce this problem.

E8500 4-way Server chipset

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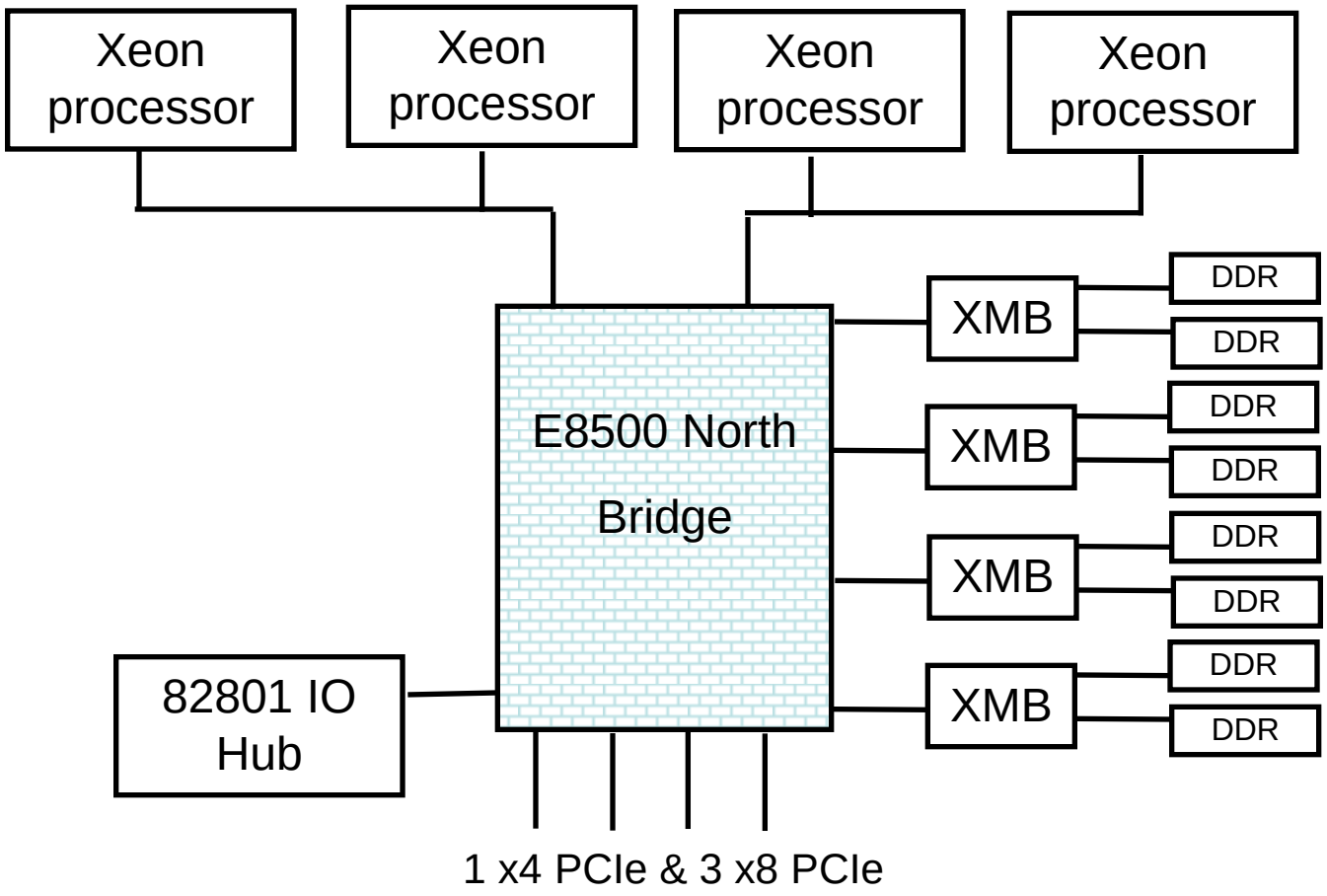

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Intel QuickPath Interconnect (QPI)

- Intel have introduced a new system to replace the Front Side Bus: Quick Path Interconnect.
- There are three significant features to this:
  - Each chip has its own memory controller, so the connection to the memory will be less of a bottle neck.
  - The bus is a multiple-lane serial bus (a bit like PCIe). Almost anything going off chip at the highest data rates is shifting from parallel to serial.
  - As well as connecting the core to the IO hub, it can be used to connect cores together.

2.1 Intel® QuickPath Interconnect (Intel® QPI) Differential Signaling

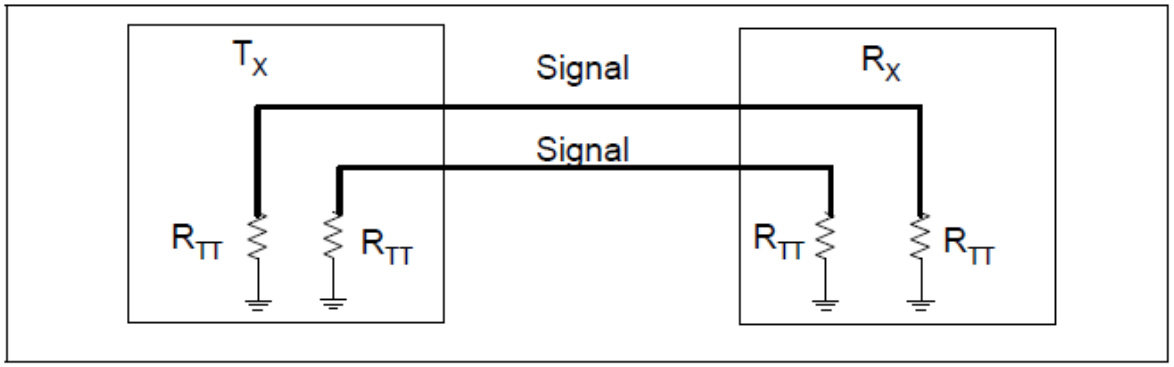
The processor provides an Intel QPI port for high speed serial transfer between other Intel QPI-enabled components. The Intel QPI port consists of two unidirectional links (for transmit and receive). Intel QPI uses a differential signalling scheme where pairs of opposite-polarity (D_P, D_N) signals are used.

On-die termination (ODT) provided on the processor silicon and termination is to V_{SS}. Intel chipsets also provide ODT; thus, eliminating the need to terminate the Intel QPI links on the system board.

Intel strongly recommends performing analog simulations of the Intel QPI interface.

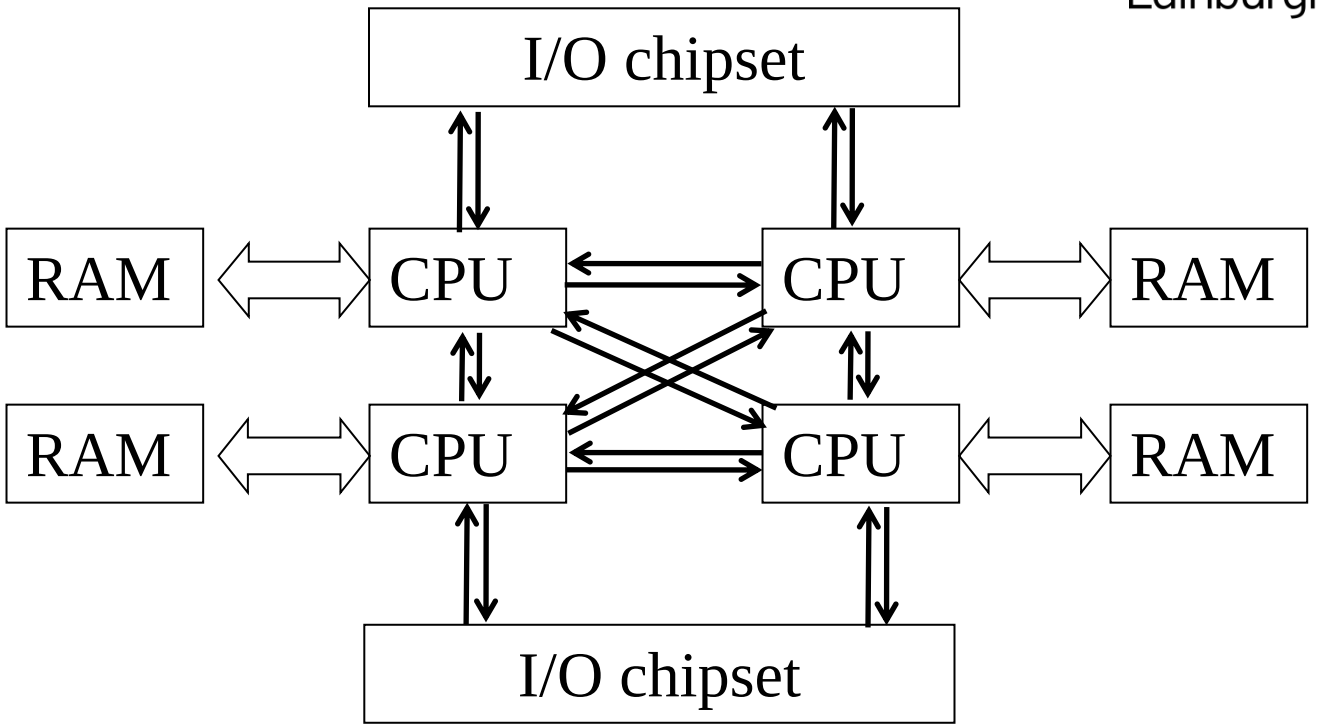
Figure 2-1 illustrates the active ODT. Signal listings are included in Table 2-3 and Table 2-4. See Chapter 5 for the pin signal definitions. All Intel QPI signals are in the differential signal group.

Figure 2-1. Active ODT for a Differential Link Example



2.2 Power and Ground Lands

For clean on-chip processor core power distribution, the processor has 210 VCC pads and 119 VSS pads associated with V_{CC}; 8 VTTA pads and 5 VSS pads associated with V_{TTA}; 28 VTTD pads and 17 VSS pads associated with V_{TTD}, 28 VDDQ pads and 17 VSS pads associated with V_{DDQ}; and 3 VCCPLL pads. All VCCP, VTTA, VTTD, VDDQ, and VCCPLL lands must be connected to their respective processor power planes, while all VSS lands must be connected to the system ground plane. The processor VCC lands must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) signals. Table 2-1 specifies the voltage level for the various VIDs.



Intel QuickPath Interconnect (QPI)

Standard parallel memory bus

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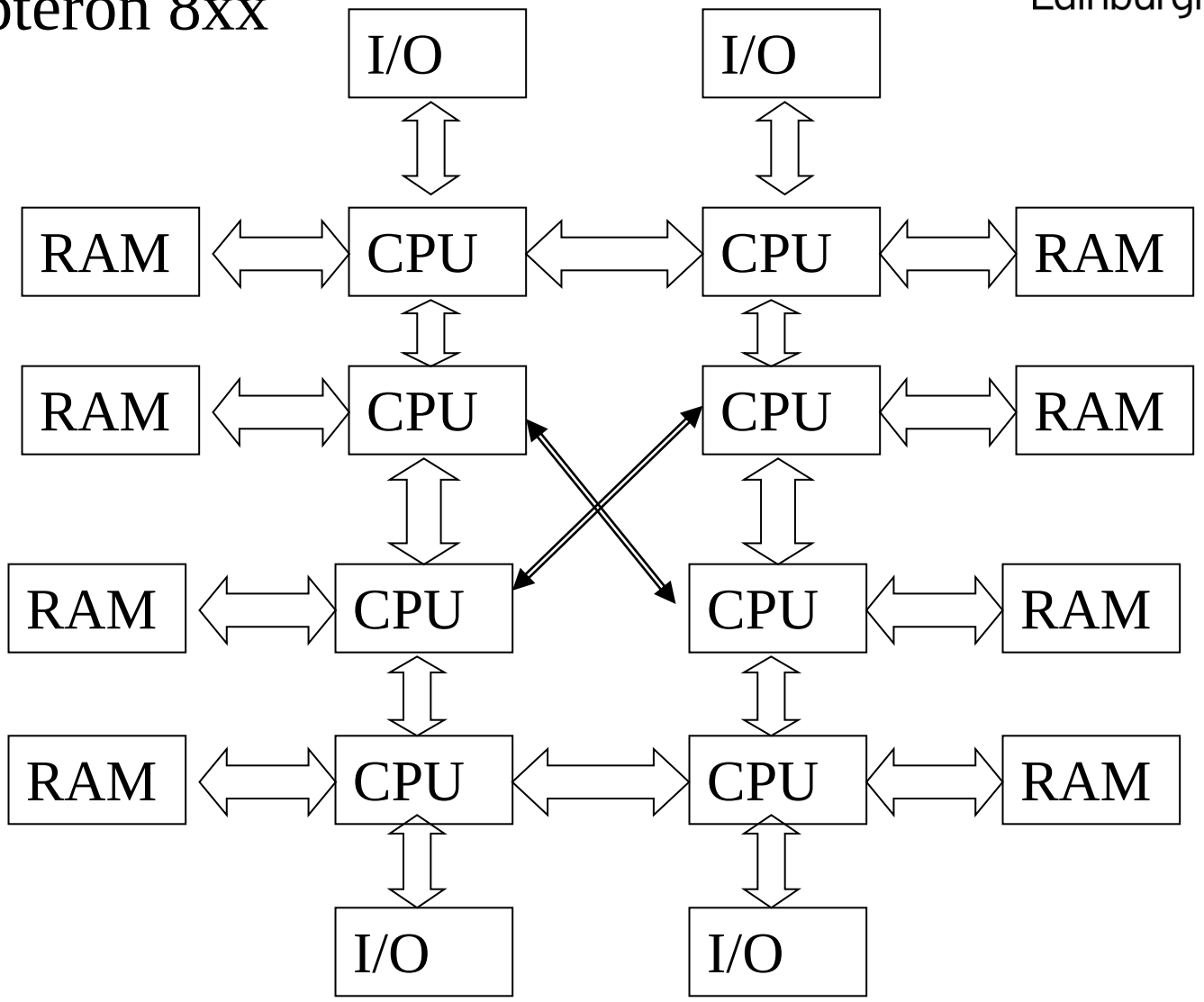
Multiple processor systems: AMD

- Opteron 2xx series processors can be connected together in dual configurations.
- 8xx series processors can be connected in twos, fours or eights.
- In the following diagram: ‘I/O’ is a bridge chip, typically connecting to PCI or PCIe.

Opteron 8xx


I/O
I/O
RAM
CPU
CPU
RAM
RAM
CPU
CPU
RAM
RAM
CPU
CPU
RAM
RAM
CPU
CPU
RAM
I/O
I/O

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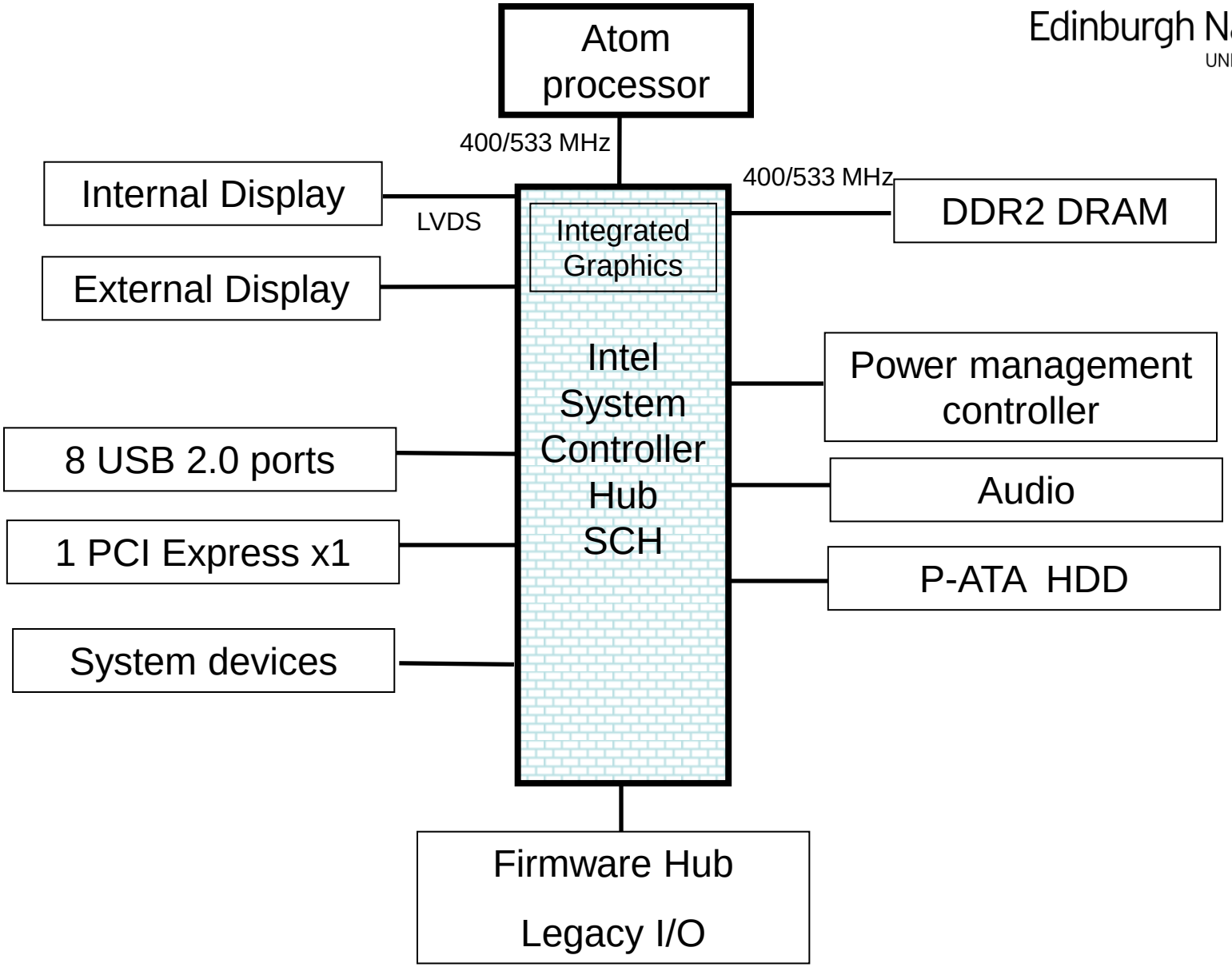
Simpler Atom based systems

- The need for low-power systems for use in Netbooks with long battery life has meant a return to relatively simple single-core processors: Atoms.
- These run the same software as Pentiums, but only have a single core though they do Hyperthreading.
- The simpler systems use a System Controller Chip that combines the two chips of the bigger chipsets.


Atom processor
400/533 MHz
Internal Display
LVDS
External Display
Integrated Graphics
400/533 MHz
DDR2 DRAM
Intel System Controller Hub SCH
Power management controller
Audio
P-ATA HDD
8 USB 2.0 ports
1 PCI Express x1
System devices
Firmware Hub
Legacy I/O

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Intel Atoms

Code-name	Series	Core	Graphics	Power*	HyperThread	Release date
Netbook						
Diamondville	N2xx	single	No	2.5 W	Yes	June 2008
	2xx	single	No	4 W	Yes	June 2008
	3xx	dual	No	8 W	Yes	September 2008
Pineview	N4xx	single	Yes	5.5 W	Yes	January 2010
	D4xx	single	Yes	10 W	Yes	January 2010
	D5xx	dual	Yes	13 W	Yes	January 2010
Mobile Internet Device						
Silverthorne	Z5xx	single	No	~2 W	Some	April 2008
Lincroft	Z6xx	single	Yes	2-3 W	Yes	May 2010

Sources: http://www.intel.com/products/processor/atom/index.htm http://en.wikipedia.org/wiki/Intel_Atom

*A core 7 quad-core processor has a peak power rating of about 130watts

Mobile systems

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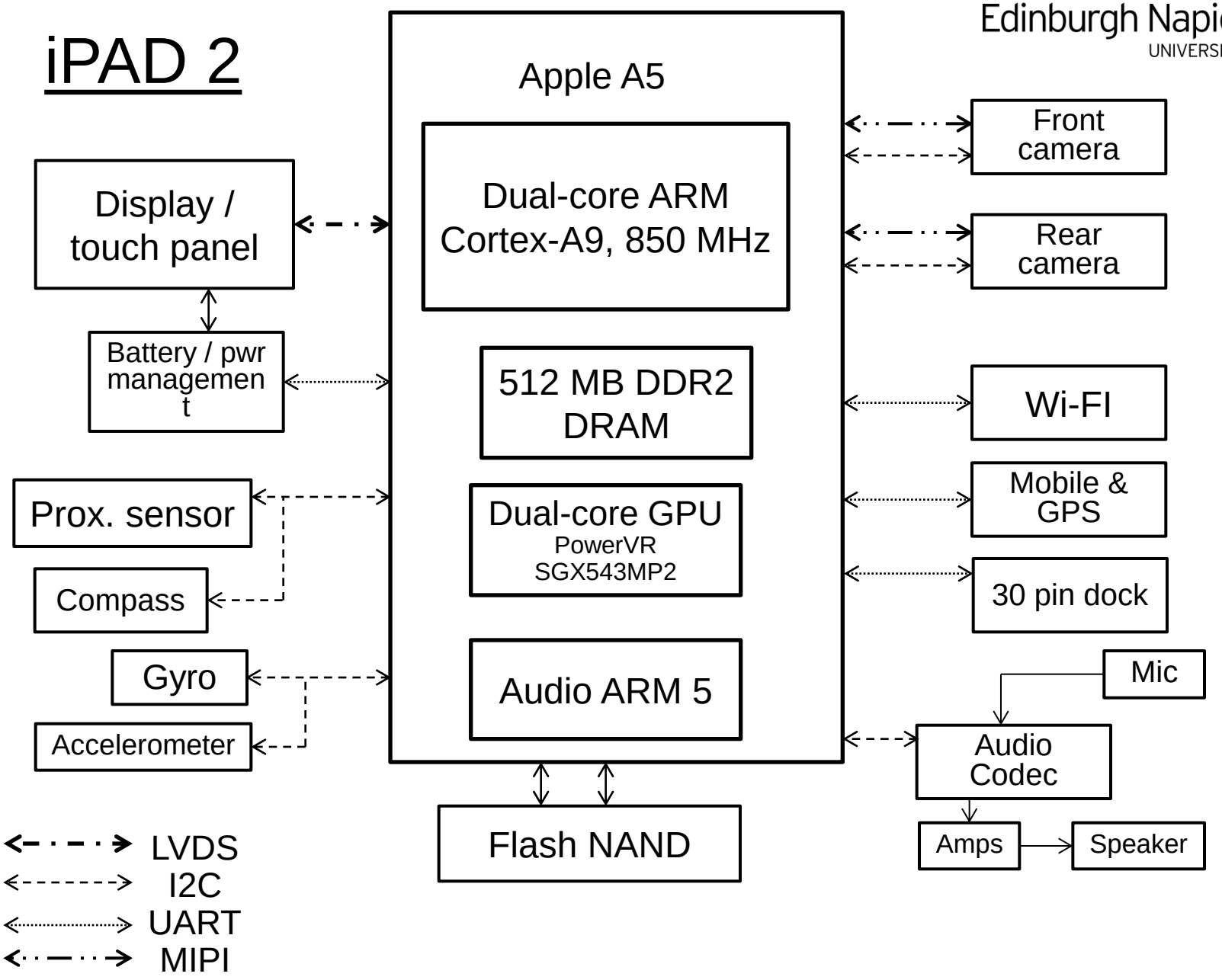
- In mobile processing (tablets, phones etc.) it is still important to have reasonable processing and graphics performance, but battery consumption becomes an important factor.
- ARM's processors are dominant in this area: better low-power performance than Intel's chips.
- ARM processors are actually designs for cores that manufacturers put into a system chip.
- There are numerous variants that have different levels of performance, features and power consumption.
- They all run the same standardised instruction set (i.e. the same software runs across the range).

iPAD 2


Apple A5
Dual-core ARM Cortex-A9, 850 MHz
512 MB DDR2 DRAM
Dual-core GPU
PowerVR SGX543MP2
Audio ARM 5
Flash NAND
Display / touch panel
Battery / pwr managemen t
Prox. sensor
Compass
Gyro
Accelerometer
Front camera
Rear camera
Wi-FI
Mobile & GPS
30 pin dock
Mic
Audio Codec
Amps
Speaker
LVDS
I2C
UART
MIPI

ARM A9

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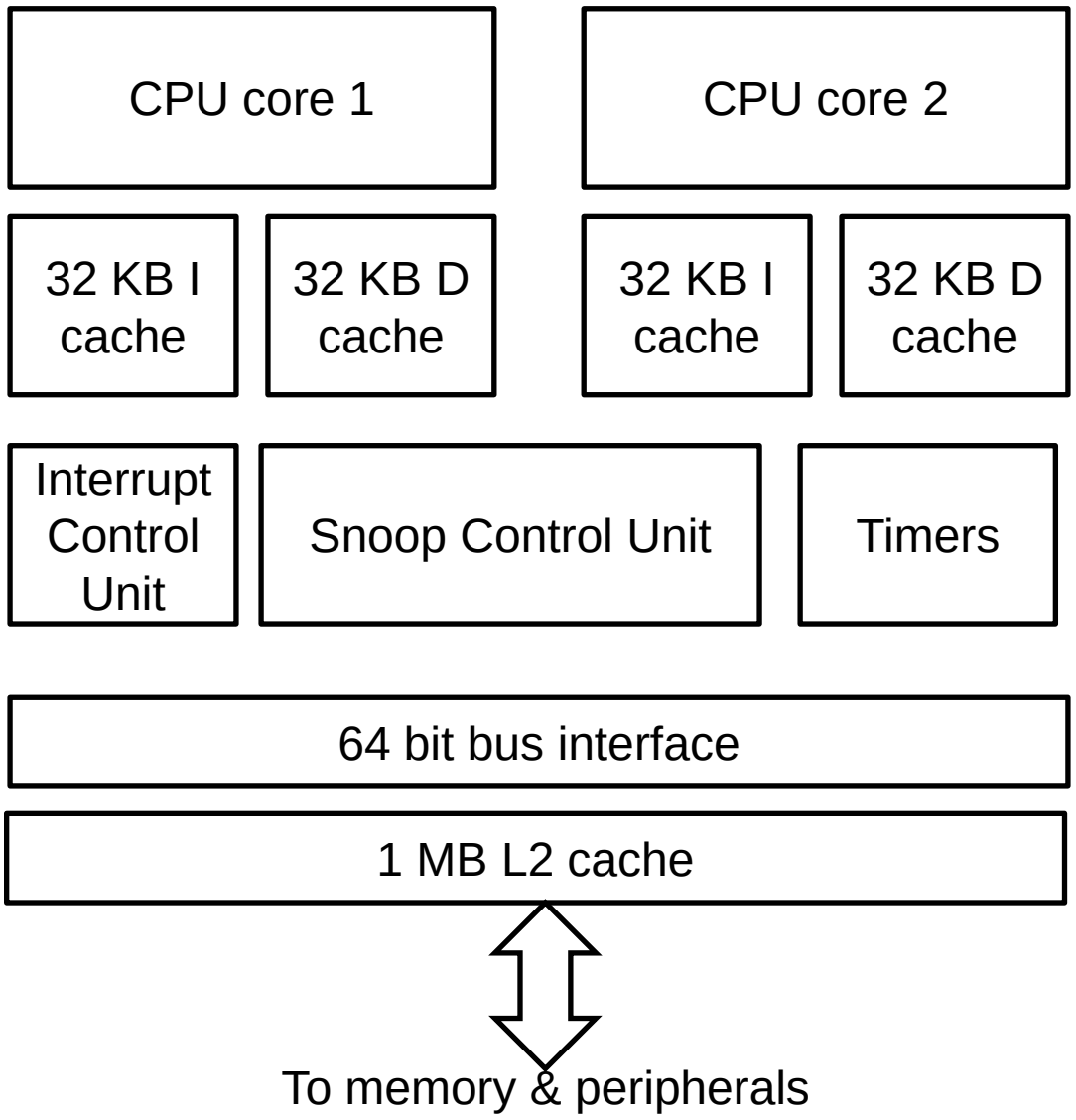

‘ big LITTLE’ processing

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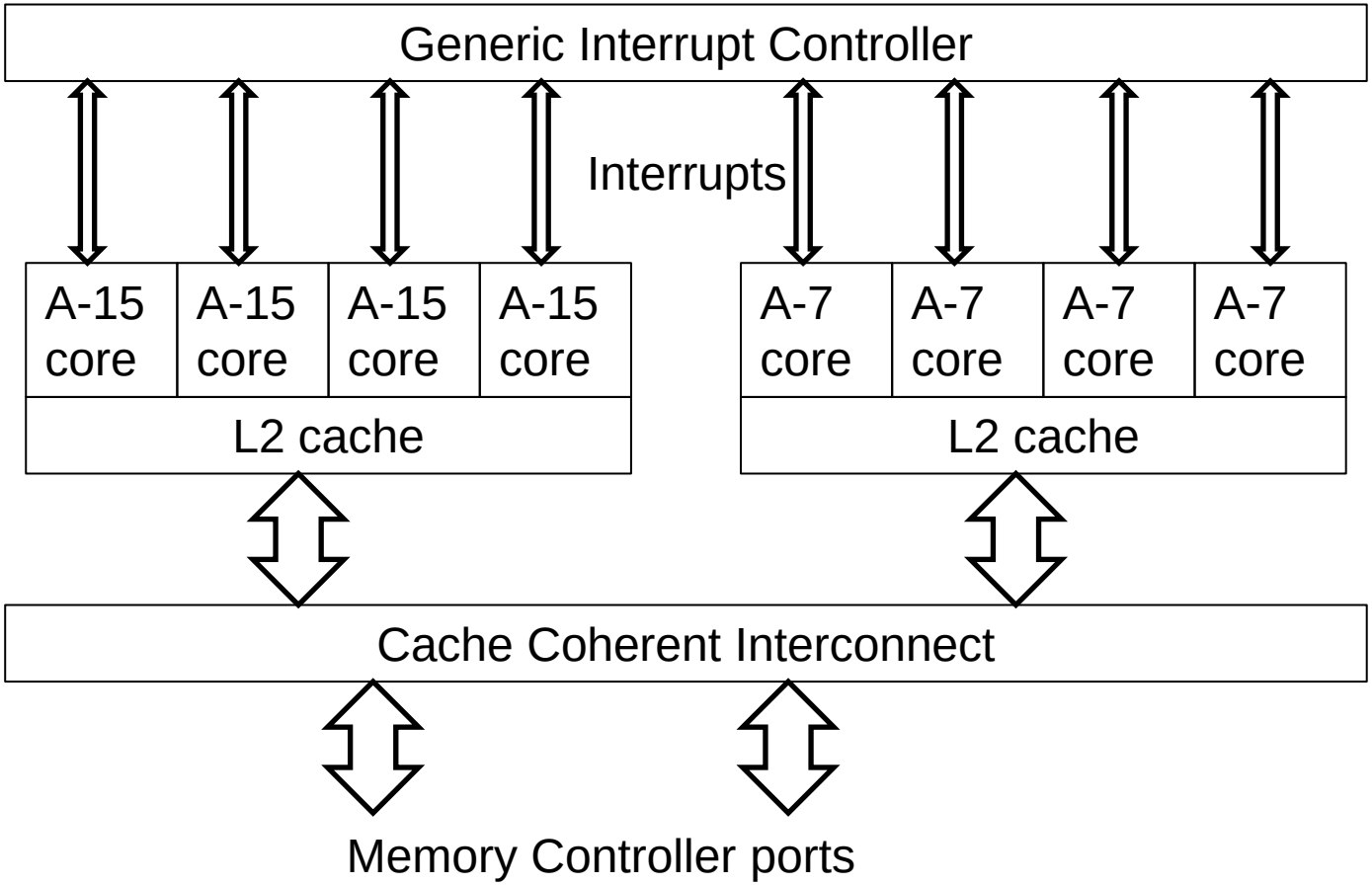
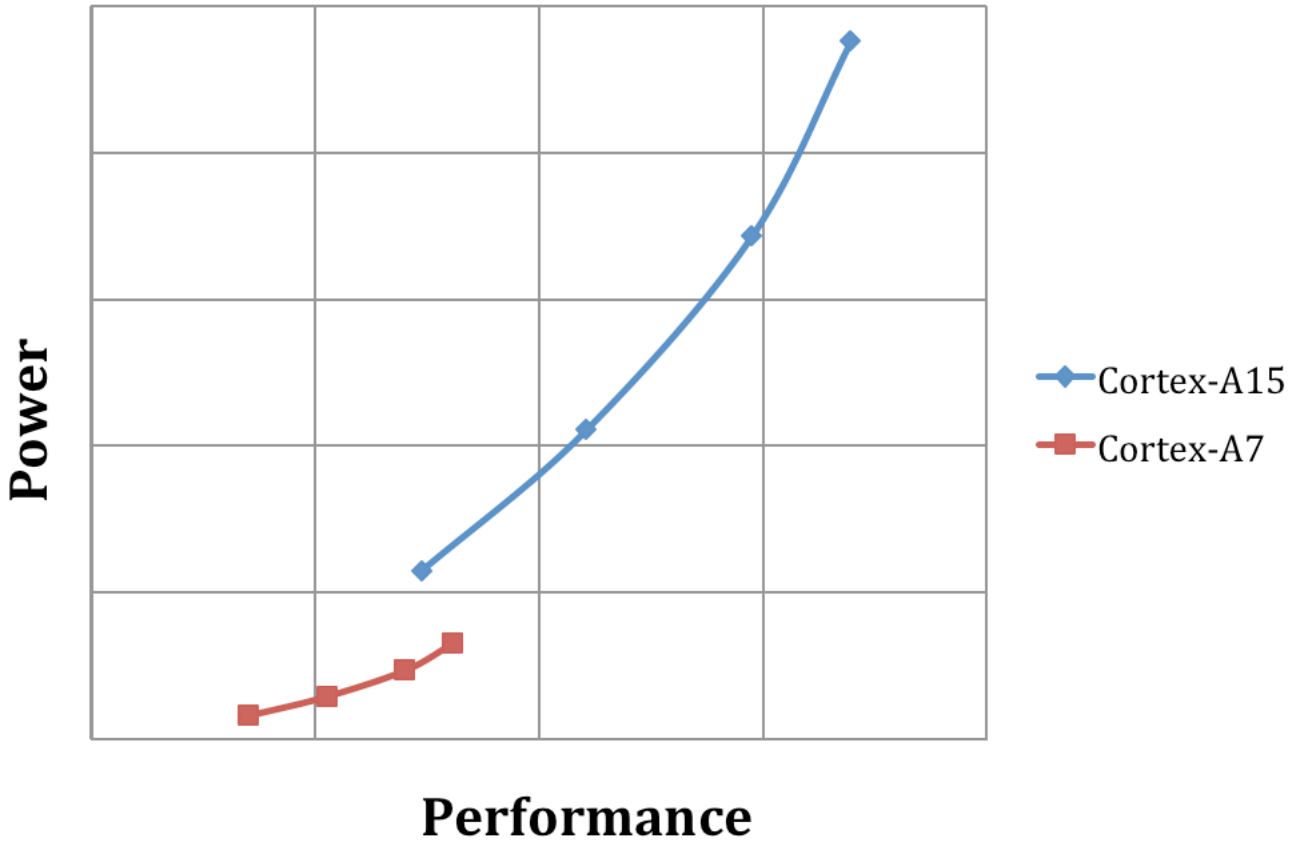
- On a desktop PC, power consumption is not a big problem; many chips are optimised to give the highest computing performance.
- In small embedded systems, power consumption may be the deciding factor, and chips are optimised for low power.
- Many mobile applications sometimes need high performance (e.g. media decoding) but often need to conserve power. It is really hard to design a processor that is optimum for both performance and power.
- If a number of processors can be designed onto the same chip, it becomes practical to have processors optimised for high performance (that may not be needed all the time) and other processors that can run using much less power when demand is low.
- ARM are a pioneer in this area of ‘big little’ processing; they call it big.LITTLE processing: pairing ‘big’ A 15 with ‘little’ A 7 processors.

Samsung Galaxy S4: Exynos Octa-core 5410 chip



Relative performance



"**big.LITTLE Processing with ARM Cortex-A15 & Cortex-A7"** *www.**arm**.com/files/downloads/**big**.**LITTLE**_Final.pdf*

Why does big.LITTLE work?

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- Although the ARM 7 & ARM 15 cores have quite different performance, they still run exactly the same instructions.
- The ARM 7 uses a relatively simple instruction decode pipeline and instructions have to be completed in strict sequence. The ARM 15 can start on more instructions every clock cycle, has a complicated decode sequence, and instructions can complete out of order.
- The Caches in the processors are designed differently too. However, these features only affect the speed at which instructions run; all the processors still run the same instructions.
- This means that tasks can be switched between high- and low-performance processors as needed: a very flexible strategy.

Questions

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- Are there disadvantages to this sort of processing?
  - There must be some overhead in transferring software from one processor to another (ARM quote 20,000 cycles).
- Is this significant?
- 20,000 cycles at, say, 1 GHz is?
  - 20 microseconds
- which of these is this equivalent to?
  - RAM latency
  - Interrupt response
  - Hard disk latency