

# JOSE “SHINKIRO” SALINAS MEZA

Electrical & Computer Engineering | Hardware–Software Systems | AI

Arizona, USA | JOSESALINASMEZA@OUTLOOK.COM

LinkedIn: [linkedin.com/in/JSM-Shinkiro](https://www.linkedin.com/in/JSM-Shinkiro) | GitHub: [github.com/JSM-Shinkiro](https://github.com/JSM-Shinkiro) | Webpage: [jsm-shinkiro.github.io](https://jsm-shinkiro.github.io)

---

## SUMMARY

Electrical & Computer Engineering student with hands-on experience in computer architecture, digital and analog hardware, and applied machine learning. Experienced in building end-to-end systems from pipelined CPUs and PCB-level analog circuits to data-driven ML models and network-scale analysis. Seeking Summer 2026 engineering internships in hardware, software, systems, or AI-adjacent roles; open to relocation across the U.S and remote opportunities.

---

## EDUCATION

University of Arizona — B.S. Electrical & Computer Engineering

Minor Focus: Computer Science & Artificial Intelligence

Expected Graduation: 2026

---

## TECHNICAL SKILLS

Programming & HDL: Python, C/C++, Java, Verilog, MATLAB, MIPS Assembly, HTML/CSS

Hardware & ECE: FPGA (Vivado), Digital Design, SPICE, PCB Design (Eagle/KiCad)

AI & Data: PyTorch, scikit-learn, NumPy, pandas, Matplotlib

Tools: Git, GitHub, Linux, VS Code

Languages: English (fluent), Spanish (native)

---

## PROJECT EXPERIENCE

### 5-Stage Pipelined MIPS CPU — Verilog, Vivado

- Designed a fully pipelined MIPS-like CPU with IF/ID/EX/MEM/WB stages
- Implemented hazard detection and forwarding logic
- Verified correctness via simulation and waveform inspection

### Audio Power Amplifier PCB — Analog Circuits

- Designed multi-stage amplifier with op-amp preamp and push-pull output stage
- Simulated gain, stability, and distortion using SPICE
- Designed custom PCB layout

### Neural Networks vs Naive Bayes — PyTorch

- Implemented and compared neural networks against Naive Bayes baseline
- Tracked learning curves and overfitting behavior

### Internet AS Topology Analysis — Python

- Built provider-to-customer graphs and computed customer cones
- Analyzed routing hierarchy and scalability

---

## ENGINEERING EXPERIENCE

- Computer Architecture Team Project — pipelined CPU design and hazard logic
- Networking Simulations — CSMA/CA, RTS/CTS, throughput analysis
- Embedded Systems — dual-axis solar tracking system

---

## INTERESTS

Computer architecture, software, circuits, hardware acceleration, applied machine learning, semiconductor systems, and large-scale technical systems.