



GRAND CANYON  
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Project Proposal for Wakup9000

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CST-451 Capstone Project Proposal

Grand Canyon University

Instructor: Professor Mark Reha

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## **ABSTRACT**

The Wakup9000 will be a digital clock that will keep track of appointments for the user, light up when it is time for set meetings, display the time on the digital clock, and display a message relating to what status the clock is in at that time. This device will be perfect for users who desire to keep a physical clock in their home offices to remind them when their appointments are. When the clock sets off an alarm, it will light up the LED lights on the board and display a message on the LCD Display screen for the user while flashing the time on the board while it still continues to move the clock's time forward.

With FPGA technology at the team's disposal, this is a perfect task for them to tackle. The hardware contains all of the features that this alarm clock requires and it is configurable in the field if the client were to want additional features in the future or for current features to be manipulated. This leads to a potential stream of revenue for the company in the future as we continue to make updates to the product and send our employees out for field operations to update purchased products for the clients. An example of a future addition to this product would be to create an outside application that can connect to the alarm clock to automatically update the product and sync up with the user's calendar. For the Wakup9000's current proposed features, the clock will conduct all of the required features of displaying a message to the user, displaying the time, allowing the user to utilize the various inputs to configure the clock settings and turn off the alarm, and flash LED lights when the alarm goes off.

History and Signoff Sheet

Change Record

| Date      | Author       | Revision Notes                      |
|-----------|--------------|-------------------------------------|
| 18-Sep-22 | Joseph Sande | Initial draft for review/discussion |
|           |              |                                     |
|           |              |                                     |

Overall Instructor Feedback/Comments

Overall Instructor Feedback/Comments

Integrated Instructor Feedback into Project Documentation

☐ Yes ☐ No

Project Approval

☐ Professor Mark Reha

## TABLE OF CONTENTS

|   |    |
|---|----|
| PROJECT OVERVIEW AND PROJECT OBJECTIVES ..... | 5  |
| PROJECT SCOPE.....                            | 7  |
| PROJECT SUCCESS MEASURES .....                | 9  |
| PROJECT HIGH-LEVEL SOLUTION .....             | 10 |
| PROJECT CONTROLS .....                        | 11 |
| PROJECT COST AND SCHEDULE .....               | 14 |
| APPENDIX A – REFERENCES .....                 | 15 |
| APPENDIX B – COPYRIGHT COMPLIANCE .....       | 16 |

## **Project Overview and Project Objectives**

### **State the Problem and Background**

The team is proposing a solution to develop a clock that can wake up even the heaviest of sleepers from their afternoon naps by utilizing a light source along with traditional features of a digital alarm clock through an FPGA board. This clock will have the capabilities of displaying the time, a message, flashing lights, buttons to program the clock, and switches for configurations of the clock. These features will solve the problem set ahead of how to wake up an individual who is an incredibly heavy sleeper that does not wake up to a traditional alarm clock. Through this project, the company will also gain the knowledge to work with FPGA boards so that it can join the market in current aviation technologies that rely upon these boards. With this skillset under the team's belt, this will propel the company forward in its marketing strategies and reach a whole new set of clientele.

### **Christian Worldview**

This project will help many people around the world that all struggle to wake up on time or to remember meetings when they occur. This can be heavily marketed in today's industry where there are more people working from home and who rely upon their phones for meeting alarms. If these people are like the average person, they will leave their phone somewhere else in their house while eating lunch and will miss their meetings because they did not have their phone to remind them. The Wakup9000 will ensure that everyone meets their timelines for whatever they are planning and to keep their general operations on track by always being stationary at their desks in order to be an effective and reliable alarm for the user. There are many people out there that struggle with time management and this will be a thing of the past when they utilize the Wakup9000 to keep their life schedule in check.

### **Project Objectives**

#### **In Scope Objectives:**

1. Program an FPGA board's buttons to configure the board.
2. Implement a digital logic circuit in an FPGA.
3. Program an FPGA board's switches to configure the board.
4. Program an FPGA board's 7-segment display to display the clock's timer.

5. Program an FPGA board's LCD screen to display messages to the user.
6. Program an FPGA board's LED lights to light up during an alarm.

### **Out of Scope Objectives:**

1. Verify if GO Lang can be substituted for C in creating software compatible with ARM processors.

### **Challenges**

There are many challenges that will be tackled with this project regarding the team's lack of prior expertise in the field and the project's general specifications. These challenges are listed below:

1. Set up a development environment for FPGA programming.
2. Ramp up technical knowledge of FPGA component programming.
3. Ramp up technical knowledge of general embedded systems development.
4. Ramp up technical knowledge of what components are and what they are utilized for on the FPGA board.
5. Ramp up technical knowledge of complex C programming.
6. Ramp up technical knowledge of ARM development.
7. Ramp up technical knowledge of BCD decoding.
8. Ramp up technical knowledge of Go Language.

### **Benefits and Opportunities**

The benefits of this project will be that it will provide the ability for the user to obtain an alarm clock that notifies them in various methods to ensure they know when their meeting is if they lose track of time. It's easy to lose track of time while working on tasks or hobbies during the day, but a clock that will light up, display a message, and play a sound as an alarm will help to deter the inability to be on time for events. This project will allow the team to learn many new skills with programming FGPA boards, familiarity with FPGA board components, learning complex C programming, ARM development, general embedded system development, and learning about the Go programming language. These skills can be leveraged from the team to develop more complex applications and features that corresponds with creating drones, mobile devices, complex navigation technology, or any other device that clientele would desire regarding an FPGA board's capabilities. These skills are invaluable for any company within the

imbedded systems industry and having the team complete this project will develop the skills necessary to make the future dreams of a company's expansion become a reality.

## Project Features Scope

### Features that are in scope:

1. Display messages.
2. Display timer.
3. Flash lights.
4. Program switches.
5. Program buttons.

### Features that will be out of scope:

1. Use Go Lang

## Schedule for Work Breakdown

| Work Breakdown Structure and Schedule |  |              |          |              |       |            |                    |                        |                   |          |
|---------------------------------------|--|--------------|----------|--------------|-------|------------|--------------------|------------------------|-------------------|----------|
| ID                                    | Task   | Dependencies | Status   | Effort Hours | Cost  | Start Date | Planned Completion | Estimate to Completion | Actual Completion | Resource |
| 1                                     | Refamiliarize with the C language                        |              | Complete | 6 hours      |       | 9-8-22     | 9-15-22            | 6 hours                | 9-12-22           |          |
| 2                                     | Setup FPGA Board development environment                 |              | Complete | 3 hours      |       | 9-8-22     | 9-12-22            | 3 hours                | 9-12-22           |          |
| 3                                     | Setup Visual Studio Code to support C                    |              | Complete | 1 hour       |       | 9-8-22     | 9-12-22            | 1 minutes              | 9-12-22           |          |
| 4                                     | Order FPGA Board   |              | Complete | 30 minutes   | \$430 | 7-2-22     | 7-2-22             | 30 minutes             | 9-12-22           |          |
| 5                                     | Configure Micro SD Boot card for FPGA                    |              | Complete | 2 hours      |       | 9-8-22     | 9-12-22            | 2 hours                | 9-12-22           |          |
| 6                                     | Run Hello World on Board                                 |              | Complete | 1 hour       |       | 9-12-22    | 9-12-22            | 1 hour                 | 9-12-22           |          |
| 7                                     | Set up FileZilla for board                               |              | Complete | 1 hour       |       | 9-12-22    | 9-12-22            | 1 hour                 | 9-12-22           |          |
| 8                                     | Set up IP address for computer to communicate with board |              | Complete | 2 hours      |       | 9-12-22    | 9-12-22            | 2 hours                | 9-12-22           |          |
| 9                                     | Complete Activity 1                                      |              | Complete | 2 hours      |       | 9-8-22     | 9-12-22            | 4 hours                | 9-12-22           |          |
| 10                                    | Complete Activity 2                                      |              | Complete | 13 hours     |       | 9-13-22    | 9-18-22            | 6 hours                | 9-23-22           |          |
| 11                                    | Complete Activity 3                                      |              | Complete | 4 hours      |       | 9-22-22    | 9-27-22            | 6 hours                | 10-1-22           |          |
| 12                                    | Complete Activity 4                                      |              | Complete | 4 hours      |       | 9-27-22    | 10-4-22            | 4 hours                | 10-1-22           |          |
| 13                                    | Complete Activity 5                                      |              | Complete | 8 hours      |       | 10-5-22    | 10-18-22           | 4 hours                | 10-22-22          |          |
| 14                                    | Complete Activity 6                                      |              | Complete | 8 hours      |       | 10-19-22   | 10-28-22           | 4 hours                | 11-4-22           |          |

|    |  |  |              |          |  |          |         |          |          |  |
|----|--|--|--------------|----------|--|----------|---------|----------|----------|--|
| 15 | Complete Activity 7                                |  | Complete     | 8 hours  |  | 10-29-22 | 11-5-22 | 4 hours  | 11-14-22 |  |
| 16 | Complete Project Proposal Template                 |  | Complete     | 10 hours |  | 9-8-22   | 9-23-22 | 10 hours | 9-24-22  |  |
| 17 | Program lights on board                            |  | Complete     | 4 hours  |  | 11-10-22 | 2-1-22  | 5 hours  | 10-19-22 |  |
| 18 | Program Buttons on board                           |  | Complete     | 4 hours  |  | Week 13  | Week 14 | 5 hours  | 11-25-22 |  |
| 19 | Program switches on board                          |  | Complete     | 4 hours  |  | Week 13  | Week 14 | 5 hours  | 11-25-22 |  |
| 20 | Program display screen on board                    |  | Complete     | 8 hours  |  | Week 13  | Week 14 | 8 hours  | 11-25-22 |  |
| 21 | Program timer on board                             |  | Complete     | 8 hours  |  | Week 13  | Week 14 | 5 hours  | 11-25-22 |  |
| 22 | Design block diagram of board                      |  | Complete     | 3 hours  |  | Week 13  | Week 14 | 2 hours  | 11-1-22  |  |
| 23 | Create task list for board                         |  | Complete     | 3 hours  |  | Week 1   | Week 3  | 3 hours  | 10-1-22  |  |
| 24 | Create User Stories for board                      |  | Complete     | 5 hours  |  | Week 4   | Week 6  | 5 hours  | 11-1-22  |  |
| 25 | Create Requirements for Board                      |  | Complete     | 5 hours  |  | Week 4   | Week 6  | 5 hours  | 11-1-22  |  |
| 26 | Create the Final Architecture Plan                 |  | Complete     | 20 hours |  | Week 7   | Week 9  | 5 hours  | 11-20-22 |  |
| 27 | Begin Coding the project                           |  | Complete     | 20 hours |  | Week 10  | Week 12 | 10 hours | 11-21-22 |  |
| 30 | Get Proposal Peer Reviewed                         |  | Complete     | 1 hour   |  | 9-8-22   | 9-20-22 | 1 hour   | 9-19-22  |  |
| 31 | Get Requirements Peer Reviewed                     |  | Complete     | 1 hour   |  | Week 4   | Week 6  | 1 hour   | 9-25-22  |  |
| 32 | Get Architecture Plan Peer Reviewed                |  | Complete     | 1 hour   |  | Week 7   | Week 9  | 1 hour   | 11-18-22 |  |
| 33 | Code Drop 2  |  | Scheduled    |          |  | Week 15  | Week 20 | 10 hours |          |  |
| 34 | Code Drop 1  |  | Scheduled    |          |  |          |         |          |          |  |
| 35 | Code Drop 3  |  | Scheduled    |          |  | Week 20  | Week 25 | 10 hours |          |  |
| 36 | Benchmark Final Project                            |  | Scheduled    |          |  | Week 25  | Week 30 | 10 hours |          |  |
| 37 | Test First Code Drop                               |  | Scheduled    |          |  | Week 12  | Week 13 | 10 hours | 12-18-22 |  |
| 38 | Test Code Drop 2                                   |  | Scheduled    |          |  | Week 13  | Week 14 | 10 hours |          |  |
| 39 | Test Code Drop 3                                   |  | Scheduled    |          |  | Week 23  | Week 24 | 1 hour   |          |  |
| 40 | Learn how to operate a 7-segment display           |  | Scheduled    |          |  | Week 11  | Week 12 | 8 hours  |          |  |
| 41 | Test Go Lang for if it can make the LED light up   |  | Out-of-scope |          |  | N/A      | N/A     | 8 hours  |          |  |
| 42 | Test Go Lang for controlling the timer             |  | Out-of-scope |          |  | N/A      | N/A     | 3 hours  |          |  |
| 43 | Test Go Lang for controlling the 7-segment display |  | Out-of-scope |          |  | N/A      | N/A     | 3 hours  |          |  |
| 44 | Test Go Lang for switches                          |  | Out-of-scope |          |  | N/A      | N/A     | 3 hours  |          |  |
| 45 | Test Go Lang for buttons                           |  | Out-of-scope |          |  | N/A      | N/A     | 3 hours  |          |  |
| 46 | Set up FPGA Development Environment                |  | Scheduled    | 4 hours  |  | 9-16-22  | 9-18-22 | 4 hours  | 9-18-22  |  |
| 47 | Complete Activity 8                                |  | Scheduled    | 10 hours |  | 12-1-22  | 12-5-22 | 5 hours  |          |  |



## Project Success Measures

| Project Completion Criteria  |  |
|--|--|
| 1 – Demonstrate the ability to properly develop a program for an FPGA board that can complete the designated requirements.                                 |  |
| 2 – Program the FPGA board to properly conduct logical operations utilizing the C programming language while adhering to VHDL standards.                   |  |
| 3 – Demonstrate the ability to properly configure the FPGA board using a BCD decoder to display information on the 7-segment display based off of a timer. |  |
| 4 – Demonstrate the ability to display content on the FPGA board's LCD screen.   |  |
| 5 – Demonstrate the ability to light up the LED lights on the FPGA board.  |  |
| 6 – Demonstrate the ability to utilize switches and buttons on the FPGA board to configure the clock's settings.   |  |

## Assumptions and Constraints

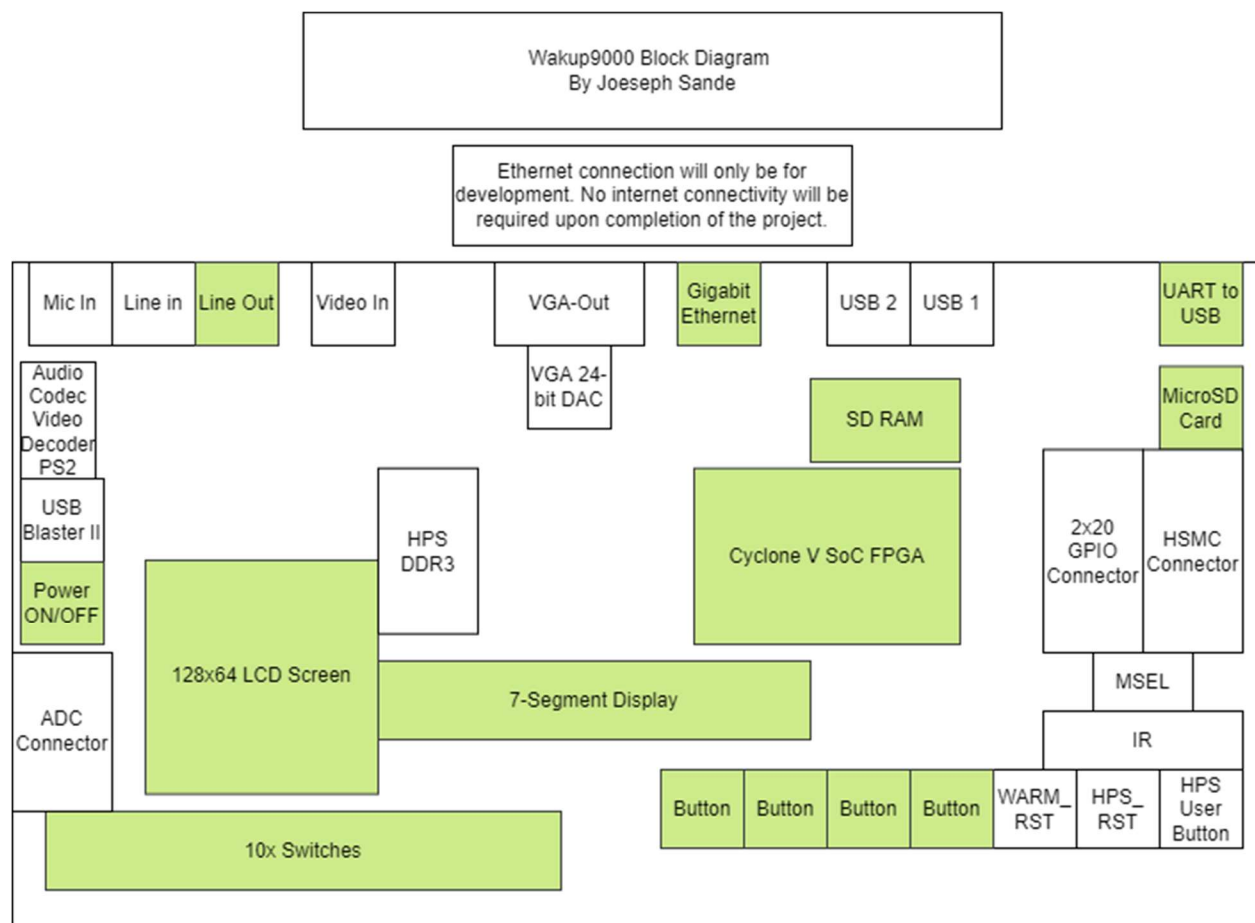
| Assumptions and Constraints |   |  |                           |          |              |
|-----------------------------|---|--|---------------------------|----------|--------------|
| ID                          | Description   | Comments   | Type                      | Status   | Date Entered |
| 1                           | Go Language can be substituted for C language programs.   | This will be saved for out of scope and assessed if there is time at the end.                        | Constraint (Out of Scope) | Blocked  | 9-14-22      |
| 2                           | FPGA board holds every component that is required to create a functional clock.   | The FPGA board contains all components required to make a functioning clock.                         | Assumption                | Resolved | 9-14-22      |
| 3                           | The training plan will cover everything the team requires to know to make this project function properly.                       | The plan goes over each element required to implement the project.                                   | Assumption                | Resolved | 9-14-22      |
| 4                           | The LCD Screen will be programmed in the clock's application. The LCD screen will not require a video input to display content. | The LCD Screen will be programmed in the clock's application.  | Constraint                | Pending  | 9-14-22      |
| 5                           | The 7-segment display will display messages with a BCD decoder.   | The BCD decoder should translate the commands for the 7-segment display to show designated messages. | Constraint                | Pending  | 9-14-22      |

## Project High-Level Solution

### Introduction

The challenge being addressed with this project the Wakeup9000 is the ability to wake the heaviest sleeper from their naps and for the team to gain familiarity with FPGA products to implement more complex solutions to future problems. This project will be the team's first interaction with imbedded systems, so this is a perfect challenge for them. The DE-10 Standard FPGA Board has every component required to create a functioning clock that will cover all of the required specifications of waking up a heavy sleeping individual. The necessary components that will be utilized to achieve this goal are the buttons, switches, lights, 7-segment display, and LCD screen.

### Block Diagram of High-Level Solution



### **Components Utilized:**

1. LCD Screen – will be utilized to display messages to the user.
2. 10x switches – will be utilized to configure settings for the clock.
3. 4x buttons – will be utilized to configure settings for the clock.
4. LED lights – will light up when the alarm goes off.
5. 7-Segment Display – will be used to display the timer of the clock.
6. MicroSD Card Slot – will be used to hold the program files for the clock.
7. Gigabit Ethernet port – will be used to connect the clock to a computer for development using FileZilla data transfers.
8. UART to USB port – will be used to connect the board to a development environment.
9. USB Port – is optional for a WIFI adapter, but will not be used in this project.
10. Cyclone V SoC FPGA Processor- will be used to process the application.
11. SD RAM- will be used to process the application.

### **High-Level Solution Description**

The solution to creating the Wakup9000 will incorporate the components within the board on the above diagram. This board runs on an ARM processor that will be programmed to incorporate the components listed above. This board will utilize its buttons and switches for providing the user with the ability to configure the board's settings, to turn off, and to reset the alarm. The Cyclone V SoC FPGA Processor will process all of the requests being sent to the board. The 128x64 LCD Screen will display the messages for what the alarm is relating to for the user. The MicroSD Card slot will hold the MicroSD card that contains the Linux and program files for the board to operate. The 7-segment display will be where the time is shown on the board. The use of the Gigabit Ethernet or a WIFI adapter to a USB slot on the board is optional to provide internet capabilities for the board and will only be required for development purposes.

## Project Controls

| Risk Management   |                          |   |  |  |
|---|--------------------------|---|--|--|
| Event Risk  | Risk Probability         | Risk Impact   | Risk Mitigation  | Contingency Plan   |
|   | (high, medium, low)      |   |  |  |
| What is the risk?   | What is the probability? | What is the impact if the risk occurs?  | What can be done to minimize the risk?   | What can be done to minimize the impact of the risk?   |
| Not ramping up enough on the general knowledge required to program an FPGA board. | Medium                   | This would lead to abandoning the project if the training plan is not adhered to.   | Complete the training plan.  | Complete the training plan to become familiar with the FPGA board and regularly hold team standups.  |
| If Go Lang can't replace C programming language.                                  | High                     | Go Lang not having the capabilities of replacing C would be devastating to the project if that is one of the initial goals. | This has been placed in the out-of-scope list to be pulled in scope later if there is still time for a proof of concept at the end of the project. | Program the board in the C programming language instead of Go Lang and conduct a proof of concept for Go Lang once the main project is complete. |
| Coding the FPGA components incorrectly.   | Low                      | This will enable the ability to complete the required feature of the project.   | Complete training plan to become familiar with each component of the board.  | Lower the number of components utilized on the board.  |
| Not properly integrating fundamental FPGA programming concepts in the project.    | Low                      | This would lead to not having the project completed by the deadline.  | Keep on schedule and plan out all tasks to ensure they are completed.  | Hold accountability with the weekly reports.   |
| Not adhering to the VHDL programming standards.                                   | Low                      | This would not meet the project completion requirement for this project.  | Learn about VHDL programming standards and implement them into the project.  | Ensure the code is written with the VHDL programming standards from the start of the application.  |
| Not running the program's functions asynchronously.                               | Low                      | This would make the clock inaccurate in keeping track of the time.  | Implement code to run asynchronously.  | Ensure each component runs through their programmed cycle as intended without interrupting the others.   |

**Issues:** No known Issues at this time.

| Issues Log |                    |  |  |                         |            |              |                |               |
|------------|--------------------|--|--|-------------------------|------------|--------------|----------------|---------------|
| ID         | Description        | Project Impact                               | Action Plan/Resolution                     | Owner                   | Importance | Date Entered | Date to Review | Date Resolved |
| 1          | What is the issue? | How will this impact scope, schedule & cost? | How do you intend to deal with this issue? | Who manages this issue? |            |              |                |               |
| 2          |                    |  |  |                         |            |              |                |               |
| 3          |                    |  |  |                         |            |              |                |               |

| Change Control Log |                    |          |            |              |               |           |        |                  |                    |
|--------------------|--------------------|----------|------------|--------------|---------------|-----------|--------|------------------|--------------------|
| ID                 | Change Description | Priority | Originator | Date Entered | Date Assigned | Evaluator | Status | Date of Decision | Included in Rev. # |
| 1                  |                    |          |            |              |               |           |        |                  |                    |
| 2                  |                    |          |            |              |               |           |        |                  |                    |

## Project Cost

| Project Cost |                                     |          |         |                |               |                         |          |                 |                   |
|--------------|-------------------------------------|----------|---------|----------------|---------------|-------------------------|----------|-----------------|-------------------|
| ID           | Item Description                    | Priority | Vendor  | Date Purchased | Date Received | Use                     | Cost     | Amount Required | Shipping Location |
| 1            | DE10-Standard FPGA Board            | High     | Terasic | 7-13-22        | 7-20-22       | Main component          | \$355    | 1               | Company           |
| 2            | AC Power Cord                       | High     | Terasic | 7-13-22        | 7-20-22       | Power FPGA Board        | \$4.50   | 1               | Company           |
| 3            | 16GB Micro SDHC Card and SD Adapter | High     | Terasic | 7-13-22        | 7-20-22       | Memory storage for FPGA | \$15     | 1               | Company           |
| 4            | Ethernet Cable                      | High     | Amazon  | 7-13-22        | 7-20-22       | Developing connectivity | \$7      | 1               | Company           |
| 5            | USB WIFI Dongle                     | Low      | Terasic | 7-13-22        | 7-20-22       | Internet connectivity   | \$8      | 1               | Company           |
| 6            | Shipping                            | High     | FedEx   | 7-13-22        | 7-20-22       | Ship products           | \$52.34  | 1               | Company           |
|              |                                     |          |         |                |               | TOTAL:                  | \$441.84 |                 |                   |

## **Appendix A – References**

## **Appendix B – Copyright Compliance**