

# DS90UB971-Q1 FPD-Link IV 7.55-Gbps Serializer With CSI-2 Interface for 8MP+ Cameras, RADAR & Other Sensors

## 1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Device temperature: -40 to +115°C ambient operating temperature range specified for electrical performance
- 7.55 Gbps (6 Gbps Video Payload) Supports High-Speed Sensors Including 8MP+ Imagers
- Power-over-Coax (PoC) Compatible Transceiver
- Single MIPI D-PHY Port with 4 Lanes
  - Compliant to MIPI D-PHY v2.1
  - 1 Clock Lane and 1, 2, or 4 Configurable Data Lanes
  - Up to 1.5 Gbps/Lane, 6Gbps/Port
  - Supports Polarity Pin Inversion (p/n)
  - 16 Virtual Channels
- Single Port MIPI CSI-2 Receiver
  - Compliant to MIPI CSI-2 v2.1
  - Supports Multiple Data Types and Multi-Exposure
- Advanced Data Protection and Diagnostics Including CRC Data Protection, Sensor Data Integrity Check, I2C Write Protection, Voltage and Temperature Measurement, Programmable Alarm and Line Fault Detection
- Flexible Programmable Output Clock Generator
- Supports Single-Ended Coaxial or Shielded-Twisted-Pair (STP) Cable
- Ultra-Low Latency Bidirectional I2C and GPIO Control Channel Enables ISP Control From ECU
- Single 1.8-V Power Supply
- Compatible with DS90UB9702-Q1, DS90UB954-Q1, DS90UB936-Q1, DS90UB960-Q1, DS90UB962-Q1 Deserializers
- Pin Compatible with DS90UB953-Q1, DS90UB953A-Q1, DS90UB935-Q1, DS90UB951-Q1 Serializers
- Small 5-mm × 5-mm VQFN Package and Solution Size for Compact Sensor Module Designs

## 2 Applications

- Automotive Driver Assistance Systems (ADAS)
  - Surround View Systems (SVS)
  - Camera Monitor Systems (CMS)
  - Forward Vision Cameras (FC)
  - Driver Monitoring Systems (DMS)
  - Rear-View Cameras (RVC)
  - Automotive Satellite RADAR & LIDAR Modules
  - Time-of-Flight (ToF) Sensors
- Security and Surveillance Cameras
- Industrial and Medical Imaging

## 3 Description

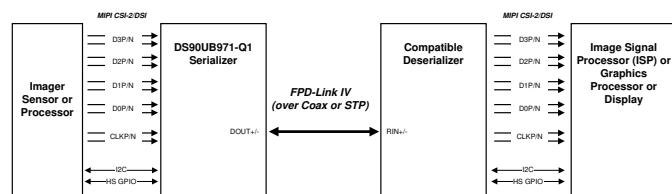
The DS90UB971-Q1 serializer represents the first generation in FPD-Link IV serializers and is designed to support ultra-high-speed raw data sensors including 8MP+ Imagers, satellite RADAR, LIDAR, and Time-of-Flight (ToF) sensors. The chip delivers an 7.55-Gbps forward channel and an ultra-low latency, 47.1875-Mbps bidirectional control channel and supports power over a single coax (PoC) or STP cable. The DS90UB971-Q1 features advanced data protection and diagnostic features to support ADAS and automotive functional safety. Together with a companion deserializer, the DS90UB971-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

The DS90UB971-Q1 is fully AEC-Q100 qualified with a wide temperature range of -40°C to 115°C. The serializer comes in a small 5-mm × 5-mm VQFN package for space-constrained sensor applications.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
DS90UB971-Q1	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



### Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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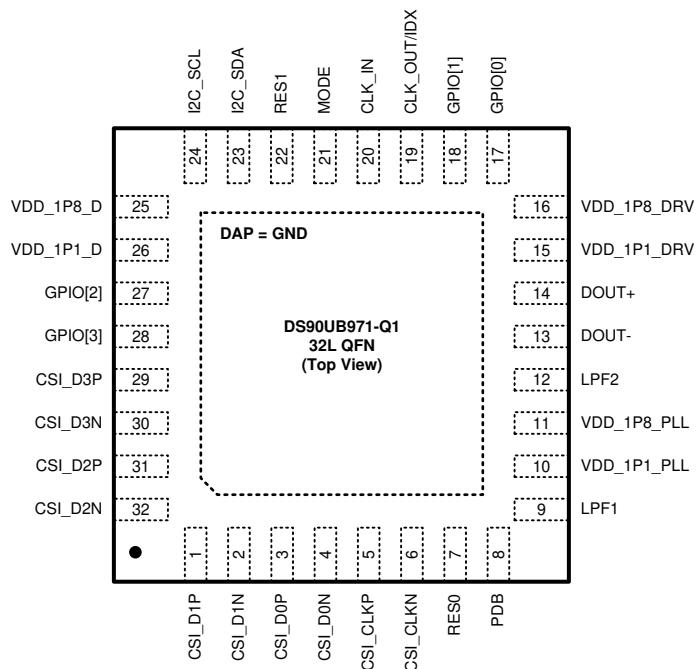
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2021) to Revision A (September 2021)	Page
• Production Data Custom NDA release.....	1

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## 5 Pin Configuration and Functions



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**Figure 5-1. RHB Package, 32-Pin VQFN, Top View**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
<b>CSI INTERFACE</b>			
CSI_CLKP	5	I, DPHY	CSI-2 clock input pins. Connect to a CSI-2 clock source with matched 100- $\Omega$ ( $\pm 5\%$ ) differential impedance interconnects.
CSI_CLKN	6	I, DPHY	
CSI_D0P	3	I, DPHY	
CSI_D0N	4	I, DPHY	
CSI_D1P	1	I, DPHY	
CSI_D1N	2	I, DPHY	CSI-2 data input pins. Connect to a CSI-2 data sources with matched 100- $\Omega$ ( $\pm 5\%$ ) differential impedance interconnects. If unused, these pins may be left floating.
CSI_D2P	31	I, DPHY	
CSI_D2N	32	I, DPHY	
CSI_D3P	29	I, DPHY	
CSI_D3N	30	I, DPHY	
<b>SERIAL CONTROL INTERFACE</b>			
I2C_SDA	23	I/O, OD	I2C Data and Clock Pins for the bidirectional control bus communication. Pulled up to either 1.8-V or 3.3-V supply rail depending on IDX setting. See <a href="#">I2C Interface Configuration</a> for further details on the I2C implementation of the DS90UB971-Q1. See <a href="#">I2C Bus Pullup Resistor Calculation</a> (SVLA689).
I2C_SCL	24	I/O, OD	
<b>CONFIGURATION and CONTROL</b>			
RES0	7	I	Reserved pin – Connect to GND
RES1	22	I	Reserved pin – Leave OPEN
PDB	8	I, PD	Power-down inverted Input Pin. Typically connected to processor GPIO with pull down. When PDB input is brought HIGH, the device is enabled and internal register and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN. PDB should remain low until after power supplies are applied and reach minimum required levels. <b>PDB INPUT IS NOT 3.3-V TOLERANT.</b> PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down.

**Table 5-1. Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE	21	S	MODE Select Pin. Applying an appropriate bias allows configuration of the mode. Typically connected to a voltage divider via external pull-up to VDD18 and pull-down to GND. See <a href="#">MODE</a> .
CLK_OUT/IDX	19	I, S	I2C Serial Control Bus Primary ID Address Select. IDX pin sets the I2C pullup voltage and device address; connect to external pullup to VDD and pulldown to GND to create a voltage divider. When PDB transitions LOW to HIGH, the strap input voltage is sensed at the CLOCK_OUT/IDX pin to determine functionality and then converted to CLK_OUT. See <a href="#">IDX</a> . If unused, it may be tied to GND.
<b>FPD-LINK IV INTERFACE</b>			
DOUT-	13	I/O	FPD-Link IV Input/Output. The pin must be AC-coupled with a capacitor. If using coax configuration, use a 100nF AC coupling capacitor for DOUT+ and terminate DOUT- to GND with a 47nF capacitor and 50Ω resistor. If using STP configuration, connect both DOUT+ and DOUT- with 100nF AC-coupling capacitors. See <a href="#">Typical Application</a> for typical connection diagram .
DOUT+	14	I/O	
<b>POWER AND GROUND</b>			
VDD_1P1_D	26	D, P	A connection for internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01- µF capacitors to GND.
VDD_1P1_DRV	15	D, P	A connection for internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01- µF capacitors to GND.
VDD_1P1_PLL	10	D, P	A connection for internal analog regulator decoupling capacitor. Typically connected to 10-µF, 0.1-µF, and 0.01- µF capacitors to GND.
VDD_1P8_D	25	P	1.8-V (±5%) Power Supply pin. Requires 10-µF and 0.01-µF capacitors to GND.
VDD_1P8_DRV	16	P	1.8-V (±5%) Analog Power Supply pin. Requires 10-µF and 0.01-µF capacitors to GND.
VDD_1P8_PLL	11	P	1.8-V (±5%) Analog Power Supply pin. Requires 10-µF and 0.01-µF capacitors to GND.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the QFN package. Connect to the ground plane (GND).
<b>LOOP FILTER</b>			
LPF1	9	P	Loop Filter 1: Connect as described in <a href="#">Typical Application</a> .
LPF2	12	P	Loop Filter 2: Connect as described in <a href="#">Typical Application</a> .
<b>CLOCK INTERFACE and GPIO</b>			
GPIO0	17	I/O, PD	General-Purpose Input/Output pins. The Internal Pulldown is 25 kΩ (typ). These pins can also be configured to sense the voltage at their inputs. At power-up these pins default to inputs. If unused, these pins may be left floating, however, it is recommended to disable them by setting the GPIOx_INPUT_EN to 0. Note that GPIO0 is part of the power-up sequence, see <a href="#">Figure 9-1</a> .
GPIO1	18	I/O, PD	General-Purpose Input/Output pins. Internal Pulldown is 25 kΩ (typ). At power-up these pins default to inputs. If unused, these pins may be left floating, however, it is recommended to disable them by setting the GPIOx_INPUT_EN to 0.
GPIO2	27	I/O, PD	General-Purpose Input/Output pins. Internal Pulldown is 25 kΩ (typ). At power-up these pins default to inputs. If unused, these pins may be left floating, however, it is recommended to disable them by setting the GPIOx_INPUT_EN to 0.
GPIO3	28	I/O, PD	General-Purpose Input/Output pins. Internal Pulldown is 25 kΩ (typ). At power-up these pins default to inputs. If unused, these pins may be left floating, however, it is recommended to disable them by setting the GPIOx_INPUT_EN to 0.
CLK_IN	20	I	Reference Clock Input pin. If operating in Non-Synchronous CLK_IN clocking mode, connect this pin to a local clock source. If unused (other clocking modes), this pin may be left open. Reference <a href="#">Table 8-3</a> for CLK_IN requirements.

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- OD = Open Drain
- PD = Internal Pulldown
- P, G = Power supply, Ground
- D = Decoupling pin for internal LDO output
- S = Strap Input
- DPHY = MIPI D-PHY Compliant pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

			MIN	MAX	UNIT
Supply voltage	VDD (VDD_1P8_D, VDD_1P8_DRV, VDD_1P8_PLL)		-0.3	2.16	V
Input voltage	GPIO[3:0], PDB, CLK_IN		-0.3	2.16	V
Input voltage	CSI_D3P, CSI_D3N, CSI_D2P, CSI_D2N, CSI_D1P, CSI_D1N, CSI_D0P, CSI_D0N, CSI_CLKP, CSI_CLKN	CSI_D3P, CSI_D3N, CSI_D2P, CSI_D2N, CSI_D1P, CSI_D1N, CSI_D0P, CSI_D0N, CSI_CLKP, CSI_CLKN	-0.3	1.35	V
FPD-Link IV output voltage	Device powered up (VDD18 within recommended operating conditions)		-0.3	1.21	V
Open-Drain voltage	I2C_SDA, I2C_SCL		-0.3	3.96	V
Junction temperature, T <sub>J</sub>			-40	150	°C
Storage temperature, T <sub>stg</sub>			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.

### 6.2 ESD Ratings

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	ESD Rating (IEC 61000-4-2, powered-up only), RD=330Ω, Cs=150pF	Contact Discharge: DOUT+ and DOUT-	±8	kV
		ESD Rating (ISO10605), RD=330Ω, Cs=150pF and 330pF	Contact Discharge: DOUT+ and DOUT-	±8	
		ESD Rating (ISO10605), RD=2kΩ, Cs=150pF and 330pF	Contact Discharge: DOUT+ and DOUT-	±8	
		ESD Rating (IEC 61000-4-2, powered-up only), RD=330Ω, Cs=150pF	Air Discharge: DOUT+ and DOUT-	±18	
		ESD Rating (ISO10605), RD=330Ω, Cs=150pF and 330pF	Air Discharge DOUT+ and DOUT-	±18	
		ESD Rating (ISO10605), RD=2kΩ, Cs=150pF and 330pF	Air Discharge DOUT+ and DOUT-	±18	
		ESD (HBM) per AEC Q100-002	All pins except DOUT+ and DOUT-	±4	
		ESD (HBM) per AEC Q100-002	Pins DOUT+ and DOUT-	±7	
		ESD (CDM) per AEC Q100-001	Charged-device model (CDM) ESD Classification Level C5, per AEC Q100-011	±1.25	

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**6.3 Thermal Information**

THERMAL METRIC <sup>(1)</sup>		DS90UB971-Q1	UNIT
		VQFN	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	31.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	20.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	11.6	°C/W

(1) Thermal data in accordance with JESD51. For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

**6.4 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	VDD (VDD_1P8_D, VDD_1P8_DRV, VDD_1P8_PLL)	1.71	1.8	1.89	V
Open drain voltage	I <sub>2</sub> C_SDA, I <sub>2</sub> C_SCL = V <sub>I<sub>2</sub>C</sub>	1.71		3.6	V
Operating free air temperature, T <sub>A</sub>		-40	25	115	°C
MIPI data rate (per CSI-2 lane)		80		1500	Mbps
CLK_IN Reference clock input frequency (+/- 100 ppm), FPD3 4.16 Gbps	CLK_IN Reference clock input frequency (+/- 100 ppm), FPD3 4.16 Gbps		26		MHz
CLK_IN Reference clock input frequency (+/- 50 ppm), FPD4 7.55 Gbps			25		MHz
Local I <sub>2</sub> C Clock Frequency, f <sub>SCL</sub>				1	MHz
Supply noise	VDD (VDD_1P8_D, VDD_1P8_DRV, VDD_1P8_PLL)		25		mV <sub>P-P</sub>
Differential Supply Noise between DOUT+ and DOUT- (PSR)	f = 10KHz - 50MHz (coax mode only)		25		mV <sub>P-P</sub>
	f = 30Hz, 10-90% Rise/Fall time > 100us (coax mode only)		25		mV <sub>P-P</sub>
Input clock rise/fall time for non-synchronous mode	CLK_IN Reference clock input rise/fall time 20% - 80% @ 15pF load	0.1	3		ns
Input clock duty cycle for non-synchronous mode	CLK_IN Reference clock input duty cycle	40	50	60	%
Input clock load capacitance for non-synchronous mode	CLK_IN Reference clock load capacitance		20		pF
Input clock RMS jitter for non-synchronous mode (t <sub>JIT</sub> )	CLK_IN Reference clock absolute RMS jitter		80		ps
Input clock jitter for synchronous mode (t <sub>JIT</sub> )	Deserializer (UB954/960 Backward Compatibility) Reference clock jitter		200		ps
Input clock jitter for synchronous mode (t <sub>JIT</sub> )	Deserializer (UB9702) Reference clock jitter		200		ps
Back channel input jitter (t <sub>JIT-BC</sub> )	DOUT+, DOUT-		0.4		UI <sub>BC</sub>

**6.5 DC Electrical Characteristics**

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>TOTAL POWER CONSUMPTION</b>							
P <sub>T5</sub>	Total power consumption	FPD 7.55 Gbps; CSI-2 1.5 Gbps (4L + 1 CLK)	VDD_1P8_D, VDD_1P8_DRV, VDD_1P8_PLL		488		mW

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$P_{T6}$	Total power consumption	FPD 4.16 Gbps - Backwards Compatibility CSI-2 832 Mbps (4L + 1 CLK)	VDD_1P8_D, VDD_1P8_DRV, VDD_1P8_PLL			412	mW
<b>SUPPLY CURRENT</b>							
$I_{DD5}$	Supply current	FPD 7.55 Gbps CSI-2 1.5 Gbps (4L + 1 CLK)	VDD_1P8_D			88	mA
$I_{DD5}$	Supply current	FPD 7.55 Gbps CSI-2 1.5 Gbps (4L + 1 CLK)	VDD_1P8_DRV			79	mA
$I_{DD5}$	Supply current	FPD 7.55 Gbps CSI-2 1.5 Gbps (4L + 1 CLK)	VDD_1P8_PLL			90	mA
$I_{DD6}$	Supply current	FPD 4.16 Gbps - Backwards Compatibility CSI-2 832 Mbps (4L + 1 CLK)	VDD_1P8_D			76	mA
			VDD_1P8_DRV			62	
			VDD_1P8_PLL			79	
$I_{DDZ}$	Shutdown current	PDB = LOW	ALL VDD PINS			1.1	mA
<b>1.8V LVC MOS I/O</b>							
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA	GPIO[3:0], CLK_OUT	$V_{(VDD18)} - 0.45$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = +4$ mA	GPIO[3:0], CLK_OUT	0		0.45	V
$V_{IH}$	High-level input voltage	$V_{(VDD18)} = 1.71$ V to 1.89 V	GPIO[3:0], PDB, CLK_IN	$0.65 \times V_{(VDD18)}$		$V_{(VDD18)}$	V
$V_{IL}$	Low-level input voltage	$V_{(VDD18)} = 1.71$ V to 1.89V	GPIO[3:0], PDB, CLK_IN	0		$0.35 \times V_{(VDD18)}$	V
$I_{IH\_CLKIN}$	Input high current	$V_{IN} = 0$ or 1.71 V to 1.89 V	PDB, CLK_IN	-5		5	$\mu A$
$I_{IH\_GPIO}$	Input high current	$V_{IN} = 0$ or 1.71 V to 1.89 V, PULL DOWN = Disabled	GPIO[3:0]	-20		20	$\mu A$
$I_{IH\_GPIO}$	Input high current	$V_{IN} = 0$ or 1.71 V to 1.89 V, PULL DOWN = Enabled	GPIO[3:0]	-80		80	$\mu A$
$I_{IL}$	Input low current	$V_{IN} = 0$ or 1.71 V to 1.89 V	GPIO[3:0], PDB, CLK_IN	-20			$\mu A$
$I_{OS}$	Output short circuit current	$V_{OUT} = 0$ V				-35	mA
$I_{OZ\_CLKOUT}$	TRI-STATE output current	$V_{OUT} = 0$ V or $V_{(VDD18)}$ , PDB = L	CLK_OUT	-5		5	$\mu A$
$I_{OZ\_GPIO}$	TRI-STATE output current	$V_{OUT} = 0$ V or $V_{(VDD18)}$ , PDB = L	GPIO[3:0]	-20		20	$\mu A$
$C_{IN}$	Input capacitance					5	pF
<b>I2C DC SPECIFICATIONS</b>							
$V_{IL}$	Input low-level		I2C_SDA, I2C_SCL	0	$0.3 \times V_{(I2C)}$		V
$V_{HYS}$	Input hysteresis		I2C_SDA, I2C_SCL		>50		mV
$V_{OL1}$	Output low-level	Standard-mode/Fast-mode, $I_{OL} = 3$ mA, $V_{(I2C)} = 3.0$ V to 3.6 V	I2C_SDA, I2C_SCL	0		0.4	V
		Fast-mode Plus, $I_{OL} = 20$ mA, $V_{(I2C)} = 3.0$ V to 3.6 V	I2C_SDA, I2C_SCL	0		0.4	V

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**6.5 DC Electrical Characteristics (continued)**

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$V_{OL2}$	Output low-level	Standard-mode/Fast-mode $I_{OL} = 3 \text{ mA}$ , $V_{(I2C)} = 1.71 \text{ V to } 1.89 \text{ V}$	I2C_SDA, I2C_SCL	0		$0.2 \times V_{(I2C)}$	V
		Fast-mode Plus $I_{OL} = 20 \text{ mA}$ , $V_{(I2C)} = 1.71 \text{ V to } 1.89 \text{ V}$	I2C_SDA, I2C_SCL	0		0.4	V
$I_{OL}$	Output Low-level current	Standard/Fast Mode	I2C_SDA, I2C_SCL		3		mA
		Fast-mode Plus	I2C_SDA, I2C_SCL		20		mA
$I_{IL}$	Input current	$V_{IN} = 0\text{V}$	I2C_SDA, I2C_SCL	-10		10	$\mu\text{A}$
$C_{IN}$	Input capacitance		I2C_SDA, I2C_SCL		5		pF

**VOLTAGE AND TEMPERATURE SENSING**

$V_{ACC}$	Voltage sensor accuracy			1.5	%
$T_{ACC}$	Temperature sensor accuracy	-10°C to 105°C junction temperature		±5	°C

**FPD-LINK IV DC SPECIFICATIONS**

$ V_{OUTl} $	Single-ended Output Amplitude	$R_L = 50\Omega$	DOUT+, DOUT-	520	575	670	mV
$ V_{OD,P-P} $	Differential Output Amplitude	$R_L = 100\Omega$		1040	1150	1340	mV
$\Delta V_{OD}$	Output differential voltage imbalance	$R_L = 100\Omega$ across DOUT+, DOUT-		1	50		mV
$V_{os}$	Output differential offset voltage	$R_L = 100\Omega$ across DOUT+, DOUT-		0.525			V
$\Delta V_{os}$	Offset voltage imbalance	$R_L = 100\Omega$ across DOUT+, DOUT-		1	50		mV
$I_{os}$	Output short -circuit current	DOUT = 0V		-20			mA
$R_T$	Internal Termination Resistor	Single-ended DOUT+ or DOUT-		40	50	60	$\Omega$
		Differential across DOUT+ and DOUT-		80	100	120	$\Omega$

**FPD-LINK IV BI-DIRECTIONAL CONTROL CHANNEL**

$V_{IN-BC}$	Back channel single ended input voltage	$R_L = 50\Omega$ Single-ended configuration	DOUT+, DOUT-	120			mV
$V_{ID-BC}$	Back channel differential input voltage	$R_L = 100\Omega$ Differential configuration		240			mV
$S_{11}$	Return Loss of TX	$f_{FCMAX} = 4.2 \text{ GHz}, 2.1\text{GHz}$		-12			dB
		$f_{BC} = 10 \text{ MHz (non-sync)}, 25\text{MHz (95x sync)}, 50\text{MHz (97x/95x sync)}$		-20			dB

**HSRX DC SPECIFICATIONS**

$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	DPHY CTS	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N	70	330		mV
$V_{IDTH}$	Differential input high threshold	DPHY CTS			70		mV
$V_{IDTL}$	Differential input low threshold	DPHY CTS		-70			mV
$V_{IHHS}$	Single-ended input high voltage	DPHY CTS			460		mV
$V_{ILHS}$	Single-ended input low voltage	DPHY CTS		-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	DPHY CTS			450		mV
$Z_{ID}$	Differential Input Impedance			80	100	125	$\Omega$

**LPRX DC SPECIFICATIONS**

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	Logic 1 input voltage	Applicable to all data rates D-PHY v2.1 onwards.	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N	740	mV	
V <sub>IL</sub>	Logic 0 input voltage			300		
V <sub>HYST</sub>	Input hysteresis			25		

## 6.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>GPIO LVCMOS I/O AC SWITCHING CHARACTERISTICS</b>						
t <sub>CLH</sub>	LVCMOS low-to-high transition-time	V <sub>VDD</sub> = 1.71 to 1.89 V, C <sub>L</sub> = 8pF (lumped load), Default Registers	GPIO[3:0]	2	ns	
t <sub>CHL</sub>	LVCMOS high-to-low transition-time	V <sub>VDD</sub> = 1.71 to 1.89 V, C <sub>L</sub> = 8pF (lumped load), Default Registers	GPIO[3:0]	2		
TJ <sub>CLK_OUT</sub>	CLK_OUT output jitter (integer M/N)	Synchronous and Non-synchronous - measure cycle to cycle jitter CLK_OUT, 5 MHz to 40 MHz	CLK_OUT	0.4	ns	
	CLK_OUT output jitter (fractional M/N)	Synchronous and Non-synchronous - measure cycle to cycle jitter CLK_OUT, , 5 MHz to 40 MHz		1.5		
t <sub>CLK_OUT-DLY_SYNC</sub>	CLK_OUT Delay	SER running, SYNC mode, PDB on DES, 9702 REFCLK Stable, 97x Supplies Stable, 7.55G Sync Mode, 47.1875MHz BC	CLK_OUT	20	ms	
t <sub>CLK_OUT-DLY_NONSYNC</sub>	CLK_OUT Delay	SER running, NON-SYNC mode, PDB on SER, 9702 REFCLK Stable, 97x Supplies Stable, 7.55G non-sync mode, 9.4375MHz BC, 25MHz CLK_IN	CLK_OUT	20		
DC <sub>CLK_OUT</sub>	CLK_OUT Duty Cycle	Synchronous and Non-synchronous	CLK_OUT	45	50	55 %
t <sub>PDB</sub>	PDB reset pulse width	Voltage supplies stable		3	ms	
t <sub>TSD</sub>	Serializer delay	Data in to Data out, DPHY 4lane, 1500Mbps/lane, 7.55Gbps FPD4 sync mode: RAW12, 30fps, 3840x2168		75		
f <sub>DEV</sub>	Spread spectrum clocking deviation frequency	Synchronous Mode, BC = 47.1875MHz		+/- 0.25	kHz	
f <sub>MOD</sub>	Spread spectrum clocking modulation frequency	Synchronous Mode, BC = 47.1875MHz		33		
<b>FPD-LINK IV AC SPECIFICATIONS</b>						
f <sub>FC</sub>	Forward Channel Line Rate	FPD-Link III (Backwards Compatibility)	DOUT+, DOUT-	4.16	Gbps	

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## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$f_{FC}$	Forward Channel Line Rate	FPD-Link IV	DOUT+, DOUT-			7.55	Gbps
$f_{BC}$	Back Channel Data Rate	FPD Synchronous: 47.1875 Mbps	DOUT+, DOUT-			47.1875	Mbps
$f_{BC}$	Back Channel Data Rate	FPD Synchronous: 50 Mbps	DOUT+, DOUT-			50	Mbps
$f_{BC}$	Back Channel Data Rate	FPD Synchronous: 52 Mbps	DOUT+, DOUT-			52	Mbps
$f_{BC}$	Back Channel Data Rate	FPD Non-synchronous: 9.4375 Mbps	DOUT+, DOUT-			9.4375	Mbps
$f_{BC}$	Back Channel Data Rate	FPD Non-synchronous: 10 Mbps (Backward Compatibility)	DOUT+, DOUT-			10.4	Mbps
$t_{JIT-FC}$	Forward channel output jitter	Non-Sync & Synchronous mode, 4.16Gbps total output jitter	DOUT+, DOUT-			0.3	UI <sub>FC</sub>
$t_{JIT-FC}$	Forward channel output jitter	Nonsync & Synchronous mode, 7.55Gbps total output jitter	DOUT+, DOUT-			0.3	UI <sub>FC</sub>
$t_{RF}$	Forward channel rise/fall time	20% to 80%	DOUT+, DOUT-		45		ps
$E_{H-FC}$	Forward channel output eye height	Coax configuration, 7.55Gbps, PRBS15 <sup>(1)</sup>	DOUT+, DOUT-	228			mV <sub>p</sub> <sub>p</sub>
		STP configuration (non- sync mode), 7.55Gbps, PRBS15 <sup>(1)</sup>	DOUT+, DOUT-	456			mV <sub>p</sub> <sub>p</sub>

(1) Measurement includes PCB and recommended external components

## 6.7 AC Electrical Characteristics CSI-2

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>HSRX AC SPECIFICATIONS</b>							
$\Delta V_{CMRX(HF)}$	Common-mode Interference beyond 450MHz	DPHY CTS	Data rate $\leq$ 1.5 Gbps			100	mV
$\Delta V_{CMRX(LF)}$	Common-mode Interference 50MHz to 450MHz	DPHY CTS	Data rate $\leq$ 1.5 Gbps	-50		50	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	DPHY CTS				450	mV
$C_{CM}$	Common-mode termination	For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification				60	pF
<b>LPRX AC SPECIFICATIONS</b>							
$e_{SPIKE}$	Input pulse rejection	DPHY CTS				300	V*ps
$T_{MIN-RX}$	Minimum pulse width response	DPHY CTS		20			ns
$V_{INT}$	Peak interference amplitude	DPHY CTS				200	mV
$f_{INT}$	Interference frequency	DPHY CTS		450			MHz
<b>DATA-CLOCK TIMING SPECIFICATIONS</b>							
$U_{INST}$	UI instantaneous	1, 2, or 4 lane configurations		0.667		12.5	ns

## 6.7 AC Electrical Characteristics CSI-2 (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$\Delta UI$	UI variation	DPHY CTS	UI $\geq$ 1ns	-0.1	0.1	UI <sub>HS</sub>	
			0.667ns < UI < 1ns	-0.05	0.05	UI <sub>HS</sub>	
$t_{\text{SETUP}(\text{RX})}$	RX Data to clock setup time tolerance	DPHY CTS	Data rate: 0.08 Gbps to 1 Gbps	0.15			UI <sub>HS</sub>
		DPHY CTS	Data rate: 1 Gbps to 1.5 Gbps	0.2			UI <sub>HS</sub>
$t_{\text{HOLD}(\text{RX})}$	RX Data to clock hold time tolerance	DPHY CTS	Data rate: 0.08 Gbps to 1 Gbps	0.15			UI <sub>HS</sub>
		DPHY CTS	Data rate: 1 Gbps to 1.5 Gbps	0.2			UI <sub>HS</sub>

### MIPI D-PHY RECEIVER RETURN LOSS CHARACTERISTICS

SDD <sub>RX</sub>	RX differential return loss	$f_h \text{MIN}$	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-15	dB
SDD <sub>RX</sub>	RX differential return loss	$f_h$	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-8.5	dB
SDD <sub>RX</sub>	RX differential return loss	$f_h \text{MAX}$	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-2.9	dB
SCC <sub>RX</sub>	RX common-mode return loss	1/4 $f_{\text{INT}}$ , MIN	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		0	dB
SCC <sub>RX</sub>	RX common-mode return loss	$f_{\text{INT}}$ , MIN	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-6	dB
SCC <sub>RX</sub>	RX common-mode return loss	$f_h \text{MAX}$	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-6	dB
SDC <sub>RX</sub>	RX mode conversion	>0 to $f_h \text{MAX}$	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLKP/N		-26	dB

## 6.8 Recommended Timing for the Serial Control Bus

Over I<sup>2</sup>C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
$f_{\text{SCL}}$	SCL Clock Frequency	Standard-mode	>0	100	kHz	
		Fast-mode	>0	400	kHz	
		Fast-mode Plus	>0	1	MHz	

## 6.8 Recommended Timing for the Serial Control Bus (continued)

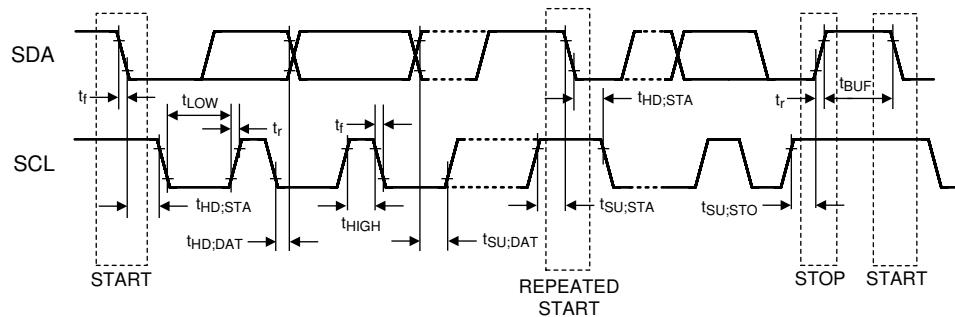
Over I<sup>2</sup>C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
$t_{LOW}$	SCL Low Period	Standard-mode	4.7			μs
		Fast-mode	1.3			μs
		Fast-mode Plus	0.5			μs
$t_{HIGH}$	SCL High Period	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{HD:DAT}$	Data hold time	Standard-mode	0	3.45		μs
		Fast-mode	0	0.9		μs
		Fast-mode Plus	0	0.45		μs
$t_{SU:DAT}$	Data set up time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU:STO}$	Set up time for STOP condition	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{BUF}$	Bus free time between STOP and START	Standard-mode	4.7			μs
		Fast-mode	1.3			μs
		Fast-mode Plus	0.5			μs
$t_r$	SCL and SDA rise time	Standard-mode		1000		ns
		Fast-mode		300		ns
		Fast-mode Plus		120		ns
$t_f$	SCL and SDA fall time	Standard-mode		300		ns
		Fast-mode		300		ns
		Fast-mode Plus		120		ns
$C_b$	Capacitive load for each bus line	Standard-mode		400		pF
		Fast-mode		400		pF
		Fast-mode Plus		550		pF
$t_{VD:DAT}$	Data valid time	Standard-mode		3.45		μs
		Fast-mode		0.9		μs
		Fast-mode Plus		0.45		μs
$t_{VD:ACK}$	Data valid acknowledge time	Standard-mode		3.45		μs
		Fast-mode		0.9		μs
		Fast-mode Plus		0.45		μs
$t_{SP}$	Input filter	Standard-mode		50		ns
		Fast-mode		20		ns
		Fast-mode Plus		6		ns

## 6.9 Timing Diagrams



**Figure 6-1. LVC MOS Transition Times**



**Figure 6-2. I2C Serial Control Bus Timing**

## 7 Detailed Description

### 7.1 Overview

The DS90UB971-Q1 serializes data from high-resolution image sensors or other sensors using the MIPI CSI-2 interface and can support 8MP+ imagers. The DS90UB971-Q1 serializer is optimized to interface with the DS90UB9702-Q1 (quad hub deserializer), DS90UB954-Q1 (dual hub deserializer), DS90UB936-Q1 (dual hub deserializer), DS90UB962-Q1 (quad hub deserializer) or the DS90UB960-Q1 deserializer (quad hub deserializer) as well as potential future deserializers. Interconnect between the serializer and the deserializer can be either coaxial cable, or shielded-twisted-pair (STP) cable. The DS90UB971-Q1 was designed to support multi-sensor systems such as surround view, and as such has the ability to synchronize sensors through the DS90UB954-Q1, DS90UB936-Q1, DS90UB962-Q1 hub, DS90UB960-Q1 hub and DS90UB9702-Q1 (quad hub). A compatibility matrix for the DS90UB971-Q1 is shown in [Table 7-1](#).

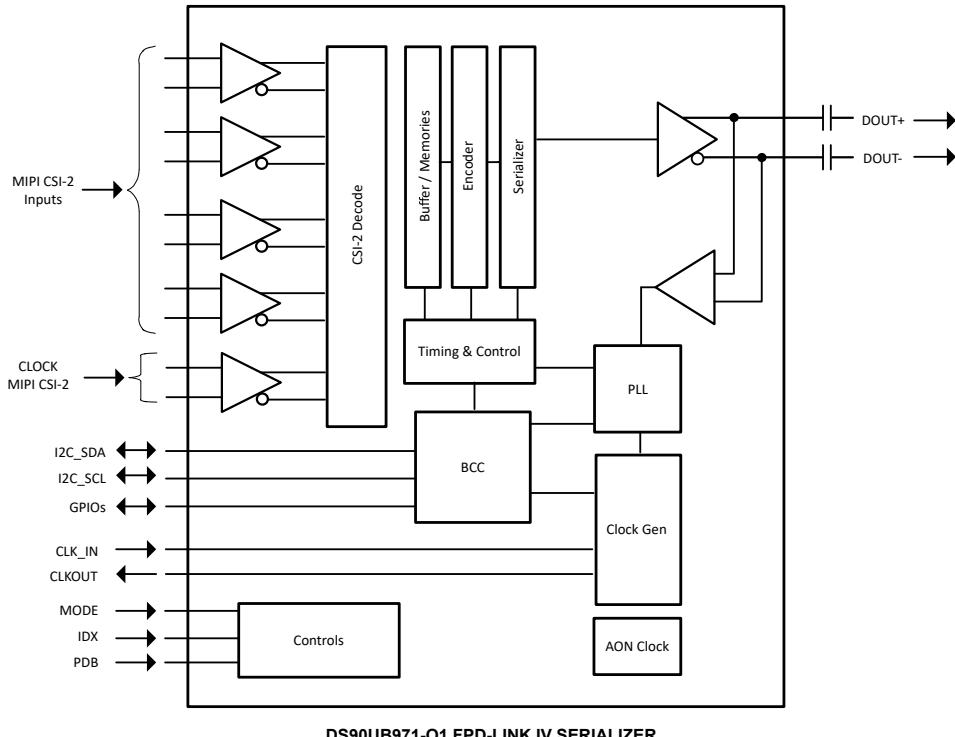
The DS90UB971-Q1 serializer and companion deserializer incorporate an I2C-compatible interface. The I2C-compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer and deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another.

**Table 7-1. DS90UB971-Q1 Compatibility Matrix**

Deserializer	UB9702-Q1	UB964-Q1	UB962-Q1	UB960-Q1	UB954-Q1	UB936-Q1	UB934-Q1	UB914A-Q1
Compatibility	Yes	No	Yes	Yes	Yes	Yes	No	No

### 7.2 Functional Block Diagram



**DS90UB971-Q1 FPD-LINK IV SERIALIZER**

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## 7.3 Feature Description

The DS90UB971-Q1 serializer is designed to support high-speed raw data sensors including 8MP+ imagers, satellite RADAR, LIDAR, and Time-of-Flight (ToF) sensors. The chip features a forward channel capable of up to 7.55 Gbps and an ultra-low latency 47.1875-Mbps bidirectional control channel. The transmission of the forward channel, bidirectional control channel, and power is supported over coaxial (Power-over-Coax) or STP cables. The DS90UB971-Q1 features advanced data protection and diagnostic features to support ADAS and autonomous driving. Together with a companion deserializer, the DS90UB971-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

### 7.3.1 CSI-2 Receiver

The DS90UB971-Q1 receives CSI-2 video data from the Sensor. During CSI-2 operation, the DPHY consists of a clock lane and one or more data lanes (1,2, or 4 lane configuration) with speeds of 80 Mbps to 1.5 Gbps (per lane) supported. The DPHY data and clock lane polarity is capable of switching pin polarity via register 0x20-0x21. The receiver supports all data types including custom data types listed in the CSI-2 v2.1 standard. The receiver also supports up to 16 virtual channels to comply with CSI-2 v2.1 specifications. The DS90UB971-Q1 is a CSI-2 slave device and only supports unidirectional lanes in the Forward direction. Low Power Escape mode is not supported.

#### 7.3.1.1 CSI-2 Receiver Operating Modes

During normal operation a Data Lane will be either in Control or High-Speed mode. In High-Speed mode, the data transmission happens in a burst and starts and ends at a Stop state (LP-11). There is a transition state to take the D-PHY from a Normal mode to the Low-Power state.

The sequence to enter High-Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a Stop state (LP-11) is received.

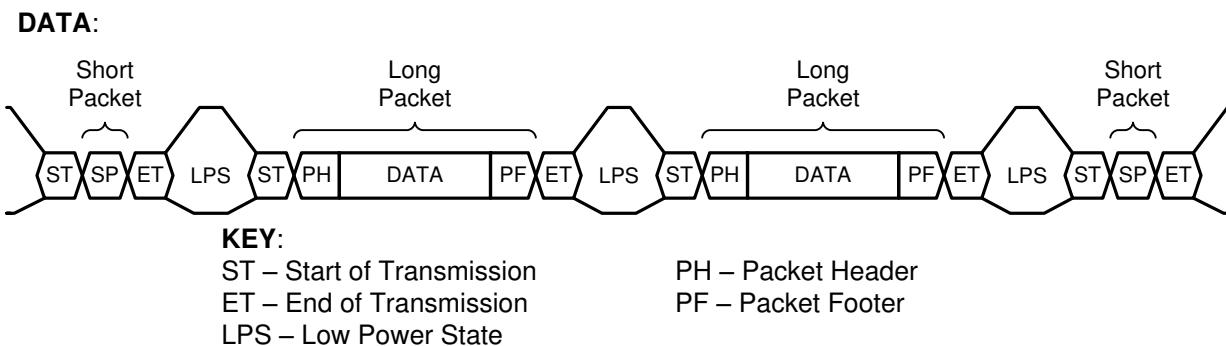
#### 7.3.1.2 CSI-2 Receiver High-Speed Mode

During high-speed data transmission, the digital D-PHY will enable termination signal to allow proper termination of the HS RX of the Analog D-PHY, and the LP RX should stay at LP-00 state. Both CSI-2 data lane and clock lane operate in the same manner. DS90UB971-Q1 support CSI-2 continuous clock lane mode, where the clock LP RX stays at LP-00 state.

#### 7.3.1.3 CSI-2 Protocol Layer

There are two different types of CSI-2 packets, a short packet and a long packet. Short packets have information such as the Frame Start/Line Start, and long packets carry the data after the frame start is asserted.

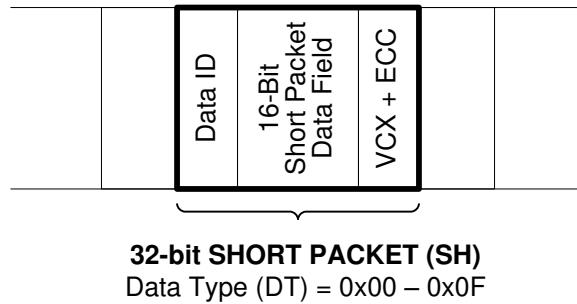
Figure 7-1 shows the CSI-2 protocol layer with short and long packets.



**Figure 7-1. CSI-2 Protocol Layer With Short and Long Packets**

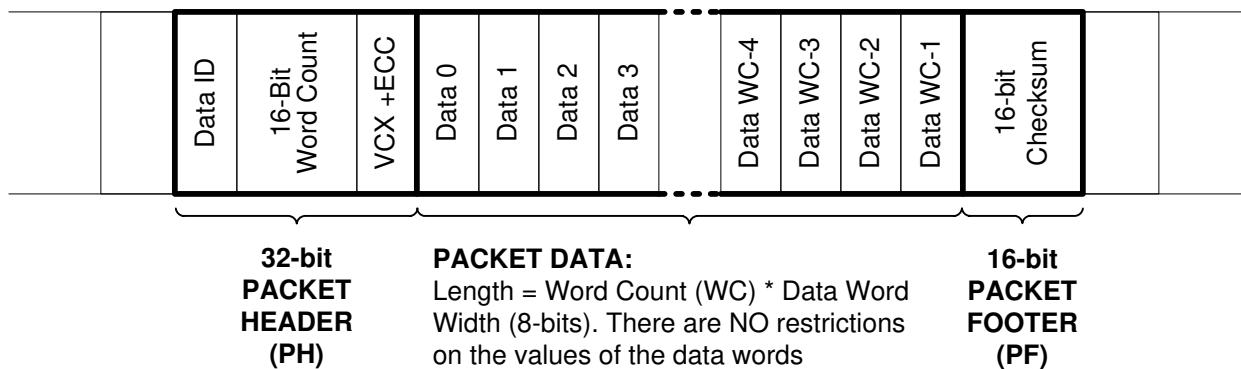
#### 7.3.1.4 CSI-2 Short Packet

The short packet provides frame or line synchronization. Figure 7-2 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

**Figure 7-2. CSI-2 Short Packet Structure**

### 7.3.1.5 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer has one element, a 16-bit checksum. [Figure 7-3](#) shows the structure of a long packet.

**Figure 7-3. CSI-2 Long Packet Structure****Table 7-2. CSI-2 Long Packet Structure Description**

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	VCX + ECC	2 + 6	2-bit virtual channel extension (VCX) and 6-bit ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC × 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

### 7.3.1.6 CSI-2 Errors and Detection

#### 7.3.1.6.1 CSI-2 ECC Detection and Correction

The CSI-2 packet header contains 6-bit Error Correction Code (ECC). ECC code in the 32-bit long packet header can be corrected when there is 1-bit error and detected when there is 2-bit error. This feature is added to monitor the CSI-2 input for ECC 1-bit error correction. When ECC error is detected, ECC error detection register will be set and an alarm indicator bit can be sent to the deserializer to indicate the ECC error has been detected. Register 0x1C control can be used to either enable or disable the alarm.

#### 7.3.1.6.2 CSI-2 Check Sum Detection

The CSI-2 long packet header contains 16-bit check sum before end of transmission. DS90UB971-Q1 calculates the check sum of the incoming CSI-2 data. If check sum error is detected, the check sum error status will be saved in the CSI\_ERR\_STATUS register (0x5D) and the status can also be forwarded to the deserializer through the bidirectional control channel.

### 7.3.1.6.3 CSI-2 Receiver Status

For the Receive ports, several status functions can be tracked and monitored through register access. The status indications are available for error conditions as well as indications of change in line length measurements. These are available through the CSI\_ERR\_COUNT (0x5C), CSI\_ERR\_STATUS (0x5D), CSI\_ERR\_DLANE01 (0x5E), CSI\_ERR\_DLANE23 (0x5F), and CSI\_ERR\_CLK\_LANE (0x60) registers.

For interleaved CSI Virtual Channels, VC selection can be enabled by setting bit 0x30[5] and a Virtual Channel can be selected with bits 0x31[7:4]. When VCI is enabled, registers 0x61 through 0x6A will show information pertaining to the selected VC

## 7.3.2 FPD-Link IV Forward-Channel Transmitter

The DS90UB971-Q1 features a high-speed signal transmitter capable of driving signals at rates of up to 7.55 Gbps.

### 7.3.2.1 Frame Format

The DS90UB971-Q1 formats the data into 40-bit long frames. Each frame is encoded to ensure DC balance, and to ensure sufficient data line transitions. Each frame contains video payload data, I2C forward channel data, CRC information, framing information, and information regarding the state of the CSI-2 interface. This 40-bit frame includes 32 bits of video payload data, so the maximum video payload is 32/40 \* forward channel line rate.

## 7.3.3 FPD-Link IV Back-Channel Receiver

The FPD-Link IV back-channel receives an encoded back channel signal over the FPD-Link IV interface. The back channel frame is a 30-bit frame which contains I2C commands and GPIO data. The back channel frame receives an encoded clock and data from the deserializer, thus the data bit rate is one-half the frequency of the highest frequency received.

The back channel frequency is programmable for operation with compatible deserializers. The default setting is determined by the MODE strap pin. For operation with different deserializers and different clocking modes, reference [Table 7-12](#).

## 7.3.4 Serializer Status and Monitoring

The DS90UB971-Q1 features enhanced FPD-Link IV diagnostics, system monitoring, and Built-in Self Test capabilities. It monitors forward channel and back channel data for errors and reports them in the status registers. It also supports on-chip temperature sensing, external voltage sensing, internal supply voltage sensing, and line fault detection for system level diagnostics. The Built-in Self Test feature allows testing of the forward channel and back channel data transmissions without external data connections.

### 7.3.4.1 Forward Channel Diagnostics

The DS90UB971-Q1 monitors the status of the forward channel link. The forward channel high-speed PLL lock status is reported in the HS\_PLL\_LOCK bit (Register 0x52[2]). When paired with the deserializer, the LOCK status is also reported in the RX\_LOCK\_DETECT bit (Register 0x52[6]).

### 7.3.4.2 Back Channel Diagnostics

The DS90UB971-Q1 monitors the status of the back channel link. The back channel CRC errors are reported in the CRC\_ERR bit (Register 0x52[1]). The number of CRC errors are stored in the CRC error counters and reported in the CRC\_ERR\_CNT1 (Register 0x55) and CRC\_ERR\_CNT2 (Register 0x56) registers. The CRC error counters are reset by setting the CRC\_ERR\_CLR (Register 0x49[3]) to 1.

When running the BIST function, the DS90UB971-Q1 reports if a BIST CRC error is detected in the BIST\_CRC\_ERR bit (Register 0x52[3]). The number of BIST errors are reported in the BIST\_ERR\_CNT field (Register 0x54). The BIST CRC error counter is reset by setting the BIST\_CRC\_ERR\_CLR (Register 0x49[5]) to 1.

### 7.3.4.3 Built-In Self Test

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

The BIST mode is enabled by BIST configuration register 0x14[3] on the deserializer. Run the test in the synchronous mode. When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the content of the error counter in the BIST\_ERR\_COUNT register 0x54 for each RX port on the deserializer side. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

### 7.3.4.4 Alarm Control

The DS90UB971-Q1 has the capability to send an alarm bit and status bit to the Deserializer. The alarm bit can be enabled or disabled through register settings while the status bit is always transmitted to the Deserializer. In general there are two main interrupt categories: CSI-2 alarm errors and Bidirection Control Channel alarm errors. The CSI-2 alarm is triggered by any of the following events: CSI-2 no valid frames error, DPHY sync errors, DPHY ctrl errors, CSI-2 ECC 2-bit errors, CSI-2 checksum (CRC) error, and CSI-2 length errors. The BCC alarm is triggered by the following two events: CRC errors, and Link detect errors.

To enable the alarm bit, program [6:0] in register 0x1C for CSI-2 interrupts and [1:0] in register 0x1E for Link interrupts. Alarms will be reported on the Deserializer side in SENSOR\_STS\_X. To monitor the status read register 0x5D [4:0], 0x5E, 0x5F, 0x60, 0x64 [7], and 0x68 for the different CSI-2 alarm events and 0x52 [1:0] for different BCC alarm events.

### 7.3.4.5 Interrupt Control

Although the DS90UB971-Q1 has no interrupt pins, it has the capability to send an interrupt status to the Deserializer. The alarm bit can be enabled or disabled through register settings while the status bit can always be read locally. In general there are five main interrupt categories: Loss of CLK\_IN interrupt, temperature sensor interrupt, voltage sensor interrupt, and line fault interrupt.

To enable global and local device interrupts, program [7:6] in register 0x11 and enable the individual interrupts in [4:0] in register 0x1B. Regardless of enabling interrupt, the status shall be reported in register 0x57 and 0x58 [4:0] for the different interrupt events.

### 7.3.4.6 Sensing

The DS90UB971-Q1 contains internal diagnostic features comprising of voltage sensing, temperature sensing, and line fault detection. The DS90UB971-Q1 features an 8-bit ADC for both internal and external voltage monitoring (the voltage sensor will not react to high frequency signals beyond 100 Hz). Internal VDD18 voltage rail sensing can be used to measure the internal bias voltages as well as the DC IR drop on the supply voltage routing.

The DS90UB971-Q1 also contains a temperature sensor to measure the die temperature and store the reading using an 8-bit ADC with an accuracy of +/- 5°C from -10°C to 105°C.

The DS90UB971-Q1 has the ability to use external line fault circuitry to detect open/shorts on the link cable.

### 7.3.4.6.1 Temperature Sensing

The DS90UB971-Q1 uses a SAR ADC and a thermal diode to measure the die temperature. The die temperature is read and stored in the TEMP\_FINAL (0x13) register on the SAR ADC Register Page. The following formula converts the TEMP\_FINAL decimal code to Celsius:

$$\text{Temperature} = (0.5637 \times \text{TEMP\_FINAL}) - 19.937 \quad (1)$$

The DS90UB971-Q1 can also trigger an interrupt when the device temperature exceeds the maximum value of the TEMP\_HIGH (0x33) register or falls below the TEMP\_LOW (0x34) register. The TEMP\_HIGH and TEMP\_LOW registers can be found on the SAR ADC Register Page. To enable this interrupt's status to be displayed on the INTB pin, set b'6 of the INTERRUPT\_CTL (reg 0x23) register on the Main Page to 1. By default, this interrupt will trigger when internal temperatures exceed 77°C or fall below 39°C. These thresholds can be changed by writing to the TEMP\_HIGH and TEMP\_LOW registers on the SAR ADC Register page.

### 7.3.4.6.2 Internal Supply Voltage Sensing

The DS90UB971-Q1 can use the internal SAR ADC to monitor the voltage levels of the 1.8 V supplies. The ADC can read voltages of two different pins. On the SAR ADC Register Page, IV0\_FINAL and IV1\_FINAL are used to read the 1.8 V supplies.

**Table 7-3. Supply Voltage Sensing Register Map**

Supply Pin	Nominal Voltage	Register Name	Register Address
VDD_1P8_DRV	1.8 V	IV0_FINAL	0x15
VDD_1P8_PLL	1.8 V	IV1_FINAL	0x16

The voltage equation to convert the decimal code for IV0\_FINAL and IV1\_FINAL (1.8V rail) is as follows:

$$\text{Voltage (V)} = \frac{4.3 \times 'IVx\_FINAL'}{255} + \frac{0.2 \times 'TEMP\_FINAL'}{1000} + \frac{5}{1000} \quad (2)$$

The DS90UB971-Q1 can also trigger an interrupt when the supply voltage goes above or below specific voltages. To enable this interrupt's status to be displayed on the INTB pin, set b'6 of the INTERRUPT\_CTL (reg 0x23) register on the Main Page to 1. The upper or lower voltage thresholds can be changed by voltage threshold registers on the SAR ADC Register Page. Refer to the following table for the default supply threshold levels and the corresponding registers. These thresholds can be changed by writing to the IVx\_HIGH and IVx\_LOW registers on the SAR ADC Register Page.

**Table 7-4. Default Supply Voltage Threshold Levels**

Supply Pin	Upper Voltage Threshold (V)	Upper Voltage Threshold Register Address	Lower Voltage Threshold	Lower Voltage Threshold Register Address
VDD_1P8_DRV	1.884	0x70	1.716	0x66
VDD_1P8_PLL	1.884	0x70	1.716	0x66

### 7.3.4.6.3 External Supply Voltage Sensing

The SAR ADC can read the voltages at GPIO0 and GPIO1. These two pins can read voltages up to 1.43 V. If a higher voltage is to be read, an external voltage divider is required. The external voltage monitor registers can be found on the SAR ADC Register Page. In order to read the GPIO voltage, EXT\_VOL0 (reg 0x08[0]) must be enabled for GPIO0, and EXT\_VOL1 (reg 0x08[1]) must be enabled for GPIO1. The GPIO voltage can read from EXT\_VOL0\_FINAL (reg 0x1B) for GPIO0 and EXT\_VOL1\_FINAL (reg 0x1C) for GPIO1.

To calculate the voltage values from decimal code in EXT\_VOLx\_FINAL, use the following formula:

$$\text{Voltage (V)} = \left(1.421 + \frac{0.15}{1000} \times 'TEMP\_FINAL'\right) \times \frac{'EXT\_VOLx\_FINAL'}{255} \quad (3)$$

FPD-Link IV devices can also trigger an interrupt when the voltages the GPIOs go above or below specific voltages. To enable this interrupt's status to be displayed on the INTB pin set bit 6 of the INTERRUPT\_CTL (reg

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0x23) register on the Main Page to b'1. The registers used to set the upper and lower voltages in FPD-Link IV devices are shown in the table below.

**Table 7-5. External Voltage Threshold Register Map**

Description	Register Name	Register Address
GPIO0 Upper Threshold	EXT_VOL0_HIGH	0x4C
GPIO0 Lower Threshold	EXT_VOL0_LOW	0x4D
GPIO1 Upper Threshold	EXT_VOL1_HIGH	0x4F
GPIO1 Lower Threshold	EXT_VOL1_LOW	0x50

**7.3.4.6.4 Line Fault Detection**

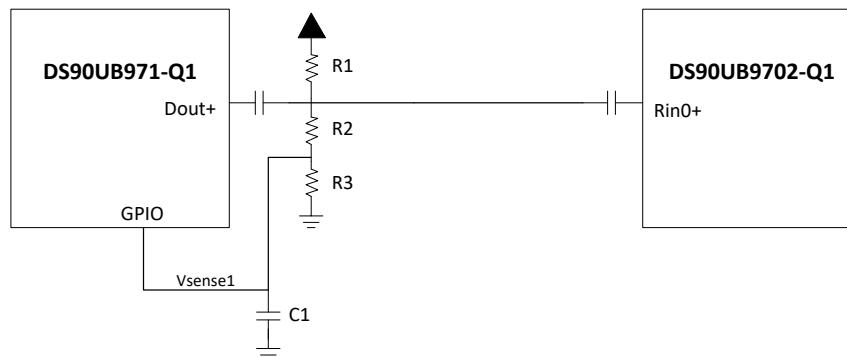
As part of the diagnostics features for the DS90UB971-Q1, the line fault detection circuitry can be used to detect faults with the connection between the serializer and deserializer. This is done by monitoring and sensing the voltage on the cable between the SerDes and transmitting that voltage to a GPIO on either the serializer or deserializer. If line fault detection is required on the serializer side of the FPD-Link system, examples are shown below.

The line fault detection circuit is a system level implementation and requires external circuitry. The circuitry will vary between single-ended PoC applications and differential STP configurations. This is because single ended coax applications are typically in ADAS systems where a PoC voltage can be used to detect faults on the cable. STP configurations are typically used in IVI applications, where there's no PoC voltage on the link, so the polarizing voltage between the two pairs of cables is used. Since there's positive and negative signals in STP configurations, the types of faults that can be detected will vary slightly between differential and single-ended cables. The table below provides a summary of the types of faults that can be detected between STP and coax.

**Table 7-6. STP vs Coax Line Faults**

STATUS	STP	COAX
Cable Open	Yes	Yes
"+" to "-" Short	Yes	-
"+" to GND Short	Yes	Yes
"-" to GND Short	Yes	-
"+" to Battery Short	Yes	Yes
"-" to Battery Short	Yes	-
PoC Voltage out of tolerance	-	Yes

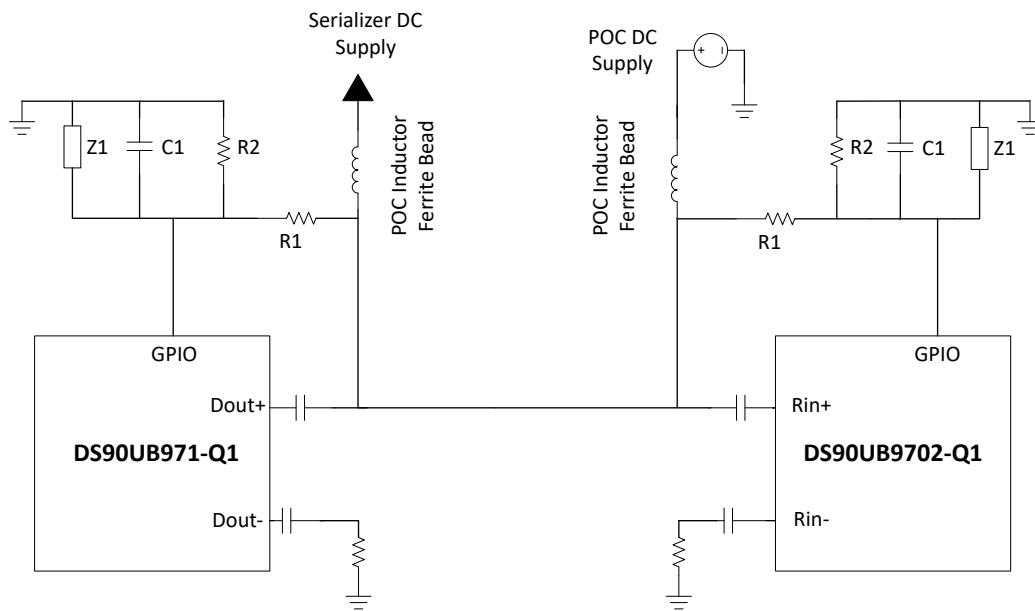
Figure 7-4 shows an example of line-fault detection circuit implementation for Coax applications. There is one voltage sensing node in Coax configurations. Table 7-7 shows recommended component values for a 1.8 V supply.

**Figure 7-4. Coax Line Fault Circuitry**

**Table 7-7. Coaxial Configuration Recommended Components**

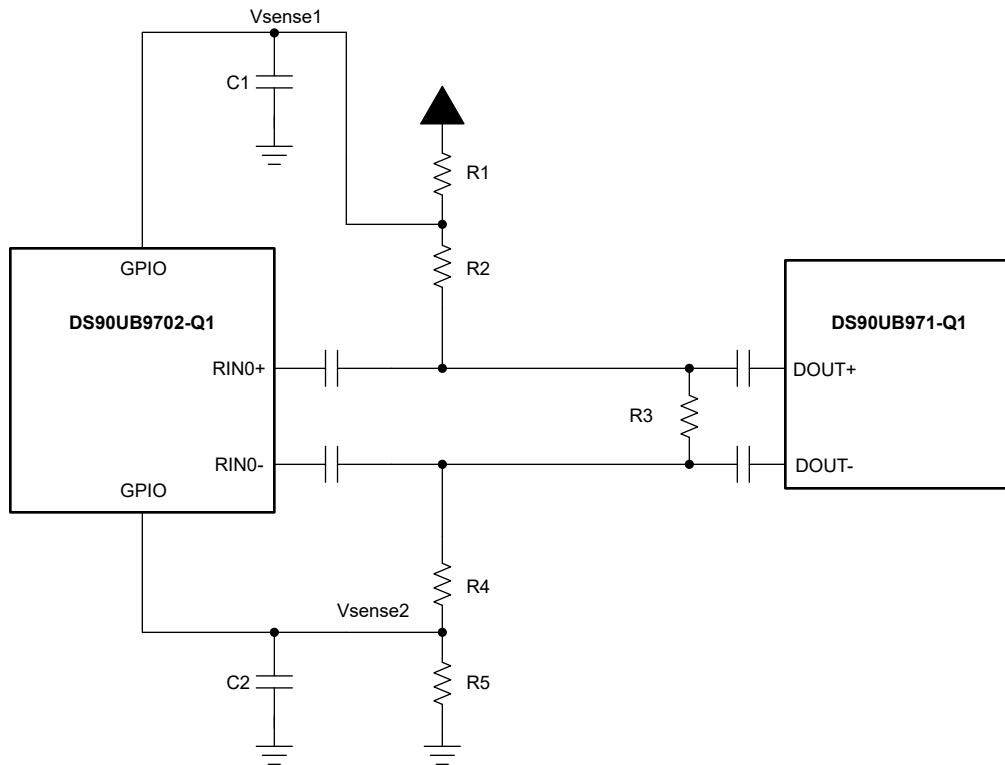
Reference Voltage	R1	R2	R3	C1
1.8 V	28 k	4.87 k	6.65 k	0.1 uF

For PoC applications, [Figure 7-5](#) shows an example of recommended line-fault detection circuit implementation. There is one voltage sensing node in the PoC configuration. The element Z1 is a placeholder for a diode protection circuit. Nominal PoC voltage is 9 V, with a low and high limit of 8.5 V and 9.5 V respectively. The battery voltage can have a range from 12 V to 13.5 V. Recommended component and supply values for PoC configurations are shown in [Table 7-8](#).

**Figure 7-5. PoC Line Fault Circuit Implementation****Table 7-8. PoC Configuration Recommended Components**

PoC Voltage	Battery Voltage	R1	R2	C1
9 V	12 V	10k ( $\pm 1\%$ )	1k ( $\pm 0.5\%$ )	0.1uF

[Figure 7-6](#) provides an example of the values for the passive components in Figure 1. R3 is required to be on the deserializer side because this ensures a current path that flows through the length of both differential cables. It is recommended that resistors with a 1% tolerance be used to ensure a high accuracy of the sensed voltage.

**Figure 7-6. STP Line Fault Circuitry****Table 7-9. Passive Component Recommendations for Differential Circuit Line Fault**

VSUPPLY	R1	R2	R3	R4	R5	C1	C2
1.8 V	25 k	10 k	10 k	10 k	10 k	0.1 uF	0.1 uF

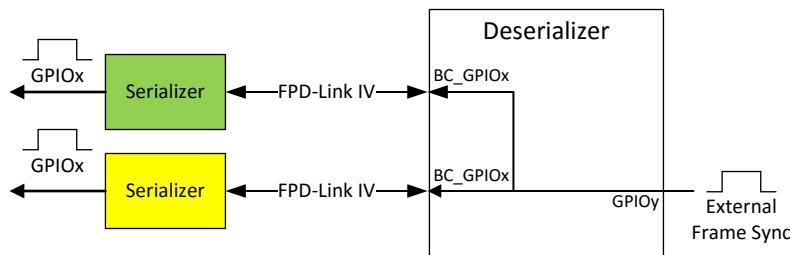
Contact Texas Instruments for additional information regarding Line Fault Detection.

### 7.3.5 FrameSync Operation

When paired with compatible deserializers, any of the DS90UB971-Q1 GPIO pins can be used for frame synchronization. This feature is useful when multiple sensors are connected to a deserializer hub. A frame synchronization signal (FrameSync) can be sent through the back channel using any of the back channel GPIOs. The FrameSync signal arrives at the serializers with limited skew.

#### 7.3.5.1 External FrameSync

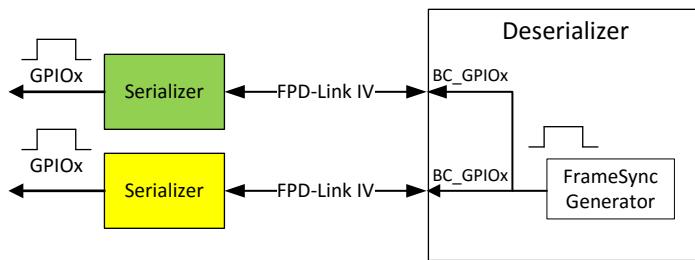
In External FrameSync mode, an external signal is input to the deserializer through one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached FPD-Link IV Serializers through a GPIO signal in the back channel.

**Figure 7-7. External FrameSync**

Enabling the external FrameSync mode is done on the deserializer side. Refer to the deserializer datasheet for more info.

### 7.3.5.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD-Link IV Serializers through a GPIO signal in the back channel.



**Figure 7-8. Internal FrameSync**

FrameSync operation is controlled by the deserializer registers. Refer to the deserializer datasheet for more info.

## 7.3.6 GPIO Support

The DS90UB971-Q1 supports four pins, GPIO0 through GPIO3, which can be monitored, configured, and controlled through I<sup>2</sup>C in registers 0x0D, 0x0E, and 0x53. These GPIOs are programmable for use in multiple options. GPIO0 and GPIO1 can have additional diagnostics functionality when programmed to sense external voltage levels.

### 7.3.6.1 GPIO Status

The status HIGH or LOW of each GPIO pin 0 through 3 may be read through the GPIO\_PIN\_STS register 0x53. This register read operation provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

### 7.3.6.2 GPIO Input Control

Upon initialization GPIO0 through GPIO3 are enabled as inputs by default. The GPIO\_INPUT\_CTL (0x0E) register, bits 3:0, allows control of the input enable. If a GPIO\_INPUT\_CTL[3:0] bit is set to 1, then the corresponding GPIO\_INPUT\_CTL[7:4] bit must be set to 0.

### 7.3.6.3 GPIO Output Control

Individual GPIO output control is programmable through the GPIO\_INPUT\_CTL (0x0E) register, bits 7:4. If a GPIO\_INPUT\_CTL[7:4] bit is set to 1, then the corresponding GPIO\_INPUT\_CTL[3:0] bit must be set to 0.

### 7.3.6.4 Forward Channel GPIO

The input on the DS90UB971-Q1 GPIO pins can be forwarded to compatible deserializers over the FPD-Link IV interface. Up to four GPIOs are supported in the forward direction.

The timing for the forward channel GPIO is dependant on the number of GPIOs assigned at the serializer. When a single GPIO input from the DS90UB971-Q1 serializer is linked to a compatible deserializer GPIO output the value is sampled every forward channel transmit frame. Two linked GPIO are sampled every two forward channel frames and three or four linked GPIO are sampled every 5 frames. As the information gets spread over multiple frames the jitter is typically increased on the order of the sampling period (number of forward channel frames). TI recommends maintaining a 4x oversampling ratio for linked GPIO throughput. The maximum recommended GPIO input frequency based on the number of GPIO linked over the specified forward channel frequency is shown in [Table 7-10](#).

**Table 7-10. Forward Channel GPIO Typical Timing**

FPD-Link IV LINE RATE (Gbps)	NUMBER OF LINKED FORWARD CHANNEL GPIOs (FC_GPIO_EN )	SAMPLING FREQUENCY (MHz)	MAXIMUM RECOMMENDED FORWARD CHANNEL GPIO FREQUENCY (MHz)	TYPICAL LATENCY (ns)	TYPICAL JITTER (ns)
7.55	1	188.75	47.19	42	12
	2	94.38	23.59	64	20
	4	47.19	11.8	130	36
3.775	1	105	26.25	85	12
	2	52.5	13.13	127	20
	4	21	5.25	254	36

### Code Example for Forward Channel GPIOs

```
# Enable Forward Channel GPIO0
# On DS90UB971-Q1
WriteI2C(0x0E, 0x01) # Set GPIO0 as input
WriteI2C(0x33, 0x01) # Set No. of Forward Channel GPIOs

# On DS90UB9702-Q1
WriteI2C(0x4C, 0x01) # Select RX Port 0
WriteI2C(0x10, 0x01) # Set GPIO0 SRC to RX Port 0 Received GPIO0
WriteI2C(0x59, 0x01) # Enable Forward Channel GPIOs
```

### 7.3.6.5 Back Channel GPIO

When enabled as an output, each DS90UB971-Q1 GPIO pin can be programmed to output remote data coming from the compatible deserializer using the LOCAL\_GPIO\_DATA register (0x0D). The maximum signal frequency that can be received over the FPD-Link IV back-channel is dependent on the DS90UB971-Q1 Clocking Mode as shown in [Table 7-11](#).

**Table 7-11. Back Channel GPIO Typical Timing**

DS90UB971-Q1 Clocking Mode	BACK CHANNEL RATE (Mbps)	SAMPLING FREQUENCY (kHz)	MAXIMUM RECOMMENDED BACK CHANNEL GPIO FREQUENCY (kHz)	TYPICAL LATENCY (μs)	TYPICAL JITTER (μs)
Synchronous Mode	47.1875	1572.91	432	1.5	0.7
Non-Synchronous CLK_IN Mode	9.4375	314	78	6.4	3.2
Non-Synchronous CLK_IN Mode	10.4	350	87.5	5.8	2.9

### Code Example Back Channel

```
# Enable Forward Channel GPIO0
# On DS90UB971-Q1
WriteI2C(0x0D, 0x11) # Set GPIO0 SRC as Remote GPIO0
WriteI2C(0x0E, 0x10) # Disable GPIO0 as Input, Enable as Output

# On DS90UB9702-Q1
WriteI2C(0x4C, 0x01) # Select RX Port 0
WriteI2C(0x0F, 0x01) # Set GPIO0 as Input
WriteI2C(0x6E, 0x00) # Enable Back Channel GPIO0
```

## 7.4 Device Functional Modes

### 7.4.1 Clocking Modes

The DS90UB971-Q1 supports two different clocking schemes, which are selected through the MODE pin. In the DS90UB971-Q1, the forward channel operates at a higher bandwidth than the requirement set by the video data being transported, and the forward channel data rate is set by a reference clock. The clocking mode determines what the device uses as its reference clock, and the most common configuration is the Synchronous Mode, in which no local reference oscillator is required. The other clocking mode is Non Synchronous Mode in which a local oscillator is required on the DS90UB971-Q1. Reference the [Section 8.2.2](#) for detailed requirements when operating in either mode. The DS90UB971-Q1 also has the ability to connect to FPD-Link III deserializers as well using the FPD-Link III versions of the modes shown in [Table 7-12](#).

**Table 7-12. Clocking Modes**

Clock Mode	Reference Source	CLK_IN Frequency (MHz)	FC Data Rate (Gbps)	BCC Data Rate (Mbps)	CSI BANDWIDTH (Gbps)
Synchronous FPD-Link IV	Back Channel	N/A	7.55	47.1875	6
Non-Synchronous FPD-Link IV	External Clock	25	7.55	9.4375	6
Synchronous FPD-Link III	Back Channel	N/A	3.775 - 4.16	47.1875 - 52	FC x (32/40)
Synchronous FPD-Link III (26MHz Back-Channel)	Back Channel	N/A	3.775 - 4.16	23.59375 - 26	FC x (32/40)
Non-Synchronous FPD-Link III External Clock	External Channel	23.59375 - 26	3.775 - 4.16	9.4375 - 10.4	FC x (32/40)
Non-Synchronous FPD-Link III Internal Clock	971 Internal Clock	N/A	4	10	3.2

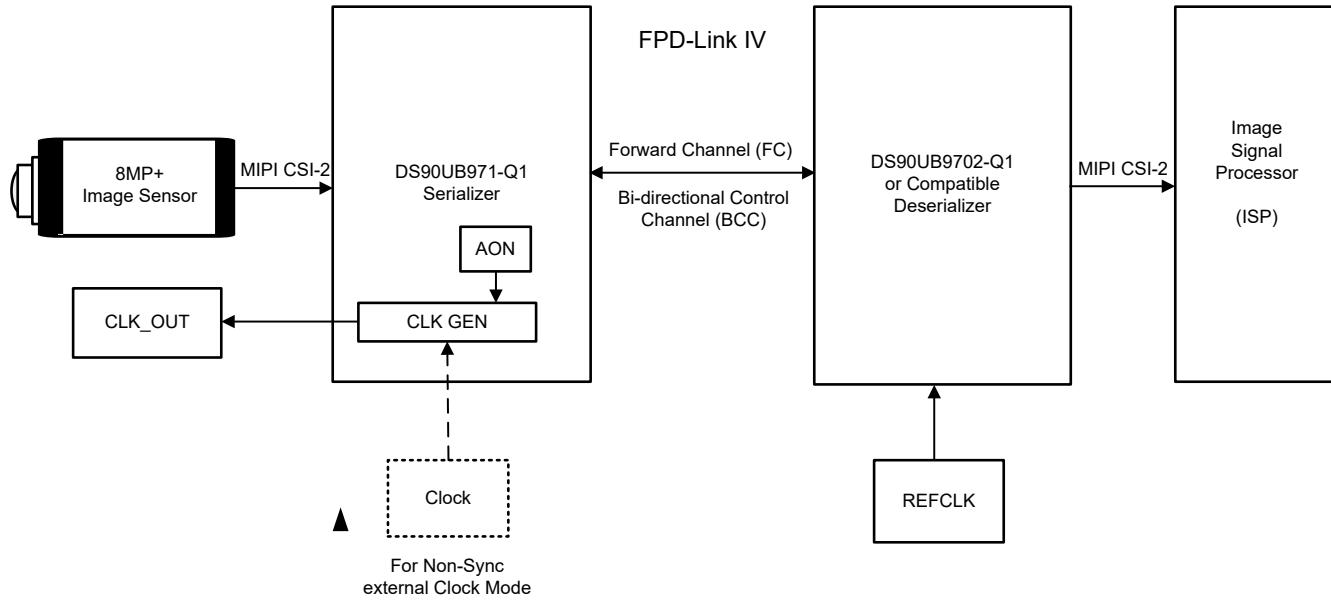
$$\text{Synchronous FPD-Link IV BC Data Rate} = \text{FC Data Rate} / 160 \quad (4)$$

$$\text{Non Synchronous FPD-Link IV BC Data Rate} = \text{FC Data Rate} / 800 \quad (5)$$

$$\text{Synchronous FPD-Link III FC Data Rate} = \text{Deserializer REFCLK} * 160 \quad (6)$$

$$\text{Synchronous FPD-Link III BC Data Rate} = \text{FC Data Rate} / 80 \quad (7)$$

$$\text{Non-Synchronous FPD-Link III BC Data Rate} = \text{FC Data Rate} / 400 \quad (8)$$



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**Figure 7-9. Clocking System Diagram**

#### 7.4.1.1 Synchronous Clocking Mode

Operation in the synchronous mode offers the advantage that in a multi-sensor system, all of the sensors and the receiver are locked to a common clock in the same clock domain, which reduces or eliminates the need for data buffering and re-synchronization. The synchronous clocking mode also eliminates the cost, space, and potential failure point of a reference oscillator within the sensor module.

In this mode, a clock is passed from the deserializer to the serializer via the FPD-Link IV back channel and the serializer is able to use this clock both as a reference clock for an attached image sensor, and as a reference clock for the link back (FPD-Link IV forward channel) to the deserializer. For operation in this mode, the DS90UB971-Q1 must be paired with a deserializer that can support this feature such as the DS90UB97x-Q1, DS90UB960-Q1, DS90UB962-Q1, DS90UB954-Q1, and DS90UB936-Q1 .

When pairing with an FPD-Link III deserializer, although the deserializer may support a reference clock source frequency from 23 - 26 MHz, the DS90UB971-Q1 cannot support a back channel lower than 47.1875 Mbps. Because of this, when pairing an FPD-Link III deserializer, the reference clock source frequency range on the deserializer is 23.59375 MHz - 26 MHz.

#### 7.4.1.2 Non-Synchronous CLK\_IN Clocking Mode

In the Non-Synchronous CLK\_IN mode, the reference clock is supplied to the serializer, and it uses this clock to derive the FPD-Link IV forward channel and a reference clock for an attached image sensor.

#### 7.4.1.3 Non-Synchronous Internal Clocking Mode

The DS90UB971-Q1 has an internal generated clock source which is intended for use primarily when the backchannel reference clock or other CLK\_IN reference clock is not available to the device. The internally generated clocking mode is only intended to function when pairing with an FPD-Link III Deserializer.

When the device is operating in non-synchronous mode and loss of CLKIN occurs, the internal oscillator will be used as the reference clock. The clock operation mode will maintain the forward channel, back channel, and LOCK/PASS condition when paired with an FPD-Link IV Deserializer.

#### 7.4.1.4 Configuring CLK\_OUT

When using the DS90UB971-Q1 in either Synchronous or Non-Synchronous CLK\_IN clocking modes, the CLK\_OUT is intended as a reference clock for the image sensor. The frequency of CLK\_OUT is set by [Equation 9](#):

$$\text{CLK\_OUT} = \text{FC} * \text{M} / (8 * \text{N}) \quad (9)$$

where

- FC is the forward channel data rate in Gbps when operating in FPD-Link IV mode and forward channel data rate \* 2 in Gbps when operating in FPD-Link III mode.
- M and N are parameters set by registers 0x06 and 0x07 when operating in Synchronous mode and Non-Synchronous CLK\_IN mode.

The PLL that generates CLK\_OUT is a digital PLL, and as such, has very low jitter if the ratio N/M is an integer.

#### Example CLK\_OUT Configuration

Assume a forward channel data rate of 7.55Gbps is being used and an imager requires a PCLK of 25MHz. [Equation 9](#) becomes:  $25\text{MHz} = 7.55\text{Gbps} * \text{M} / (8 * \text{N})$ . One solution could be M = 4 and N = 151, this yields a CLK\_OUT of exactly 25MHz but N/M is not an integer and therefore will have increased jitter. Another solution could be M = 4 and N = 152, this way N/M is an integer value and CLK\_OUT is 24.8MHz.

```
# Example of Setting CLK_OUT
WriteI2C(0x06, 0xE4) # Set M equal to 4
WriteI2C(0x07, 0x98) # Set N equal to 152
```

The DS90UB971-Q1 has ability to provide CLK\_OUT from 2 different clock input sources, HSPLL\_VCO and OSCCLK, where HSPLL\_VCO is the default path. If the OSCCLK path is enabled upon losing HSPLL\_LOCK in register 0xD8[6], the OSCCLK path input source is routed to CLK\_OUT. When HSPLL\_LOCK is restored, the path is re-routed back to the HSPLL\_VCO clock source. The CLK\_OUT signal will be disabled for 3-4 CLK\_OUT clock cycles when switching from one clock source to the other.

$$\text{CLK\_OUT} = \text{OSCCLK} * \text{M}_{\text{ALT}} / \text{N}_{\text{ALT}} \quad (10)$$

- OSCCLK is an internal oscillator with a frequency of 800MHz  $\pm 10\%$ .
- $\text{M}_{\text{ALT}}$  and  $\text{N}_{\text{ALT}}$  are parameters set in registers bits 0xD8[4:0] and 0xD9[7:0] respectively.

If 0xD8[6] is not enabled, then CLK\_OUT is not present when link detect is not present or when operating in non-synchronous mode and the CLKIN signal is temporarily lost and the device is waiting for HSPLL to re-lock. OSCCLK may be chosen as the main path by setting 0xD8[7] = 1, in which case CLK\_OUT will always be present.

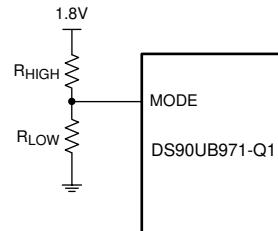
To disable the CLK\_OUT feature, set 0x1F [1] = 0.

#### 7.4.2 MODE

The DS90UB971-Q1 can operate in one of 6 different modes. The default mode is selected by the bias voltage applied to the MODE pin during power up. To set this voltage, a potential divider between VDDPLL and GND is used to apply the appropriate bias. This potential divider should be referenced to the potential on the VDDD pin. After power up, the MODE can be read or changed through register access.

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**Figure 7-10. MODE Configuration****Table 7-13. Strap Configuration Mode Select**

MODE SELECT		V <sub>TARGET</sub> VOLTAGE RANGE			V <sub>TARGET</sub> STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)	
MODE	NAME	RATIO MIN	RATIO TYP	RATIO MAX	V <sub>(VDD) = 1.8 V</sub>	R <sub>HIGH</sub> (kΩ)	R <sub>LOW</sub> (kΩ)
0	Synchronous FPD-Link IV	0.000	0.000	0.135	0	OPEN	10
1	Synchronous FPD-Link III 50 Mbps BC Rate	0.176	0.213	0.244	.384	42.2	11.5
3	Non-Synchronous FPD-Link III Internal Clock 4.0 Gbps FC Rate	0.407	0.441	0.472	0.793	28.7	22.6
4	Non-Synchronous FPD-Link III 26 MHz CLKIN 4.16 Gbps FC Rate	0.526	0.555	0.590	0.999	15	18.7
5	Non-Synchronous FPD-Link IV 25 MHz CLKIN 7.55 Gbps FC Rate	0.640	0.667	0.708	1.2	10.0	20.0
7	Synchronous FPD-Link III 25 Mbps BC Half-Rate	0.877	0.889	1.000	1.6	10	OPEN

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C Interface Configuration

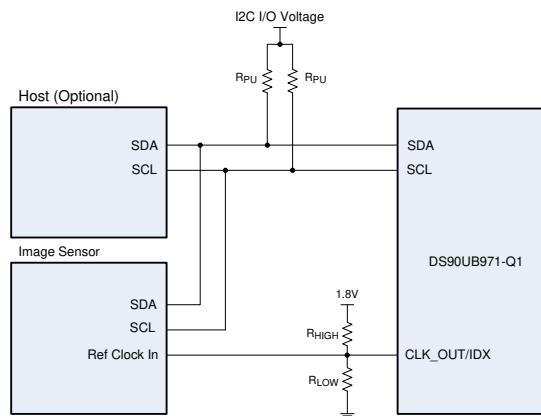
This serializer may be configured by the use of a I<sup>2</sup>C-compatible serial control bus. Multiple devices may share the serial control bus (up to 2 device addresses supported). The device address is set through a resistor divider (R1 and R2 – see [Figure 7-11](#)) connected to the IDX pin.

#### 7.5.1.1 IDX

The IDX pin configures the control interface to one of 2 possible device addresses, either 1.8-V or 3.3-V referenced I<sup>2</sup>C. A pullup resistor and a pulldown resistor must be used to set the appropriate voltage on the IDX input pin (See [Figure 7-11](#)). The IDX resistor divider must to be referred to Pin 25 (after the Ferrite Filter on the DS90UB971-Q1 pin side).

**Table 7-14. IDX Configuration Setting**

IDX	V <sub>TARGET</sub> VOLTAGE RANGE			V <sub>IDX</sub> TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		I2C 8-BIT ADDRESS	I2C 7-BIT ADDRESS	I2C I/O VOLTAGE	
	RATIO MIN	RATIO TYP	RATIO MAX		V <sub>VDD</sub> = 1.8 V	R <sub>HIGH</sub> (kΩ)	R <sub>LOW</sub> (kΩ)			
1	0.000	0.000	0.135 x V <sub>(VDD18)</sub>	0.000	Open	42.2		0x30	0x18	1.8 V
2	0.176 x V <sub>(VDD18)</sub>	0.213 x V <sub>(VDD18)</sub>	0.247 x V <sub>(VDD18)</sub>	0.384	180	47.5		0x32	0x19	1.8 V
3	0.526 x V <sub>(VDD18)</sub>	0.551 x V <sub>(VDD18)</sub>	0.584 x V <sub>(VDD18)</sub>	.999	82.5	102		0x30	0x18	3.3 V
4	0.640 x V <sub>(VDD18)</sub>	0.671 x V <sub>(VDD18)</sub>	0.701 x V <sub>(VDD18)</sub>	1.208	68.1	137		0x32	0x19	3.3 V



**Figure 7-11. Circuit to Bias IDX Pin**

#### 7.5.1.2 CLK\_OUT/IDX

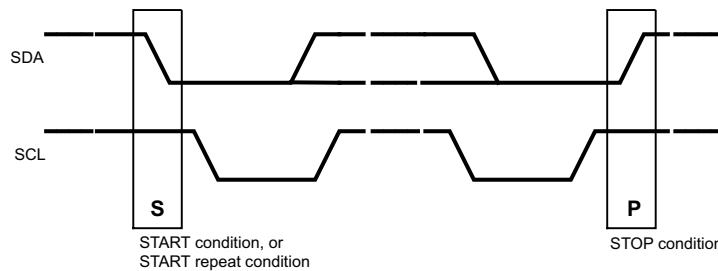
The CLK\_OUT/IDX pin serves two functions. At power up, the voltage on the IDX pin is compared to VDD and the ratio sets various parameters for configuration of the DS90UB971-Q1. Once the DS90UB971 has been configured, the CLK\_OUT/IDX pin switches over to a clock source, intended to provide a reference clock to the image sensor. The voltage divider used to select the IDX value should have a combined impedance of >35kΩ as to not interfere with the CLK\_OUT signal. It is important to account for any additional leakage current from an attached image sensor's clock input pin that may affect the voltage seen on the IDX pin at start up.

### 7.5.2 I<sup>2</sup>C Interface Operation

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input / Output signal and the SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to 1.8-V or 3.3-V.

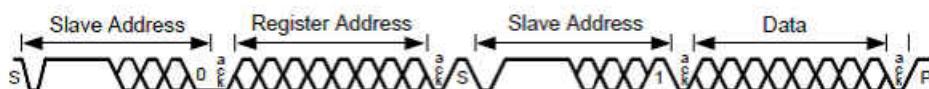
For the standard and fast I<sup>2</sup>C modes, a pullup resistor  $R_{PU} = 2.2\text{-k}\Omega$  is recommended, while a pullup resistor  $R_{PU} = 470\text{-}\Omega$  is recommended for the fast plus mode. However, the pullup resistor value may be additionally adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low. The IDX pin configures the control interface to one of 2 possible device addresses. A pullup resistor,  $R_{PU}$  and a pulldown resistor,  $R_{LOW}$  may be used to set the appropriate voltage on the IDX input pin. See [I<sup>2</sup>C Bus Pullup Resistor Calculation \(SLVA689\)](#) for more details.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See [Figure 7-12](#).

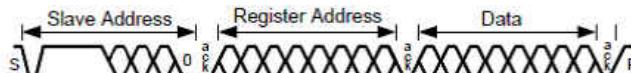


**Figure 7-12. Start and Stop Conditions**

To communicate with an I<sup>2</sup>C slave, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in [Figure 7-13](#) and a WRITE is shown in [Figure 7-14](#).



**Figure 7-13. I<sup>2</sup>C Bus Read**



**Figure 7-14. I<sup>2</sup>C Bus Write**

Any I<sup>2</sup>C Master located at the serializer must support I<sup>2</sup>C clock stretching. For more information on I<sup>2</sup>C interface requirements and throughput considerations, refer to TI Application Note [I<sup>2</sup>C Communication Over FPD-Link III with Bidirectional Control Channel \(SNLA131\)](#).

### 7.5.3 I<sup>2</sup>C Timing

The proxy master timing parameters are based on the internal reference clock with accuracy of 26.25 MHz  $\pm 10\%$ . The I<sup>2</sup>C Master regenerates the I<sup>2</sup>C read or write access using timing controls in the registers 0x0B and 0x0C to regenerate the clock and data signals to meet the desired I<sup>2</sup>C timing in standard, fast, or fast-plus modes of operation.

I<sup>2</sup>C Master SCL High Time is set in register 0x0B. This field configures the high pulse width of the SCL output when the serializer is the master on the local I<sup>2</sup>C bus. The default value is set to provide a minimum 5  $\mu\text{s}$  SCL high time with the internal reference clock at 26.2 MHz  $\pm 10\%$  including five additional oscillator clock periods or

synchronization and response time. Units are 38.1 ns for the nominal oscillator clock frequency, giving  $\text{Min\_delay} = 38.1 \text{ ns} \times (\text{SCL\_HIGH\_TIME} + 5)$ .

I<sup>2</sup>C Master SCL Low Time is set in register 0x0C. This field configures the low pulse width of the SCL output when the serializer is the master on the local deserializer I<sup>2</sup>C bus. This value is also used as the SDA setup time by the I<sup>2</sup>C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. The default value is set to provide a minimum 5- $\mu$ s SCL high time with the reference clock at 26.25 MHz  $\pm 10\%$  including five additional oscillator clock periods or synchronization and response time. Units are 38.1 ns for the nominal oscillator clock frequency, giving  $\text{Min\_delay} = 38.1 \text{ ns} \times (\text{SCL\_HIGH\_TIME} + 5)$ . See [Table 7-15](#) example settings for Standard mode, Fast mode, and Fast Mode Plus timing.

**Table 7-15. Typical I<sup>2</sup>C Timing Register Settings**

I <sup>2</sup> C MODE	SCL HIGH TIME		SCL LOW TIME	
	0x0B	NOMINAL DELAY	0x0C	NOMINAL DELAY
Standard	0x7F	5.03 $\mu$ s	0x7F	5.03 $\mu$ s
Fast	0x13	0.914 $\mu$ s	0x26	1.64 $\mu$ s
Fast - Plus	0x06	0.419 $\mu$ s	0x0B	0.648 $\mu$ s

### 7.5.4 I<sup>2</sup>C Watchdog Timer

The I<sup>2</sup>C controller includes a watchdog timer to prevent system lockup or any unexpected behavior. Watchdog timers will detect I<sup>2</sup>C bus at the local and remote I<sup>2</sup>C interface. Two timeout values in the range of 50us and the 1sec value can be register selected.

## 7.6 Pattern Generation

The DS90UB971-Q1 supports an internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns and accessed by the Pattern Generator page 0 in the indirect register set. See [Section 7.7](#) for more information on internal registers.

[Analog LaunchPAD](#) makes it easy to configure the registers of the DS90UB971-Q1 for use with the PATGEN utility.

### 7.6.1 Reference Color Bar Pattern

The Reference Color Bar Patterns are based on the pattern defined in Appendix D of the `mipi_CTS_for_D-PHY_v1-1_r03` specification. The pattern is an 8 color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 Reference pattern provides 8 color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted), X bytes of 0x33 (mid-frequency pattern), X bytes of 0xF0 (low-frequency pattern, inverted), X bytes of 0x7F (lone 0 pattern), X bytes of 0x55 (high-frequency pattern), X bytes of 0xCC (mid-frequency pattern, inverted), X bytes of 0x0F (low-frequency pattern), and Y bytes of 0x80 (long 1 pattern). In most cases, Y will be the same as X. For certain data types, the last color bar may need to be larger than the others to properly fill the video line dimensions.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 Data Type field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

The pattern generator relies on proper programming by software to ensure the color bar widths are set to multiples of the block (or word) size required for the specified DataType. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The Pattern Generator is implemented in the CSI-2 Transmit clock domain, providing the pattern directly to the CSI-2 Transmitter. The circuit generates the CSI-2 formatted data.

### 7.6.2 Fixed Color Patterns

When programmed for Fixed Color Pattern mode, Pattern Generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the Color Bar Patterns. When sending Fixed Color Patterns, the color bar controls allow alternating between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The Fixed Color patterns assume a fixed block size for the byte pattern to be sent. The block size is programmable through register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size should be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern would consist of 3-byte pixels and therefore require a 3-byte block size. A 2x12-bit pixel image would also require 3-byte block size, while a 3x12-bit pixel image would require 9 bytes (2 pixels) in order to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size for 4 pixels, so 1x10-bit and 2x10-bit could both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size would be required.

The Fixed Color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image could alternate between four different pixels by using a twelve-byte block size. An alternating black and white RGB888 image could be sent with a block size of 6-bytes and setting first three bytes to 0xFF and next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte.

### 7.6.3 Packet Generator Programming

The information in this section provides details on how to program the Pattern Generator to provide a specific color bar pattern, based on datatype, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements should include the datatype, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

FPD-Link provides a PATGEN tab through the Analog Launch Pad GUI which can be used to generate the pattern generator configuration easily.

- PGEN\_ACT\_LPF – Number of active lines per frame
- PGEN\_TOT\_LPF – Number of total lines per frame
- PGEN\_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes
- CSI-2 DataType field and VC-ID.
- Optional: PGEN\_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid.
- Optional: PGEN\_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid.
- PGEN\_LINE\_PD – Line period which controls the Frame Rate. Compute based on Frame Rate and total lines per frame based on the equation below. Round to the nearest integer.

PGEN Line Period = 1 / (frame rate \* PGEN\_TOT\_LPF) \* Forward Channel Rate (Gbps)/40

- PGEN\_BAR\_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below).

#### 7.6.3.1 Determining Color Bar Size

The color bar pattern should be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the Mipi CSI-2 specification. For example, RGB888 requires a 3-byte

block size which is the same as the pixel size. RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software should compute the required bar size in bytes based on the line size and the number of bars. For the standard 8 color bar pattern, that would require the following algorithm:

- Select the desired datatype, and a valid length for that datatype (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the datatype specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar
- Round result down to the nearest integer
- Convert blocks/bar to bytes/bar and program that value into the PGEN\_BAR\_SIZE register

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and divide by bytes/block

### 7.6.4 Code Example for Pattern Generator

```
#Patgen Fixed Colorbar 1280x720p30
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24)
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x0F)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xE0)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x1A)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0C)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x67)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
```

## 7.7 Register Maps

In the register definitions under the *DEFAULT* heading, the following definitions apply:

- RW = Read Write access
- RO = Read Only access
- SC = Register sets on event occurrence and Self-Clears when event ends
- RW/SC = Read Write access, Self-Clearing bit
- COR = Clear on Read
- RO/COR = Read Only, Clear on Read
- RO/COR = Read Only, Clear on Read
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- LH = Latched High and held until read, based upon the occurrence of the corresponding event
- S = Set based on condition of pin at power up

### 7.7.1 Main Registers

**MAIN Registers** lists the memory-mapped registers for the Main registers. All register offset addresses not listed in **MAIN Registers** should be considered as reserved locations and the register contents should not be modified.

**Table 7-16. MAIN Registers**

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG	GENERAL_CFG	Go
0x3	MODE_SEL	MODE_SEL	Go
0x6	CLKOUT_CTRL0	CLKOUT_CTRL0	Go
0x7	CLKOUT_CTRL1	CLKOUT_CTRL1	Go
0x8	BCC_WATCHDOG	BCC_WATCHDOG	Go
0x9	I2C_CONTROL1	I2C_CONTROL1	Go
0xA	I2C_CONTROL2	I2C_CONTROL2	Go
0xB	SCL_HIGH_TIME	SCL_HIGH_TIME	Go
0xC	SCL_LOW_TIME	SCL_LOW_TIME	Go
0xD	LOCAL_GPIO_DATA	LOCAL_GPIO_DATA	Go
0xE	GPIO_INPUT_CTL	GPIO_INPUT_CTL	Go
0xF	GPIO_ATP_CTL	GPIO_ATP_CTL	Go
0x11	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x17	SAR_ADC_CNTR	SAR_ADC_CNTR	Go
0x18	SAR_ADC_DOUT	SAR_ADC_DOUT	Go
0x1B	LOCAL_DEV_ICR	LOCAL_DEV_ICR	Go
0x1C	ALARM_CSI_EN	ALARM_CSI_EN	Go
0x1E	ALARM_BC_EN	ALARM_BC_EN	Go
0x20	CSI_POL_SEL	CSI_POL_SEL	Go
0x21	CSI_LP_POLARITY	CSI_LP_POLARITY	Go
0x30	CSI_PKT_VCI_CTRL	CSI_PKT_VCI_CTRL	Go
0x31	CSI_PKT_HDR_TINIT_CTRL	CSI_PKT_HDR_TINIT_CTRL	Go
0x32	BCC_CONFIG	BCC_CONFIG	Go
0x33	DATAPATH_CTL1	DATAPATH_CTL1	Go
0x35	REMOTE_PAR_CAP1	REMOTE_PAR_CAP1	Go
0x37	DES_ID	DES_ID	Go
0x39	SLAVE_ID_0	SLAVE_ID_0	Go
0x3A	SLAVE_ID_1	SLAVE_ID_1	Go

**Table 7-16. MAIN Registers (continued)**

Address	Acronym	Register Name	Section
0x3B	SLAVE_ID_2	SLAVE_ID_2	Go
0x3C	SLAVE_ID_3	SLAVE_ID_3	Go
0x3D	SLAVE_ID_4	SLAVE_ID_4	Go
0x3E	SLAVE_ID_5	SLAVE_ID_5	Go
0x3F	SLAVE_ID_6	SLAVE_ID_6	Go
0x40	SLAVE_ID_7	SLAVE_ID_7	Go
0x41	SLAVE_ID_ALIAS_0	SLAVE_ID_ALIAS_0	Go
0x42	SLAVE_ID_ALIAS_1	SLAVE_ID_ALIAS_1	Go
0x43	SLAVE_ID_ALIAS_2	SLAVE_ID_ALIAS_2	Go
0x44	SLAVE_ID_ALIAS_3	SLAVE_ID_ALIAS_3	Go
0x45	SLAVE_ID_ALIAS_4	SLAVE_ID_ALIAS_4	Go
0x46	SLAVE_ID_ALIAS_5	SLAVE_ID_ALIAS_5	Go
0x47	SLAVE_ID_ALIAS_6	SLAVE_ID_ALIAS_6	Go
0x48	SLAVE_ID_ALIAS_7	SLAVE_ID_ALIAS_7	Go
0x49	BC_CTRL	BC_CTRL	Go
0x50	REV_MASK_ID	REV_MASK_ID	Go
0x51	DEVICE_STS	DEVICE_STS	Go
0x52	GENERAL_STATUS	GENERAL_STATUS	Go
0x53	GPIO_PIN_STS	GPIO_PIN_STS	Go
0x54	BIST_ERR_CNT	BIST_ERR_CNT	Go
0x55	CRC_ERR_CNT1	CRC_ERR_CNT1	Go
0x56	CRC_ERR_CNT2	CRC_ERR_CNT2	Go
0x57	INTERRUPT_STS	INTERRUPT_STS	Go
0x58	LOCAL_DEV_ISR	LOCAL_DEV_ISR	Go
0x5C	CSI_ERR_CNT	CSI_ERR_CNT	Go
0x5D	CSI_ERR_STATUS	CSI_ERR_STATUS	Go
0x5E	CSI_ERR_DLANE01	CSI_ERR_DLANE01	Go
0x5F	CSI_ERR_DLANE23	CSI_ERR_DLANE23	Go
0x60	CSI_ERR_CLK_LANE	CSI_ERR_CLK_LANE	Go
0x61	CSI_PKT_HDR_VC_ID	CSI_PKT_HDR_VC_ID	Go
0x62	PKT_HDR_WC_LSB	PKT_HDR_WC_LSB	Go
0x63	PKT_HDR_WC_MSB	PKT_HDR_WC_MSB	Go
0x64	CSI_ECC	CSI_ECC	Go
0xB0	IND_ACC_CTL	IND_ACC_CTL	Go
0xB1	ANA_IA_ADDR	ANA_IA_ADDR	Go
0xB2	ANA_IA_DATA	ANA_IA_DATA	Go
0xD8	DIV_OSC_SEL0	DIV_OSC_SEL0	Go
0xD9	DIV_OSC_SEL1	DIV_OSC_SEL1	Go
0xF0	FPD3_RX_ID0	FPD3_RX_ID0	Go
0xF1	FPD3_RX_ID1	FPD3_RX_ID1	Go
0xF2	FPD3_RX_ID2	FPD3_RX_ID2	Go
0xF3	FPD3_RX_ID3	FPD3_RX_ID3	Go
0xF4	FPD3_RX_ID4	FPD3_RX_ID4	Go
0xF5	FPD3_RX_ID5	FPD3_RX_ID5	Go

**7.7.1.1 I2C\_DEVICE\_ID Register (Address = 0x0) [Default = 0x30]**

I2C\_DEVICE\_ID is shown in [I2C\\_DEVICE\\_ID Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-17. I2C\_DEVICE\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	DEVICE_ID	R/W	0x18	7-bit I2C ID of Serializer. This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID.
0	SER_ID_OVERRIDE	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

**7.7.1.2 RESET\_CTL Register (Address = 0x1) [Default = 0x00]**

RESET\_CTL is shown in [RESET\\_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-18. RESET\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-3	RESERVED	R/W	0x0	Reserved
2	RESTART_AUTOLOAD	RH/W1S	0x0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing.
1	DIGITAL_RESET1	RH/W1S	0x0	Digital Reset1 Resets the entire digital block including registers. This bit is self-clearing. 0: Normal operation 1: Reset
0	DIGITAL_RESET0	RH/W1S	0x0	Digital Reset0 Resets the entire digital block except registers. This bit is self-clearing. 0: Normal operation 1: Reset

**7.7.1.3 GENERAL\_CFG Register (Address = 0x2) [Default = 0x32]**

GENERAL\_CFG is shown in [GENERAL\\_CFG Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-19. GENERAL\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	CONTS_CLK	R/W	0x0	CSI Clock Lane Configuration 0: Non Continuous Clock 1: Continuous Clock
5-4	CSI_LANE_SEL	R/W	0x3	CSI Data lane configuration 00: 1-lane configuration 01: 2-lane configuration 11: 4 lane configuration
3-2	RESERVED	R	0x0	Reserved
1	CRC_TX_GEN_EN	R/W	0x1	Transmitter CRC Generator 0: Disable 1: Enable

**Table 7-19. GENERAL\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	RESERVED	R/W	0x0	Reserved

**7.7.1.4 MODE\_SEL Register (Address = 0x3) [Default = 0x00]**MODE\_SEL is shown in [MODE\\_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-20. MODE\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	MODE_OV	R/W	0x0	0: Serializer Mode from the strapped MODE pin 1: Register Mode overrides strapped value
3	MODE_DONE	R	0x0	Indicates MODE value has stabilized and been latched
2-0	MODE_VAL	R/W	0x0	This field always indicates the MODE setting of the device. When bit 4 of this register is 0, this field is read-only and shows the Mode Setting. When bit 4 of this register is 1, this field is read/write and can be used to assign MODE. Mode of operation 000: Synchronous Mode FPD4 001: Synchronous Mode FPD3 011: Non-synch Mode, Internal Clock, FPD3 100: Non-synch Mode, External Clock, FPD3 101: Non-synch Mode, External Clock FPD4 111: Synchronous Mode FPD3, BC Half-Rate

**7.7.1.5 CLKOUT\_CTRL0 Register (Address = 0x6) [Default = 0x01]**CLKOUT\_CTRL0 is shown in [CLKOUT\\_CTRL0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-21. CLKOUT\_CTRL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R/W	0x0	Reserved
4-0	DIV_M_VAL	R/W	0x1	M Value for M/N divider for CLKOUT. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed using M/N ratio of internal VCO clock to generate clock based on system camera requirement. Internal VCO clock for the M/N divider is derived by forward channel data rate div by HSPLL_VCOCLK_DIV. When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100MHz. M Value should be >=1. If set to 0 then device will internally set it to 1.

**7.7.1.6 CLKOUT\_CTRL1 Register (Address = 0x7) [Default = 0x28]**CLKOUT\_CTRL1 is shown in [CLKOUT\\_CTRL1 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-22. CLKOUT\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	DIV_N_VAL	R/W	0x28	N Value for M/N divider for CLKOUT. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed by M/N ratio of internal VCO clock to generate clock based on system camera requirement. Internal VCO clock for the M/N divider is derived by forward channel data rate div by HSPLL_VCOCLK_DIV .When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100MHz.

**7.7.1.7 BCC\_WATCHDOG Register (Address = 0x8) [Default = 0xFE]**BCC\_WATCHDOG is shown in [BCC\\_WATCHDOG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-23. BCC\_WATCHDOG Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	BCC_WD_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WD_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

**7.7.1.8 I2C\_CONTROL1 Register (Address = 0x9) [Default = 0x1E]**I2C\_CONTROL1 is shown in [I2C\\_CONTROL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-24. I2C\_CONTROL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LCL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the DeSerializer. Setting this bit does not affect remote access to I2C slaves at the Serializer.
6-4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3-0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

**7.7.1.9 I2C\_CONTROL2 Register (Address = 0xA) [Default = 0x11]**I2C\_CONTROL2 is shown in [I2C\\_CONTROL2 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-25. I2C\_CONTROL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	SDA_OUTPUT_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3-2	SDA_OUTPUT_DELAY	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEED_UP	R/W	0x0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISABLE	R/W	0x1	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

**7.7.1.10 SCL\_HIGH\_TIME Register (Address = 0xB) [Default = 0x7F]**SCL\_HIGH\_TIME is shown in [SCL\\_HIGH\\_TIME Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-26. SCL\_HIGH\_TIME Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SCL_HIGH_TIME_VAL	R/W	0x7F	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay= 38.0952ns * (TX_SCL_HIGH + 5)

**7.7.1.11 SCL\_LOW\_TIME Register (Address = 0xC) [Default = 0x7F]**SCL\_LOW\_TIME is shown in [SCL\\_LOW\\_TIME Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-27. SCL\_LOW\_TIME Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SCL_LOW_TIME_VAL	R/W	0x7F	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay= 38.0952ns * (TX_SCL_LOW + 5)

**7.7.1.12 LOCAL\_GPIO\_DATA Register (Address = 0xD) [Default = 0xF0]**LOCAL\_GPIO\_DATA is shown in [LOCAL\\_GPIO\\_DATA Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-28. LOCAL\_GPIO\_DATA Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	GPIO_RMTEN	R/W	0xF	Enable remote deserializer GPIO data on local GPIO
3-0	GPIO_OUT_SRC	R/W	0x0	GPIO Output Source This register will set the logical output of 4 GPIOs, GPIO_RMTEN must be disabled and GPIOx_OUT_EN must be enabled. Bit 3 write 0/1 on GPIO3 Bit 2 write 0/1 on GPIO2 Bit 1 write 0/1 on GPIO1 Bit 0 write 0/1 on GPIO0.

**7.7.1.13 GPIO\_INPUT\_CTL Register (Address = 0xE) [Default = 0x0F]**GPIO\_INPUT\_CTL is shown in [GPIO\\_INPUT\\_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-29. GPIO\_INPUT\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable 0: Disabled 1: Enabled
6	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable 0: Disabled 1: Enabled
5	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable 0: Disabled 1: Enabled
4	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled

**Table 7-29. GPIO\_INPUT\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

**7.7.1.14 GPIO\_ATP\_CTL Register (Address = 0xF) [Default = 0x00]**GPIO\_ATP\_CTL is shown in [GPIO\\_ATP\\_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-30. GPIO\_ATP\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO3_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
6	GPIO2_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
5	GPIO1_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
4	GPIO0_PD_DIS	R/W	0x0	1: Disable GPIO internal pull-down resistor 0: Enable GPIO internal pull-down resistor
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

**7.7.1.15 INTERRUPT\_CTL Register (Address = 0x11) [Default = 0x00]**INTERRUPT\_CTL is shown in [INTERRUPT\\_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-31. INTERRUPT\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	INTERRUPT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller
6	IE_DEV	R/W	0x0	Local Device Interrupt. Enable interrupts for general device functions such as TEMP sensor, Voltage sensor, line fault, etc. See the LOCAL_DEV_ICR register for the functions that can generate the local device interrupts
5-0	RESERVED	R	0x0	Reserved

**7.7.1.16 SAR\_ADC\_CNTR Register (Address = 0x17) [Default = 0xF1]**SAR\_ADC\_CNTR is shown in [SAR\\_ADC\\_CNTR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-32. SAR\_ADC\_CNTR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	SENSE_T_EN	R/W	0x1	Enable Temp Sensor
4	SENSE_GAIN_EN	R/W	0x1	Enable Gain stage of the Temp Sensor

**Table 7-32. SAR\_ADC\_CNTR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3-2	RESERVED	R	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	SAR_ADC_BYPASS_RE_G_LV	R/W	0x1	Bypass SAR ADC voltage regulator

**7.7.1.17 SAR\_ADC\_DOUT Register (Address = 0x18) [Default = 0x00]**SAR\_ADC\_DOUT is shown in [SAR\\_ADC\\_DOUT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-33. SAR\_ADC\_DOUT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SAR_ADC_DOUT_LV	R	0x0	ADC output=> Configurable for Line-Fault, or temp-sensor

**7.7.1.18 LOCAL\_DEV\_ICR Register (Address = 0x1B) [Default = 0x00]**LOCAL\_DEV\_ICR is shown in [LOCAL\\_DEV\\_ICR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-34. LOCAL\_DEV\_ICR Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	IE_ESD_EVENT_INTR	R/W	0x0	Interrupt on ESD event.
3	IE_LOSS_OF_CLKIN	R/W	0x0	Interrupt on loss of CLK_IN, when using external clock mode.
2	IE_TEMP_SENSOR	R/W	0x0	Interrupt on Temp Sensor. When enabled, an interrupt will be generated from the temperature sensor. Temp Sensor interrupts are controlled by registers 0x23 and 0x25 on sar adc page (page 4)
1	IE_VOLT_SENSOR	R/W	0x0	Interrupt on Voltage Sensor. When enabled, an interrupt will be generated from the voltage sensor. Voltage Sensor interrupts are controlled by registers 0x23-0x26 on sar adc page (page 4)
0	IE_LINE_FAULT	R/W	0x0	Interrupt on Line Fault. When enabled, an interrupt will be generated from the line fault detection circuit. Line Fault interrupts are controlled by registers 0x27-0x28 on sar adc page (page 4)

**7.7.1.19 ALARM\_CSI\_EN Register (Address = 0x1C) [Default = 0x00]**ALARM\_CSI\_EN is shown in [ALARM\\_CSI\\_EN Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-35. ALARM\_CSI\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5	CSI_NO_FV_EN	R/W	0x0	Enable CSI No Frame Valid alarm
4	DPHY_SYNC_ERR_EN	R/W	0x0	Enable DPHY_SYNC_ERR alarm
3	DPHY_CTRL_ERR_EN	R/W	0x0	Enable DPHY_CTRL_ERR alarm
2	CSI_ECC_2_EN	R/W	0x0	Enable CSI_ECC2 alarm
1	CSI_CHKSUM_ERR_EN	R/W	0x0	Enable CSI checksum error alarm
0	CSI_LENGTH_ERR_EN	R/W	0x0	Enable CSI length error alarm

**7.7.1.20 ALARM\_BC\_EN Register (Address = 0x1E) [Default = 0x00]**

ALARM\_BC\_EN is shown in [ALARM\\_BC\\_EN Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-36. ALARM\_BC\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

**7.7.1.21 CSI\_POL\_SEL Register (Address = 0x20) [Default = 0x00]**

CSI\_POL\_SEL is shown in [CSI\\_POL\\_SEL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-37. CSI\_POL\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	POLARITY_CLK0	R/W	0x0	CSI2 CLK lane Polarity. 1= polarity inverted 0= polarity default
3	POLARITY_D3	R/W	0x0	CSI2 Data lane 3 Polarity 1= polarity inverted 0= polarity default
2	POLARITY_D2	R/W	0x0	CSI2 Data lane 2 Polarity 1= polarity inverted 0= polarity default
1	POLARITY_D1	R/W	0x0	CSI2 Data lane 1 Polarity 1= polarity inverted 0= polarity default
0	POLARITY_D0	R/W	0x0	CSI2 Data lane 0 Polarity 1= polarity inverted 0= polarity default

**7.7.1.22 CSI\_LP\_POLARITY Register (Address = 0x21) [Default = 0x80]**

CSI\_LP\_POLARITY is shown in [CSI\\_LP\\_POLARITY Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-38. CSI\_LP\_POLARITY Register Field Descriptions**

Bit	Field	Type	Default	Description
7	SUPPORT_16VC	R/W	0x1	1 indicates 16VC support, 0 indicates 4VC support.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

**Table 7-38. CSI\_LP\_POLARITY Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	POL_LP_CLK0	R/W	0x0	LP CSI Clock lane Polarity 1= polarity inverted 0= polarity default
3-0	POL_LP_DATA	R/W	0x0	LP CSI Data lane Polarity, bit[3] is for data lane 3, ..., bit[0] is for data lane 0 1= polarity inverted 0= polarity default

**7.7.1.23 CSI\_PKT\_VCI\_CTRL Register (Address = 0x30) [Default = 0x40]**CSI\_PKT\_VCI\_CTRL is shown in [CSI\\_PKT\\_VCI\\_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-39. CSI\_PKT\_VCI\_CTRL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x1	Reserved
5	PKT_HDR_VCI_ENABLE	R/W	0x0	Enable the CSI packet header selection based on VC for interleaved mode. For interleaved VC packet set this bit to record the packet headers for each VC. For regular data packet ignore this bit.
4-0	RESERVED	R/W	0x0	Reserved

**7.7.1.24 CSI\_PKT\_HDR\_TINIT\_CTRL Register (Address = 0x31) [Default = 0x00]**CSI\_PKT\_HDR\_TINIT\_CTRL is shown in [CSI\\_PKT\\_HDR\\_TINIT\\_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-40. CSI\_PKT\_HDR\_TINIT\_CTRL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	PKT_HDR_SEL_VC	R/W	0x0	For interleaved VC packet select the VC ID to display the packet header. This is effective only if reg0x30[5] is set high (PKT_HDR_VCI_ENABLE)
3	RESERVED	R/W	0x0	Reserved
2-0	TINIT_TIME	R/W	0x0	CSI2 Initial Time after power up. Any LP control data are ignored during this time for all csi lanes. 000 - 100us, 001= 200us, 010= 300us ...111= 800us etc

**7.7.1.25 BCC\_CONFIG Register (Address = 0x32) [Default = 0x09]**BCC\_CONFIG is shown in [BCC\\_CONFIG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-41. BCC\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	I2C_PASS_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASSTHROUGH	R/W	0x0	I2C Pass-Through to Deserializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled

**Table 7-41. BCC\_CONFIG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5	AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	RESERVED	R/W	0x0	Reserved
3	RX_PARITY_CHECKER_ENABLE	R/W	0x1	Parity Checker Enable 0: Disable 1: Enable
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

**7.7.1.26 DATAPATH\_CTL1 Register (Address = 0x33) [Default = 0x04]**DATAPATH\_CTL1 is shown in [DATAPATH\\_CTL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-42. DATAPATH\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-3	RESERVED	R/W	0x0	Reserved
2	DCA_CRC_EN	R/W	0x1	DCA CRC Enable If set to a 1, the Forward Channel will send a CRC as part of the DCA sequence. The DCA CRC protects the first 8 bytes of the DCA sequence. The CRC is sent as the 9th byte.
1-0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs

**7.7.1.27 REMOTE\_PAR\_CAP1 Register (Address = 0x35) [Default = 0x00]**REMOTE\_PAR\_CAP1 is shown in [REMOTE\\_PAR\\_CAP1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-43. REMOTE\_PAR\_CAP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FREEZE_DES_CAP	R/W	0x0	Freeze Partner Capabilities Prevent auto-loading of the Partner Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x1E and 0x1F.
6	RESERVED	R/W	0x0	Reserved
5	BIST_EN	R/W	0x0	Link BIST Enable This bit indicates the remote partner is requesting BIST operation over the FPD-Link III interface. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

**Table 7-43. REMOTE\_PAR\_CAP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	MPORT	R/W	0x0	Remote Partner Multi-Port capable 0: Remote partner is a single-port device 1: Remote partner is a multi-port device This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
3-0	PORT_NUM	R/W	0x0	Remote Partner port number When connected to a multi-port device, this field indicates the port number to which the Serializer is connected. This field is automatically configured by the Bidirectional Control Channel once back channel link has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

**7.7.1.28 DES\_ID Register (Address = 0x37) [Default = 0x7A]**DES\_ID is shown in [DES\\_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-44. DES\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	DESER_ID	R/W	0x3D	Remote Deserializer ID This field is normally loaded automatically from the remote Deserializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Deserializer Device ID Prevent auto-loading of the Deserializer Device ID from the Back Channel. The ID will be frozen at the value written.

**7.7.1.29 SLAVE\_ID\_0 Register (Address = 0x39) [Default = 0x00]**SLAVE\_ID\_0 is shown in [SLAVE\\_ID\\_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-45. SLAVE\_ID\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_0	R/W	0x0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.30 SLAVE\_ID\_1 Register (Address = 0x3A) [Default = 0x00]**SLAVE\_ID\_1 is shown in [SLAVE\\_ID\\_1 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-46. SLAVE\_ID\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_1	R/W	0x0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.31 SLAVE\_ID\_2 Register (Address = 0x3B) [Default = 0x00]**SLAVE\_ID\_2 is shown in [SLAVE\\_ID\\_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-47. SLAVE\_ID\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_2	R/W	0x0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.32 SLAVE\_ID\_3 Register (Address = 0x3C) [Default = 0x00]**SLAVE\_ID\_3 is shown in [SLAVE\\_ID\\_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-48. SLAVE\_ID\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_3	R/W	0x0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.33 SLAVE\_ID\_4 Register (Address = 0x3D) [Default = 0x00]**SLAVE\_ID\_4 is shown in [SLAVE\\_ID\\_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-49. SLAVE\_ID\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_4	R/W	0x0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.34 SLAVE\_ID\_5 Register (Address = 0x3E) [Default = 0x00]**

SLAVE\_ID\_5 is shown in [SLAVE\\_ID\\_5 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-50. SLAVE\_ID\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_5	R/W	0x0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.35 SLAVE\_ID\_6 Register (Address = 0x3F) [Default = 0x00]**

SLAVE\_ID\_6 is shown in [SLAVE\\_ID\\_6 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-51. SLAVE\_ID\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_6	R/W	0x0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.36 SLAVE\_ID\_7 Register (Address = 0x40) [Default = 0x00]**

SLAVE\_ID\_7 is shown in [SLAVE\\_ID\\_7 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-52. SLAVE\_ID\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_7	R/W	0x0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0x0	RESERVED.

**7.7.1.37 SLAVE\_ID\_ALIAS\_0 Register (Address = 0x41) [Default = 0x00]**

SLAVE\_ID\_ALIAS\_0 is shown in [SLAVE\\_ID\\_ALIAS\\_0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-53. SLAVE\_ID\_ALIAS\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_0	R/W	0x0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 0 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.38 SLAVE\_ID\_ALIAS\_1 Register (Address = 0x42) [Default = 0x00]**SLAVE\_ID\_ALIAS\_1 is shown in [SLAVE\\_ID\\_ALIAS\\_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-54. SLAVE\_ID\_ALIAS\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_1	R/W	0x0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 1 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.39 SLAVE\_ID\_ALIAS\_2 Register (Address = 0x43) [Default = 0x00]**SLAVE\_ID\_ALIAS\_2 is shown in [SLAVE\\_ID\\_ALIAS\\_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-55. SLAVE\_ID\_ALIAS\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_2	R/W	0x0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 2 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.40 SLAVE\_ID\_ALIAS\_3 Register (Address = 0x44) [Default = 0x00]**SLAVE\_ID\_ALIAS\_3 is shown in [SLAVE\\_ID\\_ALIAS\\_3 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-56. SLAVE\_ID\_ALIAS\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_3	R/W	0x0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 3 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.41 SLAVE\_ID\_ALIAS\_4 Register (Address = 0x45) [Default = 0x00]**SLAVE\_ID\_ALIAS\_4 is shown in [SLAVE\\_ID\\_ALIAS\\_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-57. SLAVE\_ID\_ALIAS\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_4	R/W	0x0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 4 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.42 SLAVE\_ID\_ALIAS\_5 Register (Address = 0x46) [Default = 0x00]**SLAVE\_ID\_ALIAS\_5 is shown in [SLAVE\\_ID\\_ALIAS\\_5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-58. SLAVE\_ID\_ALIAS\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_5	R/W	0x0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 5 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.43 SLAVE\_ID\_ALIAS\_6 Register (Address = 0x47) [Default = 0x00]**SLAVE\_ID\_ALIAS\_6 is shown in [SLAVE\\_ID\\_ALIAS\\_6 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-59. SLAVE\_ID\_ALIAS\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_6	R/W	0x0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 6 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.44 SLAVE\_ID\_ALIAS\_7 Register (Address = 0x48) [Default = 0x00]**SLAVE\_ID\_ALIAS\_7 is shown in [SLAVE\\_ID\\_ALIAS\\_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-60. SLAVE\_ID\_ALIAS\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID_ALIAS_7	R/W	0x0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 7 independent of the forward channel lock state or status of the remote Deserializer Acknowledge 1: Enable 0: Disable

**7.7.1.45 BC\_CTRL Register (Address = 0x49) [Default = 0x00]**BC\_CTRL is shown in [BC\\_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-61. BC\_CTRL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	BIST_CRC_ERR_CLR	RH/W1S	0x0	Clear BIST CRC error counter 1: Enable Clear
4	RESERVED	R/W	0x0	Reserved
3	CRC_ERR_CLR	RH/W1S	0x0	Clear CRC error 0: Disable clear 1: Enable clear
2-0	RESERVED	R/W	0x0	Reserved

**7.7.1.46 REV\_MASK\_ID Register (Address = 0x50) [Default = 0x10]**REV\_MASK\_ID is shown in [REV\\_MASK\\_ID Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-62. REV\_MASK\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	REVISION_ID	R	0x1	Revision ID 0000: TC1/TC2 0001: PG1.0
3-0	MASK_ID	R	0x0	Mask ID

**7.7.1.47 DEVICE\_STS Register (Address = 0x51) [Default = 0x00]**DEVICE\_STS is shown in [DEVICE\\_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-63. DEVICE\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CFG_CKSUM_STS	R	0x0	Config Checksum Passed This bit will be set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	0x0	Power-up initialization complete This bit will be set after Initialization is complete. Configuration from eFuse ROM has completed.
5-2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

**7.7.1.48 GENERAL\_STATUS Register (Address = 0x52) [Default = 0x05]**GENERAL\_STATUS is shown in [GENERAL\\_STATUS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-64. GENERAL\_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	AON_MODE_LATCHED	R	0x0	AON mode is latched (indicating the loss of PLL reference)
6	RX_LOCK_DETECT	R	0x0	Deserializer LOCK status This bit indicates the LOCK status of the Deserializer.
5	RESERVED	R	0x0	Reserved
4	LINK_LOST_FLAG	R	0x0	Back Channel Link lost Status changed This bit is set if a change in BC LINK DET lost status has been detected. This bit will be cleared upon read of CRC ERR CLR register or HS PLL loses lock.
3	BIST_CRC_ERR	R	0x0	BIST Error is detected. The BIST_ERR_CNT register contain the number of bist error
2	HS_PLL_LOCK_VAL	R	0x1	Forward Channel High speed PLL lock flag
1	CRC_ERR	R	0x0	Back Channel CRC error detected This bit is set when the back channel errors detected when BC LINK DET is asserted. This bit will be cleared upon write 1 to the CRC ERR CLR register .
0	LINK_DET	R	0x1	Back Channel Link detect This bit is set when BC link is valid.

**7.7.1.49 GPIO\_PIN\_STS Register (Address = 0x53) [Default = 0x00]**GPIO\_PIN\_STS is shown in [GPIO\\_PIN\\_STS Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-65. GPIO\_PIN\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0x0	Reserved
3-0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on GPIO pins. Bit 3 reads GPIO3 pin status Bit 2 reads GPIO2 status Bit 1 reads GPIO1 status Bit 0 reads GPIO0 status

**7.7.1.50 BIST\_ERR\_CNT Register (Address = 0x54) [Default = 0x00]**BIST\_ERR\_CNT is shown in [BIST\\_ERR\\_CNT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-66. BIST\_ERR\_CNT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	BIST_BC_ERRCNT	R	0x0	CRC error count in BIST mode.

**7.7.1.51 CRC\_ERR\_CNT1 Register (Address = 0x55) [Default = 0x00]**CRC\_ERR\_CNT1 is shown in [CRC\\_ERR\\_CNT1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-67. CRC\_ERR\_CNT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CRC_ERRCNT1	R	0x0	CRC Error count in Mission Mode (LSB)

**7.7.1.52 CRC\_ERR\_CNT2 Register (Address = 0x56) [Default = 0x00]**CRC\_ERR\_CNT2 is shown in [CRC\\_ERR\\_CNT2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-68. CRC\_ERR\_CNT2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CRC_ERRCNT2	R	0x0	CRC Error count in Mission Mode (MSB)

**7.7.1.53 INTERRUPT\_STS Register (Address = 0x57) [Default = 0x00]**INTERRUPT\_STS is shown in [INTERRUPT\\_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-69. INTERRUPT\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	INTERRUPT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit will be set to 1

**Table 7-69. INTERRUPT\_STS Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	IS_DEV	R	0x0	Local Device Interrupt: A general device interrupt has been generated. If this bit is set, the LOCAL_DEV_ISR register should be read to determine the source of the interrupt. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt
5-0	RESERVED	R	0x0	Reserved

**7.7.1.54 LOCAL\_DEV\_ISR Register (Address = 0x58) [Default = 0x00]**LOCAL\_DEV\_ISR is shown in [LOCAL\\_DEV\\_ISR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-70. LOCAL\_DEV\_ISR Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	IS_ESD_EVENT_INTR	R	0x0	Interrupt on ESD event.
3	IS LOSS OF CLKIN	R	0x0	Interrupt on loss of CLK_IN, when in external clock mode.
2	IS TEMP SENSOR	R	0x0	Interrupt on Temp Sensor. When enabled, an interrupt will be generated from the temperature sensor. Temp Sensor interrupts are controlled by registers 0x23 and 0x25 on sar adc page (page 4)
1	IS VOLT SENSOR	R	0x0	Interrupt on Voltage Sensor. When enabled, an interrupt will be generated from the voltage sensor. Voltage Sensor interrupts are controlled by registers 0x23-0x26 on sar adc page (page 4)
0	IS LINE FAULT	R	0x0	Interrupt on Line Fault. When enabled, an interrupt will be generated from the line fault detection circuit. Line Fault interrupts are controlled by registers 0x27-0x28 on sar adc page (page 4)

**7.7.1.55 CSI\_ERR\_CNT Register (Address = 0x5C) [Default = 0x00]**CSI\_ERR\_CNT is shown in [CSI\\_ERR\\_CNT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-71. CSI\_ERR\_CNT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_ERR_CNT	RC	0x0	CSI Error Counter Register This register counts the number of CSI packets received with errors since the last read of the counter. The count increments on uncorrectable 2 bit sync and ecc errors, csi line length mismatch error and checksum error

**7.7.1.56 CSI\_ERR\_STATUS Register (Address = 0x5D) [Default = 0x00]**CSI\_ERR\_STATUS is shown in [CSI\\_ERR\\_STATUS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-72. CSI\_ERR\_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	ALL_LANE_SYNC2_ERR	RC	0x0	Indicates a 2 bit sync error (uncorrectable)
3	LINE_LEN_MISMATCH	RC	0x0	Indicates Line length less than the received Packet header Word count

**Table 7-72. CSI\_ERR\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	CHKSUM_ERR	RC	0x0	Indicates a checksum error detected in the incoming data (uncorrectable)
1	ECC_2BIT_ERR	RC	0x0	Indicates a 2 Bit Ecc error (uncorrectable) in the Packet header
0	ECC_1BIT_ERR	RC	0x0	Indicates a 1 Bit Ecc error detected in the Packet header

**7.7.1.57 CSI\_ERR\_DLANE01 Register (Address = 0x5E) [Default = 0x00]**CSI\_ERR\_DLANE01 is shown in [CSI\\_ERR\\_DLANE01 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-73. CSI\_ERR\_DLANE01 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	SOT_ERROR_1	RC	0x0	Lane 1: Single Bit Error in SYNC Sequence - Correctable
6	SOT_SYNC_ERROR_1	RC	0x0	Lane 1:Multi bit Error in SYNC Sequence - Uncorrectable
5	CNTRL_ERR_HSRQST_1	RC	0x0	Lane 1: Control Error in HS Request Mode
4	RESERVED	RC	0x0	Reserved
3	SOT_ERROR_0	RC	0x0	Lane 0: Single Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_0	RC	0x0	Lane 0:Multi bit Error in SYNC Sequence - Uncorrectable
1	CNTRL_ERR_HSRQST_0	RC	0x0	Lane 0:Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

**7.7.1.58 CSI\_ERR\_DLANE23 Register (Address = 0x5F) [Default = 0x00]**CSI\_ERR\_DLANE23 is shown in [CSI\\_ERR\\_DLANE23 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-74. CSI\_ERR\_DLANE23 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	SOT_ERROR_3	RC	0x0	Lane 3:Single Bit Error in SYNC Sequence - Correctable
6	SOT_SYNC_ERROR_3	RC	0x0	Lane 3:Multi bit Error in SYNC Sequence - Uncorrectable
5	CNTRL_ERR_HSRQST_3	RC	0x0	Lane 3:Control Error in HS Request Mode
4	RESERVED	RC	0x0	Reserved
3	SOT_ERROR_2	RC	0x0	Lane 2:Single Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_2	RC	0x0	Lane 2:Multi bit Error in SYNC Sequence - Uncorrectable
1	CNTRL_ERR_HSRQST_2	RC	0x0	Lane 2:Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

**7.7.1.59 CSI\_ERR\_CLK\_LANE Register (Address = 0x60) [Default = 0x00]**CSI\_ERR\_CLK\_LANE is shown in [CSI\\_ERR\\_CLK\\_LANE Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-75. CSI\_ERR\_CLK\_LANE Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	RC	0x0	Reserved
3-2	RESERVED	R	0x0	Reserved

**Table 7-75. CSI\_ERR\_CLK\_LANE Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	CNTRL_ERR_HSRQST_	RC	0x0	Clk Lane: Control Error in HS Request Mode
0	RESERVED	RC	0x0	Reserved

**7.7.1.60 CSI\_PKT\_HDR\_VC\_ID Register (Address = 0x61) [Default = 0x00]**CSI\_PKT\_HDR\_VC\_ID is shown in [CSI\\_PKT\\_HDR\\_VC\\_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-76. CSI\_PKT\_HDR\_VC\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	LONG_PKT_DATA_ID	R	0x0	Data ID from CSI Packet header

**7.7.1.61 PKT\_HDR\_WC\_LSB Register (Address = 0x62) [Default = 0x00]**PKT\_HDR\_WC\_LSB is shown in [PKT\\_HDR\\_WC\\_LSB Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-77. PKT\_HDR\_WC\_LSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LONG_PKT_WRD_CNT_	R	0x0	Payload count lower byte from CSI Packet header
	LSB			

**7.7.1.62 PKT\_HDR\_WC\_MSB Register (Address = 0x63) [Default = 0x00]**PKT\_HDR\_WC\_MSB is shown in [PKT\\_HDR\\_WC\\_MSB Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-78. PKT\_HDR\_WC\_MSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LONG_PKT_WRD_CNT_	R	0x0	Payload count upper byte from CSI Packet header
	MSB			

**7.7.1.63 CSI\_ECC Register (Address = 0x64) [Default = 0x00]**CSI\_ECC is shown in [CSI\\_ECC Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-79. CSI\_ECC Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_LENGTH_CHANGE	RC	0x0	Indicates Line length change detected per frame
6	RESERVED	R	0x0	Reserved
5-0	CSI_ECC	R	0x0	CSI ECC byte from packet header

**7.7.1.64 IND\_ACC\_CTL Register (Address = 0xB0) [Default = 0x00]**IND\_ACC\_CTL is shown in [IND\\_ACC\\_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-80. IND\_ACC\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	RESERVED
4-2	IA_SEL	R/W	0x0	Indirect Register Select: Selects target for register access 000: PATGEN 001: RESERVED 010: DIE ID DATA 011: RESERVED 100: SAR ADC Registers 101: RESERVED
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

**7.7.1.65 ANA\_IA\_ADDR Register (Address = 0xB1) [Default = 0x00]**

ANA\_IA\_ADDR is shown in [ANA\\_IA\\_ADDR Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-81. ANA\_IA\_ADDR Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	ANA_IA_ADDR	R/W	0x0	Analog Register Offset: This register contains the 8-bit register offset for the indirect access.

**7.7.1.66 ANA\_IA\_DATA Register (Address = 0xB2) [Default = 0x00]**

ANA\_IA\_DATA is shown in [ANA\\_IA\\_DATA Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-82. ANA\_IA\_DATA Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	ANA_IA_DATA	R/W	0x0	Analog Register Data: Writing this register will cause an indirect write of the ANA_IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

**7.7.1.67 DIV\_OSC\_SEL0 Register (Address = 0xD8) [Default = 0x01]**

DIV\_OSC\_SEL0 is shown in [DIV\\_OSC\\_SEL0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-83. DIV\_OSC\_SEL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DIV_OSC_SWITCH_FOR_CE	R/W	0x0	Forces switching the output of M/N divider of OSC to CLKOUT

**Table 7-83. DIV\_OSC\_SEL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	DIV_OSC_SWITCH_EN	R/W	0x0	Enables the CLKOUT input selection scheme. If 0, this feature is disabled. If 1, whenever PLL Lock is low or the logic switches to AON mode, the OSCCLK M/N divider is used for CLKOUT
5	RESERVED	R	0x0	RESERVED
4-0	DIV_M_OSC_VAL	R/W	0x1	M Value for M/N divider for CLKOUT whose input is OSCCLK. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed using M/N ratio of internal OSCCLK clock to generate clock based on system camera requirement. Internal OSCCLK clock for the M/N divider is derived by forward channel data rate div by OSCCLK. When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100MHz. M Value should be >=1. If set to 0 then device will internally set it to 1.

**7.7.1.68 DIV\_OSC\_SEL1 Register (Address = 0xD9) [Default = 0x20]**DIV\_OSC\_SEL1 is shown in [DIV\\_OSC\\_SEL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-84. DIV\_OSC\_SEL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	DIV_N_OSC_VAL	R/W	0x20	N Value for M/N divider for CLKOUT whose input is OSCCLK. In CSI Synchronous mode and EXT clock mode, CLKOUT can be programmed by M/N ratio of internal OSCCLK clock to generate clock based on system camera requirement. Internal OSCCLK clock for the M/N divider is derived by forward channel data rate div by OSCCLK .When selecting the M/N ratio, they should be set to yield the CLKOUT frequency less than 100MHz.

**7.7.1.69 FPD3\_RX\_ID0 Register (Address = 0xF0) [Default = 0x5F]**FPD3\_RX\_ID0 is shown in [FPD3\\_RX\\_ID0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-85. FPD3\_RX\_ID0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID0	R	0x5F	FPD3_TX_ID0: First byte ID code: '_'

**7.7.1.70 FPD3\_RX\_ID1 Register (Address = 0xF1) [Default = 0x55]**FPD3\_RX\_ID1 is shown in [FPD3\\_RX\\_ID1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-86. FPD3\_RX\_ID1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID1	R	0x55	FPD3_TX_ID1: 2nd byte of ID code: 'U'

**7.7.1.71 FPD3\_RX\_ID2 Register (Address = 0xF2) [Default = 0x42]**FPD3\_RX\_ID2 is shown in [FPD3\\_RX\\_ID2 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-87. FPD3\_RX\_ID2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID2	R	0x42	FPD3_TX_ID2: 3rd byte of ID code: 'B'

**7.7.1.72 FPD3\_RX\_ID3 Register (Address = 0xF3) [Default = 0x39]**FPD3\_RX\_ID3 is shown in [FPD3\\_RX\\_ID3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-88. FPD3\_RX\_ID3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID3	R	0x39	FPD3_TX_ID3: 4th byte of ID code: '9'

**7.7.1.73 FPD3\_RX\_ID4 Register (Address = 0xF4) [Default = 0x37]**FPD3\_RX\_ID4 is shown in [FPD3\\_RX\\_ID4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-89. FPD3\_RX\_ID4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID4	R	0x37	FPD3_TX_ID4: 5th byte of ID code: '7'

**7.7.1.74 FPD3\_RX\_ID5 Register (Address = 0xF5) [Default = 0x31]**FPD3\_RX\_ID5 is shown in [FPD3\\_RX\\_ID5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-90. FPD3\_RX\_ID5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD3_TX_ID5	R	0x31	FPD3_TX_ID5: 6th byte of ID code: '1'

## 7.7.2 PATGEN Registers

[PATGEN Registers](#) lists the memory-mapped registers for the PATGEN registers. All register offset addresses not listed in [PATGEN Registers](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-91. PATGEN Registers**

Address	Acronym	Register Name	Section
0x1	PGEN_CTL	PGEN_CTL	Go
0x2	PGEN_CFG	PGEN_CFG	Go
0x3	PGEN_CSI_DI	PGEN_CSI_DI	Go
0x4	PGEN_LINE_SIZE1	PGEN_LINE_SIZE1	Go
0x5	PGEN_LINE_SIZE0	PGEN_LINE_SIZE0	Go
0x6	PGEN_BAR_SIZE1	PGEN_BAR_SIZE1	Go
0x7	PGEN_BAR_SIZE0	PGEN_BAR_SIZE0	Go
0x8	PGEN_ACT_LPF1	PGEN_ACT_LPF1	Go
0x9	PGEN_ACT_LPF0	PGEN_ACT_LPF0	Go
0xA	PGEN_TOT_LPF1	PGEN_TOT_LPF1	Go
0xB	PGEN_TOT_LPF0	PGEN_TOT_LPF0	Go
0xC	PGEN_LINE_PD1	PGEN_LINE_PD1	Go
0xD	PGEN_LINE_PD0	PGEN_LINE_PD0	Go
0xE	PGEN_VBP	PGEN_VBP	Go
0xF	PGEN_VFP	PGEN_VFP	Go
0x10	PGEN_COLOR0	PGEN_COLOR0	Go
0x11	PGEN_COLOR1	PGEN_COLOR1	Go
0x12	PGEN_COLOR2	PGEN_COLOR2	Go
0x13	PGEN_COLOR3	PGEN_COLOR3	Go
0x14	PGEN_COLOR4	PGEN_COLOR4	Go
0x15	PGEN_COLOR5	PGEN_COLOR5	Go
0x16	PGEN_COLOR6	PGEN_COLOR6	Go
0x17	PGEN_COLOR7	PGEN_COLOR7	Go
0x18	PGEN_COLOR8	PGEN_COLOR8	Go
0x19	PGEN_COLOR9	PGEN_COLOR9	Go
0x1A	PGEN_COLOR10	PGEN_COLOR10	Go
0x1B	PGEN_COLOR11	PGEN_COLOR11	Go
0x1C	PGEN_COLOR12	PGEN_COLOR12	Go
0x1D	PGEN_COLOR13	PGEN_COLOR13	Go
0x1E	PGEN_COLOR14	PGEN_COLOR14	Go
0x1F	PGEN_COLOR15	PGEN_COLOR15	Go

### 7.7.2.1 PGEN\_CTL Register (Address = 0x1) [Default = 0x00]

PGEN\_CTL is shown in [PGEN\\_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-92. PGEN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	RESERVED	R/W	0x0	RESERVED

**Table 7-92. PGEN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

**7.7.2.2 PGEN\_CFG Register (Address = 0x2) [Default = 0x33]**PGEN\_CFG is shown in [PGEN\\_CFG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-93. PGEN\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	RESERVED
5-4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3-0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 12.

**7.7.2.3 PGEN\_CSI\_DI Register (Address = 0x3) [Default = 0x24]**PGEN\_CSI\_DI is shown in [PGEN\\_CSI\\_DI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-94. PGEN\_CSI\_DI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5-0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

**7.7.2.4 PGEN\_LINE\_SIZE1 Register (Address = 0x4) [Default = 0x07]**PGEN\_LINE\_SIZE1 is shown in [PGEN\\_LINE\\_SIZE1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-95. PGEN\_LINE\_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.7.2.5 PGEN\_LINE\_SIZE0 Register (Address = 0x5) [Default = 0x80]**

PGEN\_LINE\_SIZE0 is shown in [PGEN\\_LINE\\_SIZE0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-96. PGEN\_LINE\_SIZE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.7.2.6 PGEN\_BAR\_SIZE1 Register (Address = 0x6) [Default = 0x00]**

PGEN\_BAR\_SIZE1 is shown in [PGEN\\_BAR\\_SIZE1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-97. PGEN\_BAR\_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.7.2.7 PGEN\_BAR\_SIZE0 Register (Address = 0x7) [Default = 0xF0]**

PGEN\_BAR\_SIZE0 is shown in [PGEN\\_BAR\\_SIZE0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-98. PGEN\_BAR\_SIZE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.7.2.8 PGEN\_ACT\_LPF1 Register (Address = 0x8) [Default = 0x01]**

PGEN\_ACT\_LPF1 is shown in [PGEN\\_ACT\\_LPF1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-99. PGEN\_ACT\_LPF1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.7.2.9 PGEN\_ACT\_LPF0 Register (Address = 0x9) [Default = 0xE0]**

PGEN\_ACT\_LPF0 is shown in [PGEN\\_ACT\\_LPF0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-100. PGEN\_ACT\_LPF0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.7.2.10 PGEN\_TOT\_LPF1 Register (Address = 0xA) [Default = 0x02]**PGEN\_TOT\_LPF1 is shown in [PGEN\\_TOT\\_LPF1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-101. PGEN\_TOT\_LPF1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

**7.7.2.11 PGEN\_TOT\_LPF0 Register (Address = 0xB) [Default = 0x0D]**PGEN\_TOT\_LPF0 is shown in [PGEN\\_TOT\\_LPF0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-102. PGEN\_TOT\_LPF0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

**7.7.2.12 PGEN\_LINE\_PD1 Register (Address = 0xC) [Default = 0x0C]**PGEN\_LINE\_PD1 is shown in [PGEN\\_LINE\\_PD1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-103. PGEN\_LINE\_PD1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

**7.7.2.13 PGEN\_LINE\_PD0 Register (Address = 0xD) [Default = 0x67]**PGEN\_LINE\_PD0 is shown in [PGEN\\_LINE\\_PD0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-104. PGEN\_LINE\_PD0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

**7.7.2.14 PGEN\_VBP Register (Address = 0xE) [Default = 0x21]**

PGEN\_VBP is shown in [PGEN\\_VBP Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-105. PGEN\_VBP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

**7.7.2.15 PGEN\_VFP Register (Address = 0xF) [Default = 0x0A]**

PGEN\_VFP is shown in [PGEN\\_VFP Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-106. PGEN\_VFP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

**7.7.2.16 PGEN\_COLOR0 Register (Address = 0x10) [Default = 0xAA]**

PGEN\_COLOR0 is shown in [PGEN\\_COLOR0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-107. PGEN\_COLOR0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

**7.7.2.17 PGEN\_COLOR1 Register (Address = 0x11) [Default = 0x33]**

PGEN\_COLOR1 is shown in [PGEN\\_COLOR1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-108. PGEN\_COLOR1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

**7.7.2.18 PGEN\_COLOR2 Register (Address = 0x12) [Default = 0xF0]**

PGEN\_COLOR2 is shown in [PGEN\\_COLOR2 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-109. PGEN\_COLOR2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

**7.7.2.19 PGEN\_COLOR3 Register (Address = 0x13) [Default = 0x7F]**PGEN\_COLOR3 is shown in [PGEN\\_COLOR3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-110. PGEN\_COLOR3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

**7.7.2.20 PGEN\_COLOR4 Register (Address = 0x14) [Default = 0x55]**PGEN\_COLOR4 is shown in [PGEN\\_COLOR4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-111. PGEN\_COLOR4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

**7.7.2.21 PGEN\_COLOR5 Register (Address = 0x15) [Default = 0xCC]**PGEN\_COLOR5 is shown in [PGEN\\_COLOR5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-112. PGEN\_COLOR5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

**7.7.2.22 PGEN\_COLOR6 Register (Address = 0x16) [Default = 0x0F]**PGEN\_COLOR6 is shown in [PGEN\\_COLOR6 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-113. PGEN\_COLOR6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

**7.7.2.23 PGEN\_COLOR7 Register (Address = 0x17) [Default = 0x80]**PGEN\_COLOR7 is shown in [PGEN\\_COLOR7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-114. PGEN\_COLOR7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

**7.7.2.24 PGEN\_COLOR8 Register (Address = 0x18) [Default = 0x00]**PGEN\_COLOR8 is shown in [PGEN\\_COLOR8 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-115. PGEN\_COLOR8 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

**7.7.2.25 PGEN\_COLOR9 Register (Address = 0x19) [Default = 0x00]**PGEN\_COLOR9 is shown in [PGEN\\_COLOR9 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-116. PGEN\_COLOR9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

**7.7.2.26 PGEN\_COLOR10 Register (Address = 0x1A) [Default = 0x00]**PGEN\_COLOR10 is shown in [PGEN\\_COLOR10 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-117. PGEN\_COLOR10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

**7.7.2.27 PGEN\_COLOR11 Register (Address = 0x1B) [Default = 0x00]**

PGEN\_COLOR11 is shown in [PGEN\\_COLOR11 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-118. PGEN\_COLOR11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

**7.7.2.28 PGEN\_COLOR12 Register (Address = 0x1C) [Default = 0x00]**

PGEN\_COLOR12 is shown in [PGEN\\_COLOR12 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-119. PGEN\_COLOR12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

**7.7.2.29 PGEN\_COLOR13 Register (Address = 0x1D) [Default = 0x00]**

PGEN\_COLOR13 is shown in [PGEN\\_COLOR13 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-120. PGEN\_COLOR13 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

**7.7.2.30 PGEN\_COLOR14 Register (Address = 0x1E) [Default = 0x00]**

PGEN\_COLOR14 is shown in [PGEN\\_COLOR14 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-121. PGEN\_COLOR14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

**7.7.2.31 PGEN\_COLOR15 Register (Address = 0x1F) [Default = 0x00]**

PGEN\_COLOR15 is shown in [PGEN\\_COLOR15 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-122. PGEN\_COLOR15 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the sixteenth byte of the fixed color pattern.

### 7.7.3 SAR\_ADC Registers

SAR\_ADC Registers lists the memory-mapped registers for the SAR\_ADC registers. All register offset addresses not listed in SAR\_ADC Registers should be considered as reserved locations and the register contents should not be modified.

**Table 7-123. SAR\_ADC Registers**

Address	Acronym	Register Name	Section
0x4	SAR_ADC_CLK_SAMPLE_SEL	SAR_ADC_CLK_SAMPLE_SEL	Go
0x8	SAR_ADC_INPUT_EN_MSB	SAR_ADC_INPUT_EN_MSB	Go
0xD	ADC_CNTRL_MODE_0	ADC_CNTRL_MODE_0	Go
0x13	TEMP_FINAL	TEMP_FINAL	Go
0x15	IV0_FINAL	IV0_FINAL	Go
0x16	IV1_FINAL	IV1_FINAL	Go
0x1B	EXT_VOL0_FINAL	EXT_VOL0_FINAL	Go
0x1C	EXT_VOL1_FINAL	EXT_VOL1_FINAL	Go
0x1D	LINE_FAULT0_FINAL	LINE_FAULT0_FINAL	Go
0x1E	LINE_FAULT1_FINAL	LINE_FAULT1_FINAL	Go
0x23	INT_STATUS_LSB_LOW	INT_STATUS_LSB_LOW	Go
0x24	INT_STATUS_MSB_LOW	INT_STATUS_MSB_LOW	Go
0x25	INT_STATUS_LSB_HIGH	INT_STATUS_LSB_HIGH	Go
0x26	INT_STATUS_MSB_HIGH	INT_STATUS_MSB_HIGH	Go
0x27	INT_LINE_FAULT0_M0	INT_LINE_FAULT0_M0	Go
0x28	INT_LINE_FAULT1_M0	INT_LINE_FAULT1_M0	Go
0x2B	INT_LINE_FAULT0_M1	INT_LINE_FAULT0_M1	Go
0x2C	INT_LINE_FAULT1_M1	INT_LINE_FAULT1_M1	Go
0x2F	INT_LINE_FAULT_UNDEF	INT_LINE_FAULT_UNDEF	Go
0x30	INT_LINE_FAULT_SATURATE	INT_LINE_FAULT_SATURATE	Go
0x33	TEMP_HIGH	TEMP_HIGH	Go
0x34	TEMP_LOW	TEMP_LOW	Go
0x35	TEMP_ADC_OFFSET	TEMP_ADC_OFFSET	Go
0x39	IV0_HIGH	IV0_HIGH	Go
0x3A	IV0_LOW	IV0_LOW	Go
0x3B	IV0_ADC_OFFSET	IV0_ADC_OFFSET	Go
0x3C	IV1_HIGH	IV1_HIGH	Go
0x3D	IV1_LOW	IV1_LOW	Go
0x3E	IV1_ADC_OFFSET	IV1_ADC_OFFSET	Go
0x4B	TEMP_IV_MASK	TEMP_IV_MASK	Go
0x4C	EXT_VOL0_HIGH	EXT_VOL0_HIGH	Go
0x4D	EXT_VOL0_LOW	EXT_VOL0_LOW	Go
0x4E	EXT_VOL0_ADC_OFFSET	EXT_VOL0_ADC_OFFSET	Go
0x4F	EXT_VOL1_HIGH	EXT_VOL1_HIGH	Go
0x50	EXT_VOL1_LOW	EXT_VOL1_LOW	Go
0x51	EXT_VOL1_ADC_OFFSET	EXT_VOL1_ADC_OFFSET	Go
0x52	EXT_VOL_MASK	EXT_VOL_MASK	Go
0x53	LINE_FAULT0_THRESH_0_HI_M0	LINE_FAULT0_THRESH_0_HI_M0	Go
0x54	LINE_FAULT0_THRESH_0_LO_M0	LINE_FAULT0_THRESH_0_LO_M0	Go

**Table 7-123. SAR\_ADC Registers (continued)**

Address	Acronym	Register Name	Section
0x55	LINE_FAULT0_THRESH_1_HI_M0	LINE_FAULT0_THRESH_1_HI_M0	Go
0x56	LINE_FAULT0_THRESH_1_LO_M0	LINE_FAULT0_THRESH_1_LO_M0	Go
0x57	LINE_FAULT0_THRESH_2_HI_M0	LINE_FAULT0_THRESH_2_HI_M0	Go
0x58	LINE_FAULT0_THRESH_2_LO_M0	LINE_FAULT0_THRESH_2_LO_M0	Go
0x59	LINE_FAULT0_THRESH_3_HI_M0	LINE_FAULT0_THRESH_3_HI_M0	Go
0x5A	LINE_FAULT0_THRESH_3_LO_M0	LINE_FAULT0_THRESH_3_LO_M0	Go
0x5B	LINE_FAULT0_THRESH_4_HI_M0	LINE_FAULT0_THRESH_4_HI_M0	Go
0x5C	LINE_FAULT0_THRESH_4_LO_M0	LINE_FAULT0_THRESH_4_LO_M0	Go
0x5D	LINE_FAULT0_THRESH_5_HI_M0	LINE_FAULT0_THRESH_5_HI_M0	Go
0x5E	LINE_FAULT0_THRESH_5_LO_M0	LINE_FAULT0_THRESH_5_LO_M0	Go
0x5F	LINE_FAULT0_THRESH_6_HI_M0	LINE_FAULT0_THRESH_6_HI_M0	Go
0x60	LINE_FAULT0_THRESH_6_LO_M0	LINE_FAULT0_THRESH_6_LO_M0	Go
0x61	LINE_FAULT0_THRESH_7_HI_M0	LINE_FAULT0_THRESH_7_HI_M0	Go
0x62	LINE_FAULT0_THRESH_7_LO_M0	LINE_FAULT0_THRESH_7_LO_M0	Go
0x63	LINE_FAULT0_THRESH_MASK_M0	LINE_FAULT0_THRESH_MASK_M0	Go
0x64	LINE_FAULT0_ADC_OFFSET_M0	LINE_FAULT0_ADC_OFFSET_M0	Go
0x65	LINE_FAULT1_THRESH_0_HI_M0	LINE_FAULT1_THRESH_0_HI_M0	Go
0x66	LINE_FAULT1_THRESH_0_LO_M0	LINE_FAULT1_THRESH_0_LO_M0	Go
0x67	LINE_FAULT1_THRESH_1_HI_M0	LINE_FAULT1_THRESH_1_HI_M0	Go
0x68	LINE_FAULT1_THRESH_1_LO_M0	LINE_FAULT1_THRESH_1_LO_M0	Go
0x69	LINE_FAULT1_THRESH_2_HI_M0	LINE_FAULT1_THRESH_2_HI_M0	Go
0x6A	LINE_FAULT1_THRESH_2_LO_M0	LINE_FAULT1_THRESH_2_LO_M0	Go
0x6B	LINE_FAULT1_THRESH_3_HI_M0	LINE_FAULT1_THRESH_3_HI_M0	Go
0x6C	LINE_FAULT1_THRESH_3_LO_M0	LINE_FAULT1_THRESH_3_LO_M0	Go
0x6D	LINE_FAULT1_THRESH_4_HI_M0	LINE_FAULT1_THRESH_4_HI_M0	Go
0x6E	LINE_FAULT1_THRESH_4_LO_M0	LINE_FAULT1_THRESH_4_LO_M0	Go
0x6F	LINE_FAULT1_THRESH_5_HI_M0	LINE_FAULT1_THRESH_5_HI_M0	Go

**Table 7-123. SAR\_ADC Registers (continued)**

Address	Acronym	Register Name	Section
0x70	LINE_FAULT1_THRESH_5_LO_M0	LINE_FAULT1_THRESH_5_LO_M0	Go
0x71	LINE_FAULT1_THRESH_6_HI_M0	LINE_FAULT1_THRESH_6_HI_M0	Go
0x72	LINE_FAULT1_THRESH_6_LO_M0	LINE_FAULT1_THRESH_6_LO_M0	Go
0x73	LINE_FAULT1_THRESH_7_HI_M0	LINE_FAULT1_THRESH_7_HI_M0	Go
0x74	LINE_FAULT1_THRESH_7_LO_M0	LINE_FAULT1_THRESH_7_LO_M0	Go
0x75	LINE_FAULT1_THRESH_MASK_M0	LINE_FAULT1_THRESH_MASK_M0	Go
0x76	LINE_FAULT1_ADC_OFFSET_M0	LINE_FAULT1_ADC_OFFSET_M0	Go
0x9B	LINE_FAULT0_THRESH_0_HI_M1	LINE_FAULT0_THRESH_0_HI_M1	Go
0x9C	LINE_FAULT0_THRESH_0_LO_M1	LINE_FAULT0_THRESH_0_LO_M1	Go
0x9D	LINE_FAULT0_THRESH_1_HI_M1	LINE_FAULT0_THRESH_1_HI_M1	Go
0x9E	LINE_FAULT0_THRESH_1_LO_M1	LINE_FAULT0_THRESH_1_LO_M1	Go
0x9F	LINE_FAULT0_THRESH_2_HI_M1	LINE_FAULT0_THRESH_2_HI_M1	Go
0xA0	LINE_FAULT0_THRESH_2_LO_M1	LINE_FAULT0_THRESH_2_LO_M1	Go
0xA1	LINE_FAULT0_THRESH_3_HI_M1	LINE_FAULT0_THRESH_3_HI_M1	Go
0xA2	LINE_FAULT0_THRESH_3_LO_M1	LINE_FAULT0_THRESH_3_LO_M1	Go
0xA3	LINE_FAULT0_THRESH_4_HI_M1	LINE_FAULT0_THRESH_4_HI_M1	Go
0xA4	LINE_FAULT0_THRESH_4_LO_M1	LINE_FAULT0_THRESH_4_LO_M1	Go
0xA5	LINE_FAULT0_THRESH_5_HI_M1	LINE_FAULT0_THRESH_5_HI_M1	Go
0xA6	LINE_FAULT0_THRESH_5_LO_M1	LINE_FAULT0_THRESH_5_LO_M1	Go
0xA7	LINE_FAULT0_THRESH_6_HI_M1	LINE_FAULT0_THRESH_6_HI_M1	Go
0xA8	LINE_FAULT0_THRESH_6_LO_M1	LINE_FAULT0_THRESH_6_LO_M1	Go
0xA9	LINE_FAULT0_THRESH_7_HI_M1	LINE_FAULT0_THRESH_7_HI_M1	Go
0xAA	LINE_FAULT0_THRESH_7_LO_M1	LINE_FAULT0_THRESH_7_LO_M1	Go
0xAB	LINE_FAULT0_THRESH_MASK_M1	LINE_FAULT0_THRESH_MASK_M1	Go
0xAC	LINE_FAULT0_ADC_OFFSET_M1	LINE_FAULT0_ADC_OFFSET_M1	Go
0xAD	LINE_FAULT1_THRESH_0_HI_M1	LINE_FAULT1_THRESH_0_HI_M1	Go
0xAE	LINE_FAULT1_THRESH_0_LO_M1	LINE_FAULT1_THRESH_0_LO_M1	Go

**Table 7-123. SAR\_ADC Registers (continued)**

Address	Acronym	Register Name	Section
0xAF	LINE_FAULT1_THRESH_1_HI_M1	LINE_FAULT1_THRESH_1_HI_M1	Go
0xB0	LINE_FAULT1_THRESH_1_LO_M1	LINE_FAULT1_THRESH_1_LO_M1	Go
0xB1	LINE_FAULT1_THRESH_2_HI_M1	LINE_FAULT1_THRESH_2_HI_M1	Go
0xB2	LINE_FAULT1_THRESH_2_LO_M1	LINE_FAULT1_THRESH_2_LO_M1	Go
0xB3	LINE_FAULT1_THRESH_3_HI_M1	LINE_FAULT1_THRESH_3_HI_M1	Go
0xB4	LINE_FAULT1_THRESH_3_LO_M1	LINE_FAULT1_THRESH_3_LO_M1	Go
0xB5	LINE_FAULT1_THRESH_4_HI_M1	LINE_FAULT1_THRESH_4_HI_M1	Go
0xB6	LINE_FAULT1_THRESH_4_LO_M1	LINE_FAULT1_THRESH_4_LO_M1	Go
0xB7	LINE_FAULT1_THRESH_5_HI_M1	LINE_FAULT1_THRESH_5_HI_M1	Go
0xB8	LINE_FAULT1_THRESH_5_LO_M1	LINE_FAULT1_THRESH_5_LO_M1	Go
0xB9	LINE_FAULT1_THRESH_6_HI_M1	LINE_FAULT1_THRESH_6_HI_M1	Go
0xBA	LINE_FAULT1_THRESH_6_LO_M1	LINE_FAULT1_THRESH_6_LO_M1	Go
0xBB	LINE_FAULT1_THRESH_7_HI_M1	LINE_FAULT1_THRESH_7_HI_M1	Go
0xBC	LINE_FAULT1_THRESH_7_LO_M1	LINE_FAULT1_THRESH_7_LO_M1	Go
0xBD	LINE_FAULT1_THRESH_MASK_M1	LINE_FAULT1_THRESH_MASK_M1	Go
0xBE	LINE_FAULT1_ADC_OFFSET_M1	LINE_FAULT1_ADC_OFFSET_M1	Go
0xE3	LINE_FAULT0_11_PD_SEL	LINE_FAULT0_11_PD_SEL	Go
0xE5	ADC_OFFSET_POL0	ADC_OFFSET_POL0	Go
0xE6	ADC_OFFSET_POL1	ADC_OFFSET_POL1	Go
0xE7	ADC_OFFSET_POL2	ADC_OFFSET_POL2	Go

**7.7.3.1 SAR\_ADC\_CLK\_SAMPLE\_SEL Register (Address = 0x4) [Default = 0xD0]**SAR\_ADC\_CLK\_SAMPLE\_SEL is shown in [SAR\\_ADC\\_CLK\\_SAMPLE\\_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-124. SAR\_ADC\_CLK\_SAMPLE\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	SAR_ADC_AVERAGING_SEL	R/W	0x3	Moving average select 0: no avg 1: 2 samples 2: 4 samples 3: 8 samples
5-4	RESERVED	R/W	0x1	Reserved
3-0	RESERVED	R	0x0	Reserved

**7.7.3.2 SAR\_ADC\_INPUT\_EN\_MSB Register (Address = 0x8) [Default = 0x00]**

SAR\_ADC\_INPUT\_EN\_MSB is shown in [SAR\\_ADC\\_INPUT\\_EN\\_MSB Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-125. SAR\_ADC\_INPUT\_EN\_MSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SAR_ADC_INPUT_EN_MSB	R/W	0x0	Enable for sar adc and selects which inputs to sample - Thermal coded SAR_ADC_INPUT_EN[0]= EXT_VOL0 - GPIO0 SAR_ADC_INPUT_EN[1]= EXT_VOL1 - GPIO1 SAR_ADC_INPUT_EN[2]= LINE_FAULT0 - GPIO0 SAR_ADC_INPUT_EN[3]= LINE_FAULT1 - GPIO1 SAR_ADC_INPUT_EN[4]= RESERVED SAR_ADC_INPUT_EN[5]= RESERVED SAR_ADC_INPUT_EN[6]= RESERVED SAR_ADC_INPUT_EN[7]= RESERVED

**7.7.3.3 ADC\_CNTRL\_MODE\_0 Register (Address = 0xD) [Default = 0x80]**

ADC\_CNTRL\_MODE\_0 is shown in [ADC\\_CNTRL\\_MODE\\_0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-126. ADC\_CNTRL\_MODE\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ADC_DISABLE	R/W	0x1	Setting 1 disables the ADC controller
6	RESERVED	R/W	0x0	Reserved
5-3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R	0x0	Reserved

**7.7.3.4 TEMP\_FINAL Register (Address = 0x13) [Default = 0x00]**

TEMP\_FINAL is shown in [TEMP\\_FINAL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-127. TEMP\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_FINAL	R	0x0	Holds ADC value for temp_final

**7.7.3.5 IV0\_FINAL Register (Address = 0x15) [Default = 0x00]**

IV0\_FINAL is shown in [IV0\\_FINAL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-128. IV0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_FINAL	R	0x0	Holds ADC value for IV0_final

**7.7.3.6 IV1\_FINAL Register (Address = 0x16) [Default = 0x00]**

IV1\_FINAL is shown in [IV1\\_FINAL Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-129. IV1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_FINAL	R	0x0	Holds ADC value for IV1_final

**7.7.3.7 EXT\_VOL0\_FINAL Register (Address = 0x1B) [Default = 0x00]**EXT\_VOL0\_FINAL is shown in [EXT\\_VOL0\\_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-130. EXT\_VOL0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_FINAL	R	0x0	Holds ADC value for EXT_VOL0_final

**7.7.3.8 EXT\_VOL1\_FINAL Register (Address = 0x1C) [Default = 0x00]**EXT\_VOL1\_FINAL is shown in [EXT\\_VOL1\\_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-131. EXT\_VOL1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_FINAL	R	0x0	Holds ADC value for EXT_VOL1_final

**7.7.3.9 LINE\_FAULT0\_FINAL Register (Address = 0x1D) [Default = 0x00]**LINE\_FAULT0\_FINAL is shown in [LINE\\_FAULT0\\_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-132. LINE\_FAULT0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_FINAL	R	0x0	Holds ADC value for LINE_FAULT0_final

**7.7.3.10 LINE\_FAULT1\_FINAL Register (Address = 0x1E) [Default = 0x00]**LINE\_FAULT1\_FINAL is shown in [LINE\\_FAULT1\\_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-133. LINE\_FAULT1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_FINAL	R	0x0	Holds ADC value for LINE_FAULT1_final

**7.7.3.11 INT\_STATUS\_LSB\_LOW Register (Address = 0x23) [Default = 0x00]**INT\_STATUS\_LSB\_LOW is shown in [INT\\_STATUS\\_LSB\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-134. INT\_STATUS\_LSB\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_LSB_LOW		0x0	Interrupt status for temperature/internal voltages [0]= temp [1]= RESERVED [2]= IV0 [3]= IV1 [4]= RESERVED [5]= RESERVED [6]= RESERVED [7]= RESERVED

**7.7.3.12 INT\_STATUS\_MSB\_LOW Register (Address = 0x24) [Default = 0x00]**INT\_STATUS\_MSB\_LOW is shown in [INT\\_STATUS\\_MSB\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-135. INT\_STATUS\_MSB\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_MSB_LOW		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= EXT_VOL0 00000010= EXT_VOL1 00000100= RESERVED 00001000= RESERVED 00010000= RESERVED 00100000= RESERVED 01000000= RESERVED 10000000= RESERVED

**7.7.3.13 INT\_STATUS\_LSB\_HIGH Register (Address = 0x25) [Default = 0x00]**INT\_STATUS\_LSB\_HIGH is shown in [INT\\_STATUS\\_LSB\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-136. INT\_STATUS\_LSB\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_LSB_HIGH		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= temp 00000010= RESERVED 00000100= IV0 00001000= IV1 00010000= RESERVED 00100000= RESERVED 01000000= RESERVED 10000000= RESERVED

**7.7.3.14 INT\_STATUS\_MSB\_HIGH Register (Address = 0x26) [Default = 0x00]**INT\_STATUS\_MSB\_HIGH is shown in [INT\\_STATUS\\_MSB\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-137. INT\_STATUS\_MSB\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_MSB_HIGH		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= EXT_VOL0 00000010= EXT_VOL1 00000100= RESERVED 00001000= RESERVED 00010000= RESERVED 00100000= RESERVED 01000000= RESERVED 10000000= RESERVED

**7.7.3.15 INT\_LINE\_FAULT0\_M0 Register (Address = 0x27) [Default = 0x00]**INT\_LINE\_FAULT0\_M0 is shown in [INT\\_LINE\\_FAULT0\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-138. INT\_LINE\_FAULT0\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT0_M0		0x0	Interrupt status for LINE_FAULT0 (one-hot) 00000001= short to ground (threshold 0) 00000010= normal operation (threshold 1) 00000100= short to 1.1V (threshold 2) 00001000= short to 1.8V (threshold 3) 00010000= short to 3.3V (threshold 4) 00100000= threshold 5 01000000= threshold 6 10000000= threshold 7

**7.7.3.16 INT\_LINE\_FAULT1\_M0 Register (Address = 0x28) [Default = 0x00]**INT\_LINE\_FAULT1\_M0 is shown in [INT\\_LINE\\_FAULT1\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-139. INT\_LINE\_FAULT1\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT1_M0		0x0	Interrupt status for LINE_FAULT1 (one-hot) 00000001= short to ground (threshold 0) 00000010= normal operation (threshold 1) 00000100= short to 1.1V (threshold 2) 00001000= short to 1.8V (threshold 3) 00010000= short to 3.3V (threshold 4) 00100000= threshold 5 01000000= threshold 6 10000000= threshold 7

**7.7.3.17 INT\_LINE\_FAULT0\_M1 Register (Address = 0x2B) [Default = 0x00]**INT\_LINE\_FAULT0\_M1 is shown in [INT\\_LINE\\_FAULT0\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-140. INT\_LINE\_FAULT0\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT0_M1		0x0	Interrupt status for LINE_FAULT0 (one-hot) 00000001= short to ground (threshold 0) 00000010= normal operation (threshold 1) 00000100= short to 1.1V (threshold 2) 00001000= short to 1.8V (threshold 3) 00010000= short to 3.3V (threshold 4) 00100000= threshold 5 01000000= threshold 6 10000000= threshold 7

**7.7.3.18 INT\_LINE\_FAULT1\_M1 Register (Address = 0x2C) [Default = 0x00]**INT\_LINE\_FAULT1\_M1 is shown in [INT\\_LINE\\_FAULT1\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-141. INT\_LINE\_FAULT1\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT1_M1		0x0	Interrupt status for LINE_FAULT1 (one-hot) 00000001= short to ground (threshold 0) 00000010= normal operation (threshold 1) 00000100= short to 1.1V (threshold 2) 00001000= short to 1.8V (threshold 3) 00010000= short to 3.3V (threshold 4) 00100000= threshold 5 01000000= threshold 6 10000000= threshold 7

**7.7.3.19 INT\_LINE\_FAULT\_UNDEF Register (Address = 0x2F) [Default = 0x00]**INT\_LINE\_FAULT\_UNDEF is shown in [INT\\_LINE\\_FAULT\\_UNDEF Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-142. INT\_LINE\_FAULT\_UNDEF Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	INT_LINE_FAULT_UNDE F_M1		0x0	Interrupt status to signal ADC value in undefined range 0 - LINE_FAULT0 1 - LINE_FAULT1 2 - RESERVED 3 - RESERVED
3-0	INT_LINE_FAULT_UNDE F_M0		0x0	Interrupt status to signal ADC value in undefined range 0 - LINE_FAULT0 1 - LINE_FAULT1 2 - RESERVED 3 - RESERVED

**7.7.3.20 INT\_LINE\_FAULT\_SATURATE Register (Address = 0x30) [Default = 0x00]**INT\_LINE\_FAULT\_SATURATE is shown in [INT\\_LINE\\_FAULT\\_SATURATE Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-143. INT\_LINE\_FAULT\_SATURATE Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0x0	

**Table 7-143. INT\_LINE\_FAULT\_SATURATE Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	INT_LINE_FAULT1_SATURATE		0x0	Indicates LINE_FAULT Detection Saturated, Voltage sensed is beyond the ADC range
0	INT_LINE_FAULT0_SATURATE		0x0	Indicates LINE_FAULT Detection Saturated, Voltage sensed is beyond the ADC range

**7.7.3.21 TEMP\_HIGH Register (Address = 0x33) [Default = 0xAC]**TEMP\_HIGH is shown in [TEMP\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-144. TEMP\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_HIGH	R/W	0xAC	Upper threshold for the Die Temp

**7.7.3.22 TEMP\_LOW Register (Address = 0x34) [Default = 0x69]**TEMP\_LOW is shown in [TEMP\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-145. TEMP\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_LOW	R/W	0x69	Lower threshold for the Die temp

**7.7.3.23 TEMP\_ADC\_OFFSET Register (Address = 0x35) [Default = 0x00]**TEMP\_ADC\_OFFSET is shown in [TEMP\\_ADC\\_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-146. TEMP\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the temperature conversion

**7.7.3.24 IV0\_HIGH Register (Address = 0x39) [Default = 0x70]**IV0\_HIGH is shown in [IV0\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-147. IV0\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_HIGH	R/W	0x70	Upper threshold for IV0

**7.7.3.25 IV0\_LOW Register (Address = 0x3A) [Default = 0x66]**IV0\_LOW is shown in [IV0\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-148. IV0\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_LOW	R/W	0x66	Lower threshold for IV0

**7.7.3.26 IV0\_ADC\_OFFSET Register (Address = 0x3B) [Default = 0x00]**IV0\_ADC\_OFFSET is shown in [IV0\\_ADC\\_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-149. IV0\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the IV0 voltage conversion

**7.7.3.27 IV1\_HIGH Register (Address = 0x3C) [Default = 0x70]**IV1\_HIGH is shown in [IV1\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-150. IV1\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_HIGH	R/W	0x70	Upper threshold for IV1

**7.7.3.28 IV1\_LOW Register (Address = 0x3D) [Default = 0x66]**IV1\_LOW is shown in [IV1\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-151. IV1\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_LOW	R/W	0x66	Lower threshold for IV1

**7.7.3.29 IV1\_ADC\_OFFSET Register (Address = 0x3E) [Default = 0x00]**IV1\_ADC\_OFFSET is shown in [IV1\\_ADC\\_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-152. IV1\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the IV1 voltage conversion

**7.7.3.30 TEMP\_IV\_MASK Register (Address = 0x4B) [Default = 0xC2]**TEMP\_IV\_MASK is shown in [TEMP\\_IV\\_MASK Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-153. TEMP\_IV\_MASK Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved

**Table 7-153. TEMP\_IV\_MASK Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	IV1_THRESH_MASK	R/W	0x0	1: no interrupt
2	IV0_THRESH_MASK	R/W	0x0	1: no interrupt
1	RESERVED	R/W	0x1	Reserved
0	TEMP_THRESH_MASK	R/W	0x0	1: no interrupt

**7.7.3.31 EXT\_VOL0\_HIGH Register (Address = 0x4C) [Default = 0x00]**EXT\_VOL0\_HIGH is shown in [EXT\\_VOL0\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-154. EXT\_VOL0\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_HIGH	R/W	0x0	Upper threshold for EXT_VOL0

**7.7.3.32 EXT\_VOL0\_LOW Register (Address = 0x4D) [Default = 0x00]**EXT\_VOL0\_LOW is shown in [EXT\\_VOL0\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-155. EXT\_VOL0\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_LOW	R/W	0x0	Lower threshold for EXT_VOL0

**7.7.3.33 EXT\_VOL0\_ADC\_OFFSET Register (Address = 0x4E) [Default = 0x00]**EXT\_VOL0\_ADC\_OFFSET is shown in [EXT\\_VOL0\\_ADC\\_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-156. EXT\_VOL0\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the vol0 voltage conversion

**7.7.3.34 EXT\_VOL1\_HIGH Register (Address = 0x4F) [Default = 0x00]**EXT\_VOL1\_HIGH is shown in [EXT\\_VOL1\\_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-157. EXT\_VOL1\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_HIGH	R/W	0x0	Upper threshold for EXT_VOL1

**7.7.3.35 EXT\_VOL1\_LOW Register (Address = 0x50) [Default = 0x00]**EXT\_VOL1\_LOW is shown in [EXT\\_VOL1\\_LOW Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-158. EXT\_VOL1\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_LOW	R/W	0x0	Lower threshold for EXT_VOL1

**7.7.3.36 EXT\_VOL1\_ADC\_OFFSET Register (Address = 0x51) [Default = 0x00]**EXT\_VOL1\_ADC\_OFFSET is shown in [EXT\\_VOL1\\_ADC\\_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-159. EXT\_VOL1\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the vol1 voltage conversion

**7.7.3.37 EXT\_VOL\_MASK Register (Address = 0x52) [Default = 0x00]**EXT\_VOL\_MASK is shown in [EXT\\_VOL\\_MASK Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-160. EXT\_VOL\_MASK Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0x0	
1	EXT_VOL1_THRESH_MSK	R/W	0x0	1 means no interrupt
0	EXT_VOL0_THRESH_MSK	R/W	0x0	1 means no interrupt

**7.7.3.38 LINE\_FAULT0\_THRESH\_0\_HI\_M0 Register (Address = 0x53) [Default = 0xF1]**LINE\_FAULT0\_THRESH\_0\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_0\\_HI\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-161. LINE\_FAULT0\_THRESH\_0\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_HI_M0	R/W	0xF1	Upper threshold 0 for LINE_FAULT0 (Mode0)

**7.7.3.39 LINE\_FAULT0\_THRESH\_0\_LO\_M0 Register (Address = 0x54) [Default = 0xB6]**LINE\_FAULT0\_THRESH\_0\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_0\\_LO\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-162. LINE\_FAULT0\_THRESH\_0\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_LO_M0	R/W	0xB6	Lower threshold 0 for LINE_FAULT0 (Mode0)

**7.7.3.40 LINE\_FAULT0\_THRESH\_1\_HI\_M0 Register (Address = 0x55) [Default = 0xAF]**LINE\_FAULT0\_THRESH\_1\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_1\\_HI\\_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-163. LINE\_FAULT0\_THRESH\_1\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_HI_M0	R/W	0xAF	Upper threshold 1 for LINE_FAULT0 (Mode0)

**7.7.3.41 LINE\_FAULT0\_THRESH\_1\_LO\_M0 Register (Address = 0x56) [Default = 0x7C]**

LINE\_FAULT0\_THRESH\_1\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_1\\_LO\\_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-164. LINE\_FAULT0\_THRESH\_1\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_LO_M0	R/W	0x7C	Lower threshold 1 for LINE_FAULT0 (Mode0)

**7.7.3.42 LINE\_FAULT0\_THRESH\_2\_HI\_M0 Register (Address = 0x57) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_2\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_2\\_HI\\_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-165. LINE\_FAULT0\_THRESH\_2\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT0 (Mode0)

**7.7.3.43 LINE\_FAULT0\_THRESH\_2\_LO\_M0 Register (Address = 0x58) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_2\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_2\\_LO\\_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-166. LINE\_FAULT0\_THRESH\_2\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT0 (Mode0)

**7.7.3.44 LINE\_FAULT0\_THRESH\_3\_HI\_M0 Register (Address = 0x59) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_3\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_3\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-167. LINE\_FAULT0\_THRESH\_3\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT0 (Mode0)

**7.7.3.45 LINE\_FAULT0\_THRESH\_3\_LO\_M0 Register (Address = 0x5A) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_3\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_3\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-168. LINE\_FAULT0\_THRESH\_3\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT0 (Mode0)

**7.7.3.46 LINE\_FAULT0\_THRESH\_4\_HI\_M0 Register (Address = 0x5B) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_4\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_4\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-169. LINE\_FAULT0\_THRESH\_4\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT0 (Mode0)

**7.7.3.47 LINE\_FAULT0\_THRESH\_4\_LO\_M0 Register (Address = 0x5C) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_4\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_4\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-170. LINE\_FAULT0\_THRESH\_4\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT0 (Mode0)

**7.7.3.48 LINE\_FAULT0\_THRESH\_5\_HI\_M0 Register (Address = 0x5D) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_5\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_5\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-171. LINE\_FAULT0\_THRESH\_5\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT0 (Mode0)

**7.7.3.49 LINE\_FAULT0\_THRESH\_5\_LO\_M0 Register (Address = 0x5E) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_5\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_5\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-172. LINE\_FAULT0\_THRESH\_5\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT0 (Mode0)

**7.7.3.50 LINE\_FAULT0\_THRESH\_6\_HI\_M0 Register (Address = 0x5F) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_6\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_6\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-173. LINE\_FAULT0\_THRESH\_6\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT0 (Mode0)

**7.7.3.51 LINE\_FAULT0\_THRESH\_6\_LO\_M0 Register (Address = 0x60) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_6\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_6\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-174. LINE\_FAULT0\_THRESH\_6\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT0 (Mode0)

**7.7.3.52 LINE\_FAULT0\_THRESH\_7\_HI\_M0 Register (Address = 0x61) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_7\_HI\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_7\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-175. LINE\_FAULT0\_THRESH\_7\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT0 (Mode0)

**7.7.3.53 LINE\_FAULT0\_THRESH\_7\_LO\_M0 Register (Address = 0x62) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_7\_LO\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_7\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-176. LINE\_FAULT0\_THRESH\_7\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT0 (Mode0)

**7.7.3.54 LINE\_FAULT0\_THRESH\_MASK\_M0 Register (Address = 0x63) [Default = 0xFC]**

LINE\_FAULT0\_THRESH\_MASK\_M0 is shown in [LINE\\_FAULT0\\_THRESH\\_MASK\\_M0 Register Field Descriptions](#).

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**Table 7-177. LINE\_FAULT0\_THRESH\_MASK\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_FAULT0_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**Table 7-177. LINE\_FAULT0\_THRESH\_MASK\_M0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	LINE_FAULT0_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT0_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
4	LINE_FAULT0_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT0_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT0_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT0_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT0_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**7.7.3.55 LINE\_FAULT0\_ADC\_OFFSET\_M0 Register (Address = 0x64) [Default = 0x00]**LINE\_FAULT0\_ADC\_OFFSET\_M0 is shown in [LINE\\_FAULT0\\_ADC\\_OFFSET\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-178. LINE\_FAULT0\_ADC\_OFFSET\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_ADC_OFFSET_M0	R/W	0x0	ADC offset added to the final ADC code after the LINE_FAULT0 voltage conversion

**7.7.3.56 LINE\_FAULT1\_THRESH\_0\_HI\_M0 Register (Address = 0x65) [Default = 0xF1]**LINE\_FAULT1\_THRESH\_0\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_0\\_HI\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-179. LINE\_FAULT1\_THRESH\_0\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_HI_M0	R/W	0xF1	Upper threshold 0 for LINE_FAULT1 (Mode0)

**7.7.3.57 LINE\_FAULT1\_THRESH\_0\_LO\_M0 Register (Address = 0x66) [Default = 0xB6]**LINE\_FAULT1\_THRESH\_0\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_0\\_LO\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-180. LINE\_FAULT1\_THRESH\_0\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_LO_M0	R/W	0xB6	Lower threshold 0 for LINE_FAULT1 (Mode0)

**7.7.3.58 LINE\_FAULT1\_THRESH\_1\_HI\_M0 Register (Address = 0x67) [Default = 0xAF]**LINE\_FAULT1\_THRESH\_1\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_1\\_HI\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-181. LINE\_FAULT1\_THRESH\_1\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_HI_M0	R/W	0xAF	Upper threshold 1 for LINE_FAULT1 (Mode0)

**7.7.3.59 LINE\_FAULT1\_THRESH\_1\_LO\_M0 Register (Address = 0x68) [Default = 0x7C]**

LINE\_FAULT1\_THRESH\_1\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_1\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-182. LINE\_FAULT1\_THRESH\_1\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_LO_M0	R/W	0x7C	Lower threshold 1 for LINE_FAULT1 (Mode0)

**7.7.3.60 LINE\_FAULT1\_THRESH\_2\_HI\_M0 Register (Address = 0x69) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_2\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_2\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-183. LINE\_FAULT1\_THRESH\_2\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT1 (Mode0)

**7.7.3.61 LINE\_FAULT1\_THRESH\_2\_LO\_M0 Register (Address = 0x6A) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_2\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_2\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-184. LINE\_FAULT1\_THRESH\_2\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT1 (Mode0)

**7.7.3.62 LINE\_FAULT1\_THRESH\_3\_HI\_M0 Register (Address = 0x6B) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_3\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_3\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-185. LINE\_FAULT1\_THRESH\_3\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT1 (Mode0)

**7.7.3.63 LINE\_FAULT1\_THRESH\_3\_LO\_M0 Register (Address = 0x6C) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_3\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_3\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-186. LINE\_FAULT1\_THRESH\_3\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT1 (Mode0)

**7.7.3.64 LINE\_FAULT1\_THRESH\_4\_HI\_M0 Register (Address = 0x6D) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_4\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_4\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-187. LINE\_FAULT1\_THRESH\_4\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT1 (Mode0)

**7.7.3.65 LINE\_FAULT1\_THRESH\_4\_LO\_M0 Register (Address = 0x6E) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_4\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_4\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-188. LINE\_FAULT1\_THRESH\_4\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT1 (Mode0)

**7.7.3.66 LINE\_FAULT1\_THRESH\_5\_HI\_M0 Register (Address = 0x6F) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_5\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_5\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-189. LINE\_FAULT1\_THRESH\_5\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT1 (Mode0)

**7.7.3.67 LINE\_FAULT1\_THRESH\_5\_LO\_M0 Register (Address = 0x70) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_5\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_5\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-190. LINE\_FAULT1\_THRESH\_5\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT1 (Mode0)

**7.7.3.68 LINE\_FAULT1\_THRESH\_6\_HI\_M0 Register (Address = 0x71) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_6\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_6\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-191. LINE\_FAULT1\_THRESH\_6\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT1 (Mode0)

**7.7.3.69 LINE\_FAULT1\_THRESH\_6\_LO\_M0 Register (Address = 0x72) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_6\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_6\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-192. LINE\_FAULT1\_THRESH\_6\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT1 (Mode0)

**7.7.3.70 LINE\_FAULT1\_THRESH\_7\_HI\_M0 Register (Address = 0x73) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_7\_HI\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_7\\_HI\\_M0 Register Field Descriptions](#).

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**Table 7-193. LINE\_FAULT1\_THRESH\_7\_HI\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT1 (Mode0)

**7.7.3.71 LINE\_FAULT1\_THRESH\_7\_LO\_M0 Register (Address = 0x74) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_7\_LO\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_7\\_LO\\_M0 Register Field Descriptions](#).

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**Table 7-194. LINE\_FAULT1\_THRESH\_7\_LO\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT1 (Mode0)

**7.7.3.72 LINE\_FAULT1\_THRESH\_MASK\_M0 Register (Address = 0x75) [Default = 0xFC]**

LINE\_FAULT1\_THRESH\_MASK\_M0 is shown in [LINE\\_FAULT1\\_THRESH\\_MASK\\_M0 Register Field Descriptions](#).

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**Table 7-195. LINE\_FAULT1\_THRESH\_MASK\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_FAULT1_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT1_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT1_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**Table 7-195. LINE\_FAULT1\_THRESH\_MASK\_M0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	LINE_FAULT1_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT1_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT1_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT1_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT1_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**7.7.3.73 LINE\_FAULT1\_ADC\_OFFSET\_M0 Register (Address = 0x76) [Default = 0x00]**LINE\_FAULT1\_ADC\_OFFSET\_M0 is shown in [LINE\\_FAULT1\\_ADC\\_OFFSET\\_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-196. LINE\_FAULT1\_ADC\_OFFSET\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_ADC_OFF_SET_M0	R/W	0x0	ADC offset added to the final ADC code after the LINE_FAULT 1 voltage conversion

**7.7.3.74 LINE\_FAULT0\_THRESH\_0\_HI\_M1 Register (Address = 0x9B) [Default = 0x00]**LINE\_FAULT0\_THRESH\_0\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_0\\_HI\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-197. LINE\_FAULT0\_THRESH\_0\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_HI_M1	R/W	0x0	Upper threshold 0 for LINE_FAULT0 (Mode1)

**7.7.3.75 LINE\_FAULT0\_THRESH\_0\_LO\_M1 Register (Address = 0x9C) [Default = 0x00]**LINE\_FAULT0\_THRESH\_0\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_0\\_LO\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-198. LINE\_FAULT0\_THRESH\_0\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_LO_M1	R/W	0x0	Lower threshold 0 for LINE_FAULT0 (Mode1)

**7.7.3.76 LINE\_FAULT0\_THRESH\_1\_HI\_M1 Register (Address = 0x9D) [Default = 0x00]**LINE\_FAULT0\_THRESH\_1\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_1\\_HI\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-199. LINE\_FAULT0\_THRESH\_1\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_HI_M1	R/W	0x0	Upper threshold 1 for LINE_FAULT0 (Mode1)

**7.7.3.77 LINE\_FAULT0\_THRESH\_1\_LO\_M1 Register (Address = 0x9E) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_1\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_1\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-200. LINE\_FAULT0\_THRESH\_1\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_LO_M1	R/W	0x0	Lower threshold 1 for LINE_FAULT0 (Mode1)

**7.7.3.78 LINE\_FAULT0\_THRESH\_2\_HI\_M1 Register (Address = 0x9F) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_2\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_2\\_HI\\_M1 Register Field Descriptions](#).

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**Table 7-201. LINE\_FAULT0\_THRESH\_2\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_HI_M1	R/W	0x0	Upper threshold 2 for LINE_FAULT0 (Mode1)

**7.7.3.79 LINE\_FAULT0\_THRESH\_2\_LO\_M1 Register (Address = 0xA0) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_2\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_2\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-202. LINE\_FAULT0\_THRESH\_2\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_LO_M1	R/W	0x0	Lower threshold 2 for LINE_FAULT0 (Mode1)

**7.7.3.80 LINE\_FAULT0\_THRESH\_3\_HI\_M1 Register (Address = 0xA1) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_3\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_3\\_HI\\_M1 Register Field Descriptions](#).

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**Table 7-203. LINE\_FAULT0\_THRESH\_3\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_HI_M1	R/W	0x0	Upper threshold 3 for LINE_FAULT0 (Mode1)

**7.7.3.81 LINE\_FAULT0\_THRESH\_3\_LO\_M1 Register (Address = 0xA2) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_3\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_3\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-204. LINE\_FAULT0\_THRESH\_3\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_LO_M1	R/W	0x0	Lower threshold 3 for LINE_FAULT0 (Mode1)

**7.7.3.82 LINE\_FAULT0\_THRESH\_4\_HI\_M1 Register (Address = 0xA3) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_4\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_4\\_HI\\_M1 Register Field Descriptions](#).

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**Table 7-205. LINE\_FAULT0\_THRESH\_4\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_HI_M1	R/W	0x0	Upper threshold 4 for LINE_FAULT0 (Mode1)

**7.7.3.83 LINE\_FAULT0\_THRESH\_4\_LO\_M1 Register (Address = 0xA4) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_4\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_4\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-206. LINE\_FAULT0\_THRESH\_4\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_LO_M1	R/W	0x0	Lower threshold 4 for LINE_FAULT0 (Mode1)

**7.7.3.84 LINE\_FAULT0\_THRESH\_5\_HI\_M1 Register (Address = 0xA5) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_5\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_5\\_HI\\_M1 Register Field Descriptions](#).

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**Table 7-207. LINE\_FAULT0\_THRESH\_5\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for LINE_FAULT0 (Mode1)

**7.7.3.85 LINE\_FAULT0\_THRESH\_5\_LO\_M1 Register (Address = 0xA6) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_5\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_5\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-208. LINE\_FAULT0\_THRESH\_5\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for LINE_FAULT0 (Mode1)

**7.7.3.86 LINE\_FAULT0\_THRESH\_6\_HI\_M1 Register (Address = 0xA7) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_6\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_6\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-209. LINE\_FAULT0\_THRESH\_6\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for LINE_FAULT0 (Mode1)

**7.7.3.87 LINE\_FAULT0\_THRESH\_6\_LO\_M1 Register (Address = 0xA8) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_6\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_6\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-210. LINE\_FAULT0\_THRESH\_6\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for LINE_FAULT0 (Mode1)

**7.7.3.88 LINE\_FAULT0\_THRESH\_7\_HI\_M1 Register (Address = 0xA9) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_7\_HI\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_7\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-211. LINE\_FAULT0\_THRESH\_7\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for LINE_FAULT0 (Mode1)

**7.7.3.89 LINE\_FAULT0\_THRESH\_7\_LO\_M1 Register (Address = 0xAA) [Default = 0x00]**

LINE\_FAULT0\_THRESH\_7\_LO\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_7\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-212. LINE\_FAULT0\_THRESH\_7\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for LINE_FAULT0 (Mode1)

**7.7.3.90 LINE\_FAULT0\_THRESH\_MASK\_M1 Register (Address = 0xAB) [Default = 0xFF]**

LINE\_FAULT0\_THRESH\_MASK\_M1 is shown in [LINE\\_FAULT0\\_THRESH\\_MASK\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-213. LINE\_FAULT0\_THRESH\_MASK\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_FAULT0_THRESH_7_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT0_THRESH_6_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT0_THRESH_5_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**Table 7-213. LINE\_FAULT0\_THRESH\_MASK\_M1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	LINE_FAULT0_THRESH_4_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT0_THRESH_3_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT0_THRESH_2_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT0_THRESH_1_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT0_THRESH_0_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**7.7.3.91 LINE\_FAULT0\_ADC\_OFFSET\_M1 Register (Address = 0xAC) [Default = 0x00]**LINE\_FAULT0\_ADC\_OFFSET\_M1 is shown in [LINE\\_FAULT0\\_ADC\\_OFFSET\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-214. LINE\_FAULT0\_ADC\_OFFSET\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_ADC_OFF_SET_M1	R/W	0x0	ADC offset added to the final ADC code after the LINE_FAULT0 voltage conversion

**7.7.3.92 LINE\_FAULT1\_THRESH\_0\_HI\_M1 Register (Address = 0xAD) [Default = 0x00]**LINE\_FAULT1\_THRESH\_0\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_0\\_HI\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-215. LINE\_FAULT1\_THRESH\_0\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_HI_M1	R/W	0x0	Upper threshold 0 for LINE_FAULT1 (Mode1)

**7.7.3.93 LINE\_FAULT1\_THRESH\_0\_LO\_M1 Register (Address = 0xAE) [Default = 0x00]**LINE\_FAULT1\_THRESH\_0\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_0\\_LO\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-216. LINE\_FAULT1\_THRESH\_0\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_LO_M1	R/W	0x0	Lower threshold 0 for LINE_FAULT1 (Mode1)

**7.7.3.94 LINE\_FAULT1\_THRESH\_1\_HI\_M1 Register (Address = 0xAF) [Default = 0x00]**LINE\_FAULT1\_THRESH\_1\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_1\\_HI\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).

**Table 7-217. LINE\_FAULT1\_THRESH\_1\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_HI_M1	R/W	0x0	Upper threshold 1 for LINE_FAULT1 (Mode1)

**7.7.3.95 LINE\_FAULT1\_THRESH\_1\_LO\_M1 Register (Address = 0xB0) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_1\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_1\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-218. LINE\_FAULT1\_THRESH\_1\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_LO_M1	R/W	0x0	Lower threshold 1 for LINE_FAULT1 (Mode1)

**7.7.3.96 LINE\_FAULT1\_THRESH\_2\_HI\_M1 Register (Address = 0xB1) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_2\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_2\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-219. LINE\_FAULT1\_THRESH\_2\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_HI_M1	R/W	0x0	Upper threshold 2 for LINE_FAULT1 (Mode1)

**7.7.3.97 LINE\_FAULT1\_THRESH\_2\_LO\_M1 Register (Address = 0xB2) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_2\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_2\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-220. LINE\_FAULT1\_THRESH\_2\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_LO_M1	R/W	0x0	Lower threshold 2 for LINE_FAULT1 (Mode1)

**7.7.3.98 LINE\_FAULT1\_THRESH\_3\_HI\_M1 Register (Address = 0xB3) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_3\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_3\\_HI\\_M1 Register Field Descriptions](#).

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**Table 7-221. LINE\_FAULT1\_THRESH\_3\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_HI_M1	R/W	0x0	Upper threshold 3 for LINE_FAULT1 (Mode1)

**7.7.3.99 LINE\_FAULT1\_THRESH\_3\_LO\_M1 Register (Address = 0xB4) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_3\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_3\\_LO\\_M1 Register Field Descriptions](#).

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**Table 7-222. LINE\_FAULT1\_THRESH\_3\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_LO_M1	R/W	0x0	Lower threshold 3 for LINE_FAULT1 (Mode1)

**7.7.3.100 LINE\_FAULT1\_THRESH\_4\_HI\_M1 Register (Address = 0xB5) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_4\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_4\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-223. LINE\_FAULT1\_THRESH\_4\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_HI_M1	R/W	0x0	Upper threshold 4 for LINE_FAULT1 (Mode1)

**7.7.3.101 LINE\_FAULT1\_THRESH\_4\_LO\_M1 Register (Address = 0xB6) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_4\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_4\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-224. LINE\_FAULT1\_THRESH\_4\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_LO_M1	R/W	0x0	Lower threshold 4 for LINE_FAULT1 (Mode1)

**7.7.3.102 LINE\_FAULT1\_THRESH\_5\_HI\_M1 Register (Address = 0xB7) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_5\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_5\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-225. LINE\_FAULT1\_THRESH\_5\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_HI_M1	R/W	0x0	Upper threshold 5 for LINE_FAULT1 (Mode1)

**7.7.3.103 LINE\_FAULT1\_THRESH\_5\_LO\_M1 Register (Address = 0xB8) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_5\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_5\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-226. LINE\_FAULT1\_THRESH\_5\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_LO_M1	R/W	0x0	Lower threshold 5 for LINE_FAULT1 (Mode1)

**7.7.3.104 LINE\_FAULT1\_THRESH\_6\_HI\_M1 Register (Address = 0xB9) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_6\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_6\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-227. LINE\_FAULT1\_THRESH\_6\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_HI_M1	R/W	0x0	Upper threshold 6 for LINE_FAULT1 (Mode1)

**7.7.3.105 LINE\_FAULT1\_THRESH\_6\_LO\_M1 Register (Address = 0xBA) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_6\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_6\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-228. LINE\_FAULT1\_THRESH\_6\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_LO_M1	R/W	0x0	Lower threshold 6 for LINE_FAULT1 (Mode1)

**7.7.3.106 LINE\_FAULT1\_THRESH\_7\_HI\_M1 Register (Address = 0xBB) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_7\_HI\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_7\\_HI\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-229. LINE\_FAULT1\_THRESH\_7\_HI\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_HI_M1	R/W	0x0	Upper threshold 7 for LINE_FAULT1 (Mode1)

**7.7.3.107 LINE\_FAULT1\_THRESH\_7\_LO\_M1 Register (Address = 0xBC) [Default = 0x00]**

LINE\_FAULT1\_THRESH\_7\_LO\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_7\\_LO\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-230. LINE\_FAULT1\_THRESH\_7\_LO\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_LO_M1	R/W	0x0	Lower threshold 7 for LINE_FAULT1 (Mode1)

**7.7.3.108 LINE\_FAULT1\_THRESH\_MASK\_M1 Register (Address = 0xBD) [Default = 0xFF]**

LINE\_FAULT1\_THRESH\_MASK\_M1 is shown in [LINE\\_FAULT1\\_THRESH\\_MASK\\_M1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-231. LINE\_FAULT1\_THRESH\_MASK\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_FAULT1_THRESH_7_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT1_THRESH_6_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT1_THRESH_5_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**Table 7-231. LINE\_FAULT1\_THRESH\_MASK\_M1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	LINE_FAULT1_THRESH_4_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT1_THRESH_3_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT1_THRESH_2_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT1_THRESH_1_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT1_THRESH_0_MASK_M1	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

**7.7.3.109 LINE\_FAULT1\_ADC\_OFFSET\_M1 Register (Address = 0xBE) [Default = 0x00]**LINE\_FAULT1\_ADC\_OFFSET\_M1 is shown in [LINE\\_FAULT1\\_ADC\\_OFFSET\\_M1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-232. LINE\_FAULT1\_ADC\_OFFSET\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_ADC_OFFSET_M1	R/W	0x0	ADC offset added to the final ADC code after the LINE_FAULT1 voltage conversion

**7.7.3.110 LINE\_FAULT0\_11\_PD\_SEL Register (Address = 0xE3) [Default = 0x00]**LINE\_FAULT0\_11\_PD\_SEL is shown in [LINE\\_FAULT0\\_11\\_PD\\_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-233. LINE\_FAULT0\_11\_PD\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	LINE_FAULT1_PD_SEL	R/W	0x0	Configure Pull down for GPIO 0 - 3 if ADC source is GPIO 1 Bit 3 - RESERVED Bit 2 - RESERVED Bit 1 - GPIO 1 Bit 0 - GPIO 0 Set bit to 0 to disable pull down Set bit to 1 to enable pull down
3-0	LINE_FAULT0_PD_SEL	R/W	0x0	Configure Pull down for GPIO 0 - 3 if ADC source is GPIO 0 Bit 3 - RESERVED Bit 2 - RESERVED Bit 1 - GPIO 1 Bit 0 - GPIO 0 Set bit to 0 to disable pull down Set bit to 1 to enable pull down

**7.7.3.111 ADC\_OFFSET\_POL0 Register (Address = 0xE5) [Default = 0x00]**ADC\_OFFSET\_POL0 is shown in [ADC\\_OFFSET\\_POL0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-234. ADC\_OFFSET\_POL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

**Table 7-234. ADC\_OFFSET\_POL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	RESERVED	R/W	0x0	Reserved
3	IV1_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
2	IV0_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
1	RESERVED	R/W	0x0	Reserved
0	TEMP_ADC_OFFSET_P OL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative

**7.7.3.112 ADC\_OFFSET\_POL1 Register (Address = 0xE6) [Default = 0x00]**ADC\_OFFSET\_POL1 is shown in [ADC\\_OFFSET\\_POL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-235. ADC\_OFFSET\_POL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0x0	
1	EXT_VOL1_ADC_OFFSET T_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
0	EXT_VOL0_ADC_OFFSET T_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative

**7.7.3.113 ADC\_OFFSET\_POL2 Register (Address = 0xE7) [Default = 0x00]**ADC\_OFFSET\_POL2 is shown in [ADC\\_OFFSET\\_POL2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-236. ADC\_OFFSET\_POL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	LINE_FAULT1_M1_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
2	LINE_FAULT1_M0_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
1	LINE_FAULT0_M1_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative
0	LINE_FAULT0_M0_ADC_OFFSET_POL	R/W	0x0	The sign of the added offset, 0: positive, 1: negative

### 7.7.4 DIE\_ID Registers

[DIE\\_ID Registers](#) lists the memory-mapped registers for the DIE\_ID registers. All register offset addresses not listed in [DIE\\_ID Registers](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-237. DIE\_ID Registers**

Address	Acronym	Register Name	Section
0x0	UNIQUE_ID_0	UNIQUE_ID_0	Go
0x1	UNIQUE_ID_1	UNIQUE_ID_1	Go
0x2	UNIQUE_ID_2	UNIQUE_ID_2	Go
0x3	UNIQUE_ID_3	UNIQUE_ID_3	Go
0x4	UNIQUE_ID_4	UNIQUE_ID_4	Go
0x5	UNIQUE_ID_5	UNIQUE_ID_5	Go
0x6	UNIQUE_ID_6	UNIQUE_ID_6	Go
0x7	UNIQUE_ID_7	UNIQUE_ID_7	Go
0x8	UNIQUE_ID_8	UNIQUE_ID_8	Go
0x9	UNIQUE_ID_9	UNIQUE_ID_9	Go
0x10	UNIQUE_ID_10	UNIQUE_ID_10	Go
0x11	UNIQUE_ID_11	UNIQUE_ID_11	Go
0x12	UNIQUE_ID_12	UNIQUE_ID_12	Go
0x13	UNIQUE_ID_13	UNIQUE_ID_13	Go
0x14	UNIQUE_ID_14	UNIQUE_ID_14	Go
0x15	UNIQUE_ID_15	UNIQUE_ID_15	Go

#### 7.7.4.1 UNIQUE\_ID\_0 Register (Address = 0x0) [Default = 0x00]

UNIQUE\_ID\_0 is shown in [UNIQUE\\_ID\\_0 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-238. UNIQUE\_ID\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_0	R	0x0	Unique DIE ID byte 0

#### 7.7.4.2 UNIQUE\_ID\_1 Register (Address = 0x1) [Default = 0x00]

UNIQUE\_ID\_1 is shown in [UNIQUE\\_ID\\_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-239. UNIQUE\_ID\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_1	R	0x0	Unique DIE ID byte 1

#### 7.7.4.3 UNIQUE\_ID\_2 Register (Address = 0x2) [Default = 0x00]

UNIQUE\_ID\_2 is shown in [UNIQUE\\_ID\\_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-240. UNIQUE\_ID\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_2	R	0x0	Unique DIE ID byte 2

**7.7.4.4 UNIQUE\_ID\_3 Register (Address = 0x3) [Default = 0x00]**UNIQUE\_ID\_3 is shown in [UNIQUE\\_ID\\_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-241. UNIQUE\_ID\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_3	R	0x0	Unique DIE ID byte 3

**7.7.4.5 UNIQUE\_ID\_4 Register (Address = 0x4) [Default = 0x00]**UNIQUE\_ID\_4 is shown in [UNIQUE\\_ID\\_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-242. UNIQUE\_ID\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_4	R	0x0	Unique DIE ID byte 4

**7.7.4.6 UNIQUE\_ID\_5 Register (Address = 0x5) [Default = 0x00]**UNIQUE\_ID\_5 is shown in [UNIQUE\\_ID\\_5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-243. UNIQUE\_ID\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_5	R	0x0	Unique DIE ID byte 5

**7.7.4.7 UNIQUE\_ID\_6 Register (Address = 0x6) [Default = 0x00]**UNIQUE\_ID\_6 is shown in [UNIQUE\\_ID\\_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-244. UNIQUE\_ID\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_6	R	0x0	Unique DIE ID byte 6

**7.7.4.8 UNIQUE\_ID\_7 Register (Address = 0x7) [Default = 0x00]**UNIQUE\_ID\_7 is shown in [UNIQUE\\_ID\\_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-245. UNIQUE\_ID\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_7	R	0x0	Unique DIE ID byte 7

**7.7.4.9 UNIQUE\_ID\_8 Register (Address = 0x8) [Default = 0x00]**

UNIQUE\_ID\_8 is shown in [UNIQUE\\_ID\\_8 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-246. UNIQUE\_ID\_8 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_8	R	0x0	Unique DIE ID byte 8

**7.7.4.10 UNIQUE\_ID\_9 Register (Address = 0x9) [Default = 0x00]**

UNIQUE\_ID\_9 is shown in [UNIQUE\\_ID\\_9 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-247. UNIQUE\_ID\_9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_9	R	0x0	Unique DIE ID byte 9

**7.7.4.11 UNIQUE\_ID\_10 Register (Address = 0x10) [Default = 0x00]**

UNIQUE\_ID\_10 is shown in [UNIQUE\\_ID\\_10 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-248. UNIQUE\_ID\_10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_10	R	0x0	Unique DIE ID byte 10

**7.7.4.12 UNIQUE\_ID\_11 Register (Address = 0x11) [Default = 0x00]**

UNIQUE\_ID\_11 is shown in [UNIQUE\\_ID\\_11 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-249. UNIQUE\_ID\_11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_11	R	0x0	Unique DIE ID byte 11

**7.7.4.13 UNIQUE\_ID\_12 Register (Address = 0x12) [Default = 0x00]**

UNIQUE\_ID\_12 is shown in [UNIQUE\\_ID\\_12 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-250. UNIQUE\_ID\_12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_12	R	0x0	Unique DIE ID byte 12

**7.7.4.14 UNIQUE\_ID\_13 Register (Address = 0x13) [Default = 0x00]**

UNIQUE\_ID\_13 is shown in [UNIQUE\\_ID\\_13 Register Field Descriptions](#).

Return to the [Summary Table](#).

**Table 7-251. UNIQUE\_ID\_13 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_13	R	0x0	Unique DIE ID byte 13

**7.7.4.15 UNIQUE\_ID\_14 Register (Address = 0x14) [Default = 0x00]**UNIQUE\_ID\_14 is shown in [UNIQUE\\_ID\\_14 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-252. UNIQUE\_ID\_14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_14	R	0x0	Unique DIE ID byte 14

**7.7.4.16 UNIQUE\_ID\_15 Register (Address = 0x15) [Default = 0x00]**UNIQUE\_ID\_15 is shown in [UNIQUE\\_ID\\_15 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 7-253. UNIQUE\_ID\_15 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_15	R	0x0	Unique DIE ID byte 15

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

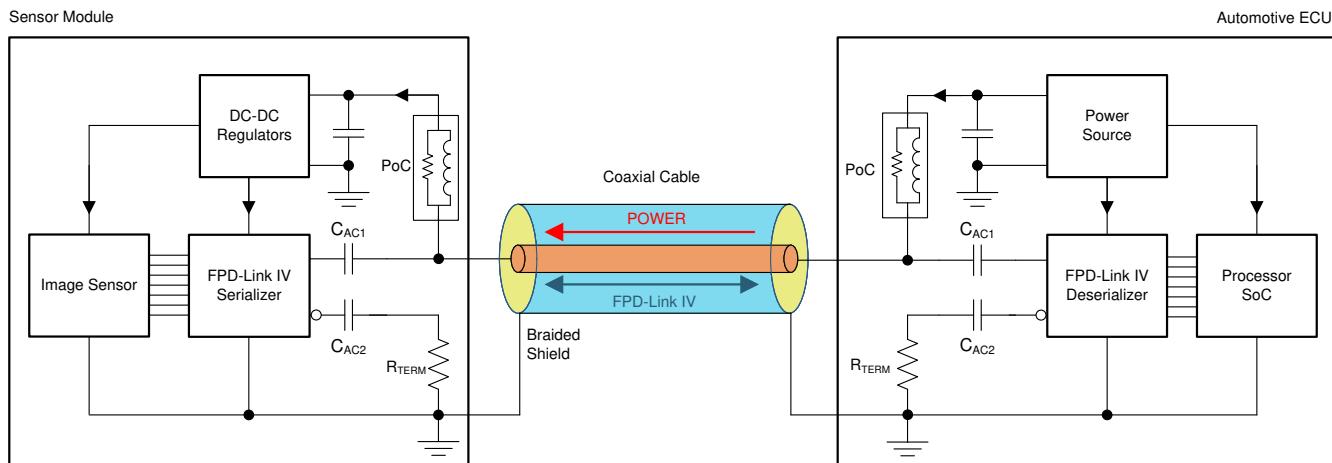
#### 8.1.1 System

For these two communications links to operate properly, the circuit between the serializer and the deserializer must present a characteristic impedance of  $50\ \Omega$ . Deviations from this  $50\ \Omega$  characteristic will lead to signal reflections either at the serializer or deserializer, which will result in bit errors.

The link between the DS90UB971-Q1 and the companion deserializer has two distinct data paths: a forward channel which is nominally running at up to 7.55 Gbps, and is encoded such that it occupies a bandwidth up to 3.775 GHz, and a back channel from the deserializer to the serializer which occupies a frequency range up to 52 MHz.

#### 8.1.2 Power Over Coax

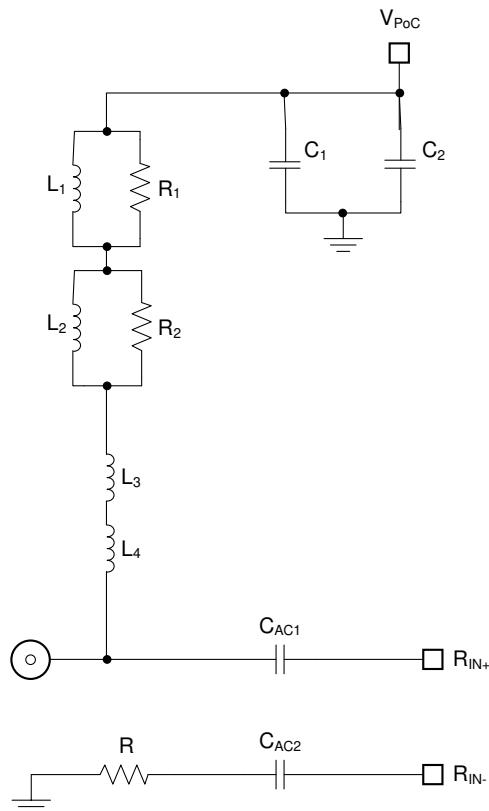
The DS90UB971-Q1 is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data and bi-directional control and diagnostics data transmission. The method uses passive networks or filters that isolate the transmission line from the loading of the DC-DC regulator circuits and their connecting power traces on both sides of the link as shown in [Figure 8-1](#).



**Figure 8-1. Power-over-Coax (PoC) System Diagram**

The PoC networks' impedance of  $\geq 2\ k\Omega$  over a specific frequency band is typically sufficient to isolate the transmission line from the loading of the regulator circuits. The lower limit of the frequency band is defined as  $\frac{1}{2}$  of the bidirectional control channel's frequency,  $f_{BCC}$ . The upper limit of the frequency band is the frequency of the forward high-speed channel,  $f_{FC}$ .

[Figure 8-2](#) shows an example of a PoC network suitable for FPD-Link IV consisting of DS90UB971-Q1, DS90UB9702-Q1, DS90UB9722-Q1 rated for up to 300mA of DC current. This network is also suitable for "4G" FPD-LINK III deserializers consisting of DS90UB936-Q1, DS90UB954-Q1, DS90UB962-Q1 or DS90UB960-Q1. The bi-directional channel is operating at 47.1875 Mbps and the forward channel operating at 7.55 Gbps ( $f_{FC} \approx 3.775\ GHz$ ). Other PoC networks are possible and may be different on the serializer and the deserializer boards as long as the PCB board return loss requirements given in are met.



**Figure 8-2. Preliminary Typical PoC Network for a "8G" FPD-Link IV**

Table 8-1 lists essential components for this particular PoC network.

**Table 8-1. Suggested Components for a "8G" FPD-Link IV PoC Network**

Ref Des	Description	Part Number	MFR
L1	Inductor, 100uH, 1400mΩ DCR, 450mA	LPS4018-104	Coilcraft
L2	Inductor, 6.8uH, 360mΩ DCR, 390mA	1205POC-682	Coilcraft
L3	Inductor, 180 nH, 210mΩ DCR, 900mA	PFL1005-181	Coilcraft
L4			
R1	2.61kΩ		
R2	3.6kΩ		

In addition to the PoC network components selection, their placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of its pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the through-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.
- Use coupled 100-Ω differential signal traces from the device pins to the ac-coupling caps. Use 50-Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9-Ω resistors.

The V<sub>POC</sub> fluctuations on the serializer side, caused by the sensor's transient current draw and the DC resistance of cables and PoC components, need to be kept at minimum as well. Increasing the V<sub>POC</sub> voltage and adding extra decoupling capacitance (> 10 µF) help reduce the amplitude and slew rate of the V<sub>POC</sub> fluctuations.

Please contact Texas Instruments for additional information regarding PoC network recommendations.

## 8.2 Typical Application

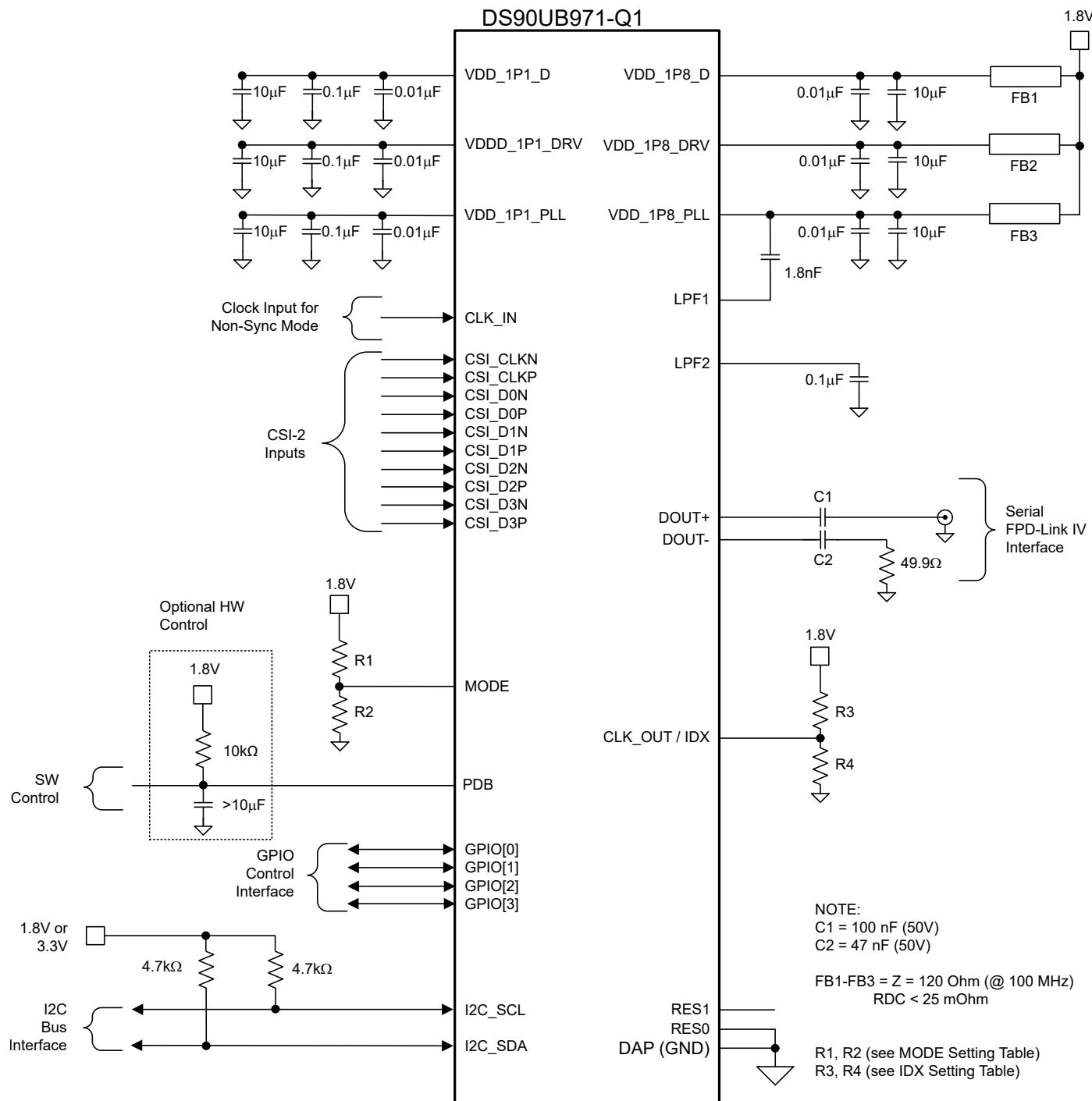
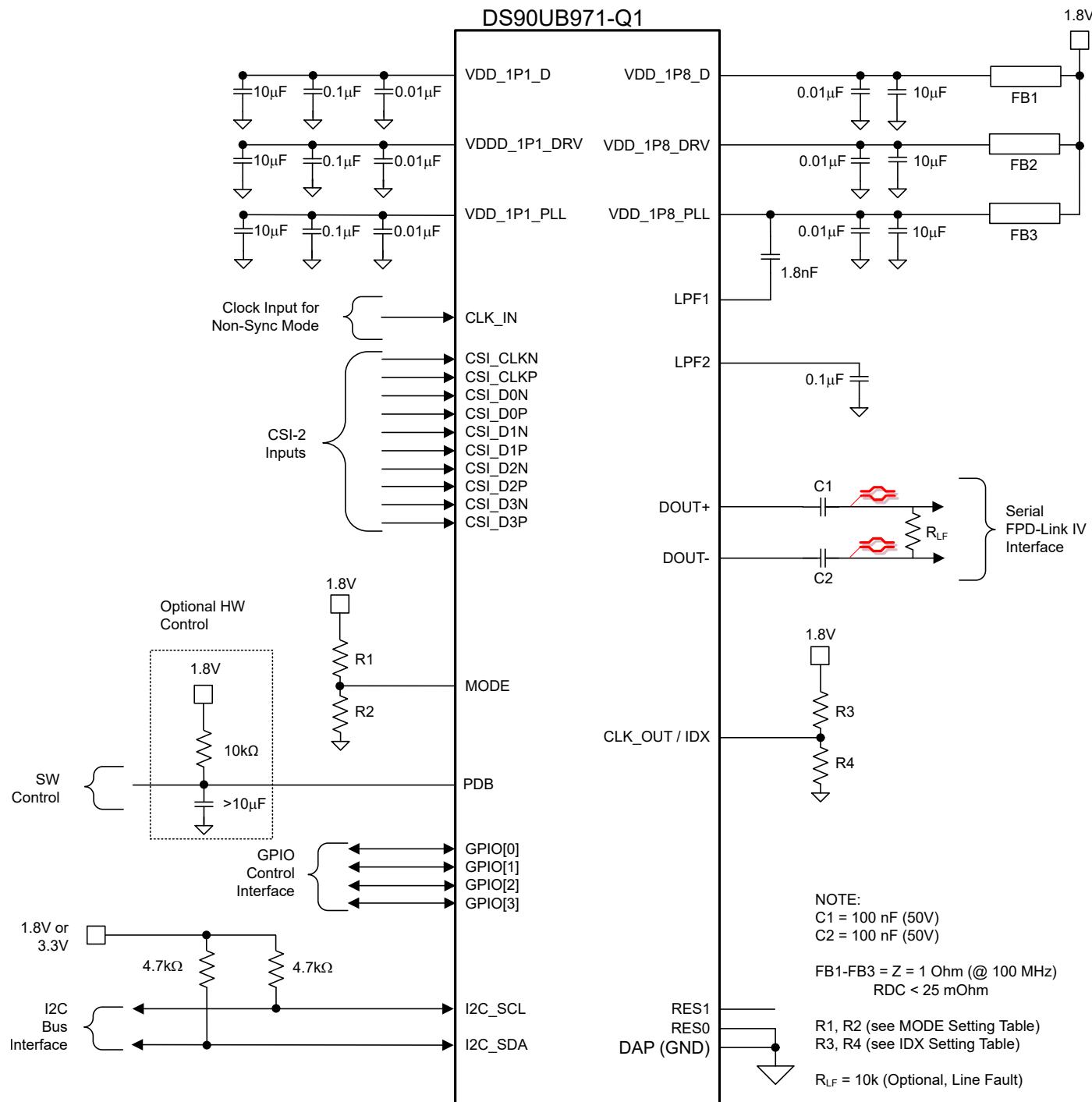


Figure 8-3. Typical Connection Diagram Coaxial

**DS90UB971-Q1**

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**Figure 8-4. Typical Connection Diagram STP**

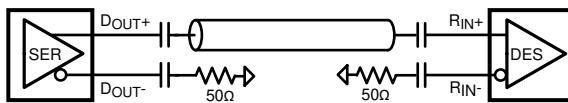
### 8.2.1 Design Requirements

For the typical design application, use the parameters listed in [Table 8-2](#).

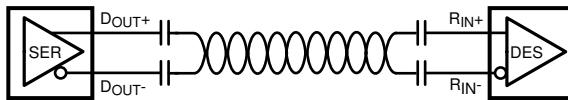
**Table 8-2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
V <sub>V(VDD)</sub>	1.8 V
AC-Coupling Capacitor for Coaxial Mode: DOUT+	100 nF (50 V / X7R / 0402)
AC-Coupling Capacitor for Coaxial Synchronous Mode: DOUT-	47 nF (50 V / X7R / 0402)
AC-Coupling Capacitor for STP Non-Synchronous Mode: DOUT+, DOUT-	100 nF (50 V / X7R / 0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link IV signal path as shown in [Figure 8-5](#) and [Figure 8-6](#). For applications using single-ended 50-Ω coaxial cable, terminate the unused data pins (DOUT+, DOUT-) with an AC-coupling capacitor and a 50-Ω resistor.



**Figure 8-5. AC-Coupled Connection (Coaxial)**



**Figure 8-6. AC-Coupled Connection (STP)**

For high-speed FPD-Link IV transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

### 8.2.2 Oscillator Requirements

Whether operating in non synchronous clocking mode, please see the table below to check the oscillator requirements.

**Table 8-3. DS90UB971-Q1 Oscillator Requirements for Asynchronous Operation**

Parameter	Test Conditions	Min	Typ	Max	Unit
Frequency Tolerance	-40°C to 115°C	-50		50	ppm
Frequency Stability	Aging	-50		50	ppm
Duty Cycle		40	50	60	%
Rise/Fall Time	20% - 80%	0.1		3	ns @ 15 pF loading
Jitter	12 kHz to 20 MHz			200	ps pk-pk
Frequency	FPD-Link IV		25		MHz
	FPD-Link III		26		MHz

\* In non synchronous mode, the ppm tolerance will be applied to the whole system (DS90UB971-Q1 oscillator + paired device oscillator). Non Synchronous mode does not support SSC.

### 8.2.3 Detailed Design Procedure

[Section 8.2](#) shows a typical application circuit of the DS90UB971-Q1. The next sections highlight recommendations for the critical device pins.

#### 8.2.3.1 CSI-2 Interface

The CSI-2 input port on the DS90UB971-Q1 is compliant with the MIPI DPHY v2.1 and CSI-2 v2.1 specifications. The CSI-2 interface consists of a clock and an option of one, two, or four data lanes. The clock and each of the data lanes are differential lines. The DS90UB971-Q1 CSI-2 input needs to be DC coupled to a compatible CSI-2 transmitter.

#### 8.2.3.2 FPD-Link IV Input / Output

The DS90UB971-Q1 serial data out signal operates at different data rates depending upon the mode in which the device is operating. In synchronous mode, where the reference clock is provided by the deserializer, the serial data rate is up to 7.55 Gbps.

The signals at DOUT+ and DOUT- must be AC-coupled. The AC-coupling capacitor is 100 nF when the device is running in synchronous mode. When connecting to a coax cable, the AC-coupling capacitor on the negative terminal (DOUT-) should also have an AC-coupling capacitor at a value of approximately  $\frac{1}{2}$  of the AC-coupling capacitor and terminated to a  $50\text{-}\Omega$  load. Adhering to the PCB layout guidelines given in [Section 10.2](#) is critical.

#### 8.2.3.3 External Regulator Bypassing

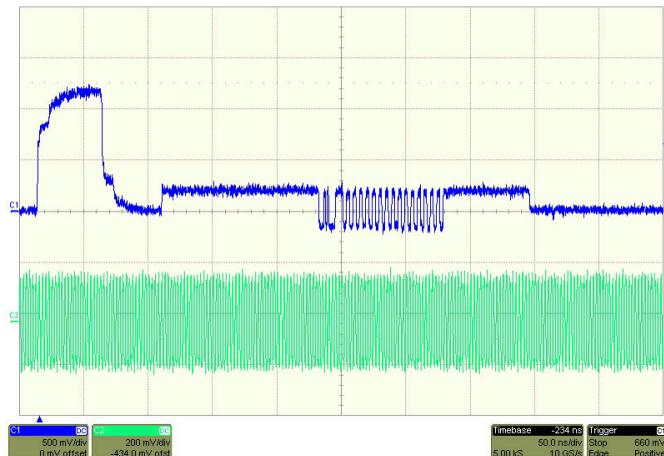
The DSUB90UB971-Q1 features internal regulators that must be bypassed to GND. The VDD\_1P1\_D, VDD\_1P1\_DRV, and VDD\_1P1\_PLL are the pins that expose the outputs of the internal regulators for bypassing. TI recommends that each pin have a 10- $\mu\text{F}$ , 0.1- $\mu\text{F}$ , and a 0.01- $\mu\text{F}$  capacitor to GND. The 0.01- $\mu\text{F}$  caps must be placed as close as practical to the bypass pins.

#### 8.2.3.4 Loop Filter Decoupling

The LPF1 and LPF2 pins are for connecting filter capacitors to the internal PLL circuits. LPF1 should have a 1.8nF capacitor connected to the VDD\_1P8\_\_PLL pin (pin 11). The capacitor connected between LPF1 and VDD\_1P8\_PLL must enclose as small of a loop as possible. LPF2 must have a 0.1- $\mu\text{F}$  capacitor connecting the pin to GND. One of these PLLs generates the high-speed clock used in the serialization of the output, while the other PLL is used in the CSI-2 receive port. Noise coupled into these pins degrades the performance of the PLLs in the DS90UB971-Q1, so the caps must be placed close to the pins that they are connected to, and the area of the loop enclosed must be minimized.

### 8.2.4 Application Curve

The falling edge of the blue trace indicates that the device should shift from LP to HS mode – the rise that comes about one division later is when the DS90UB971-Q1 turns on its internal termination and is ready to receive HS data. The transitions are the CSI-2 data, and then the drop of the blue trace indicates that the termination has been turned off.

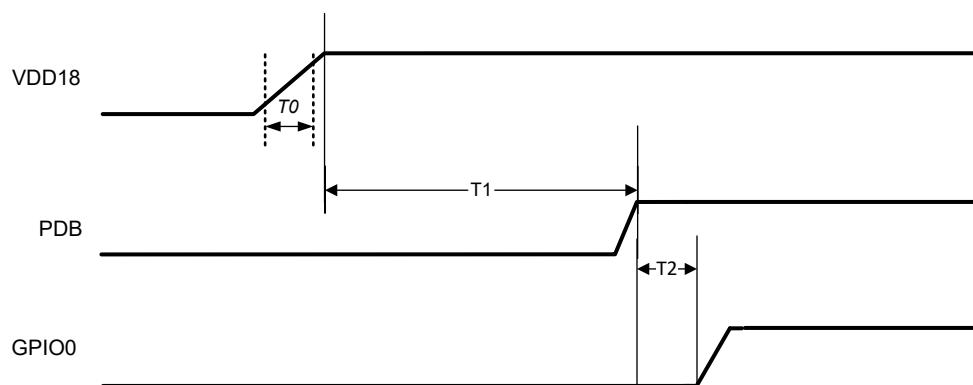
**Figure 8-7. CSI-2 LP to HS Mode Transition**

## 9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The Pin Functions section provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

### 9.1 Power-Up Sequencing

The power-up sequence for the DS90UB971-Q1 is as follows:



**Figure 9-1. Power Supply Sequencing**

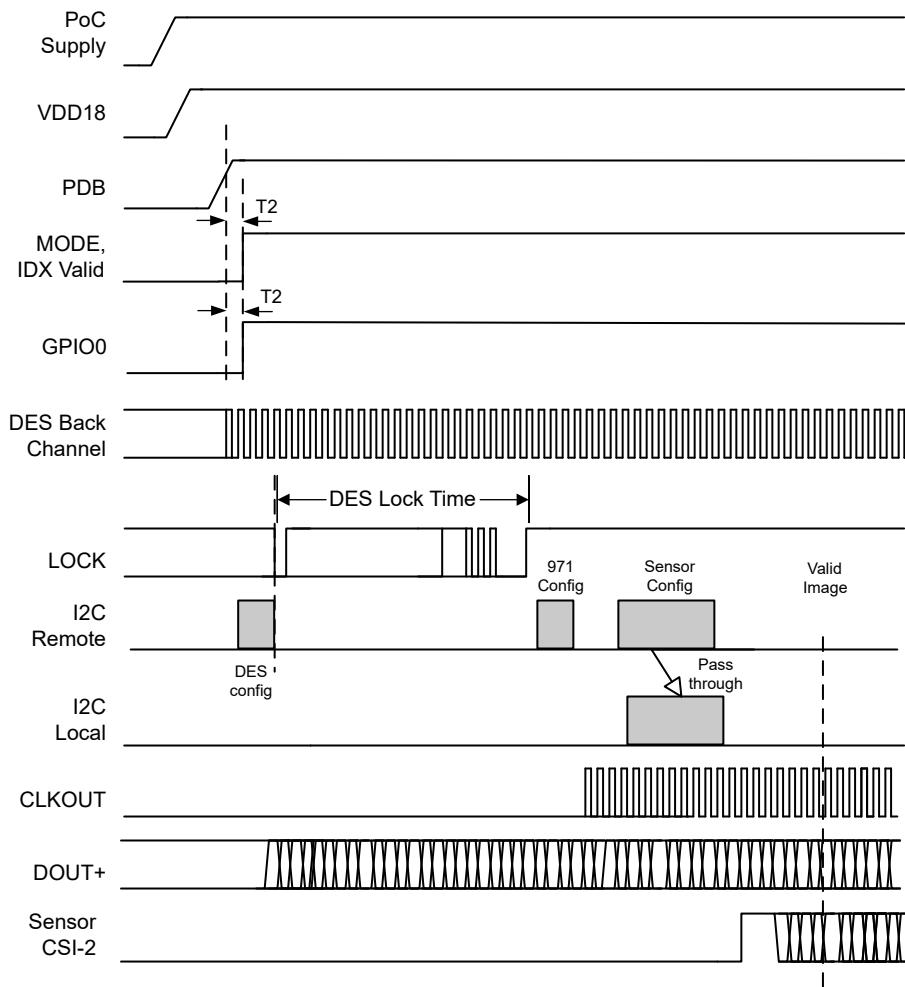
**Table 9-1. Timing Diagram for the Power Supply Start Up and Initialization Sequences**

PARAMETER	MIN	TYP	MAX	UNIT	NOTES
T0      VDD18 rise time	0.1			ms	at 10/90%
T1      VDD18 to PDB	0			ms	After VDD18 is stable
T2 <sup>3</sup> PDB to I2C/GPIO0 Ready	2			ms	See Figure 9-2

1. To issue a hard reset, pull the PDB voltage low for at least 3 ms.
2. To speed up I2C communication TI recommends setting 0x0A[1] to 1 and 0x0A[0] to 0 after start-up.
3. GPIO0 must be held low for the duration of T2.

### 9.1.1 System Initialization

When initializing the communications link between a deserializer hub and a DS90UB971-Q1 serializer, the system timing will depend on the mode selected for generating the serializer reference clock. When synchronous clocking mode is selected, the serializer will relock onto the extracted back channel reference clock once available so there is no need for local crystal oscillator at the sensor module. The initialization sequence follows the illustration given in [Figure 9-2](#).



**Figure 9-2. Initialization Sequence: Synchronous Clocking Mode**

## 9.2 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through VDD, where  $VDD = 1.71\text{ V}$  to  $1.89\text{ V}$ . PDB should be brought high after all power supplies on the board have stabilized.

When PDB is driven low, ensure that the pin is driven to  $0\text{ V}$  for at least  $3\text{ ms}$  before releasing or driving high. In the case where PDB is pulled up to VDD directly, a  $10\text{-k}\Omega$  pullup resistor and a  $> 1\text{-}\mu\text{F}$  capacitor to ground are required.

Toggling PDB low powers down the device and resets all control registers to default. After power up, if there are any errors seen, TI recommends clearing the registers to reset the errors.

## 10 PCB Layout

### 10.1 PCB Layout Guidelines

Circuit board layout and stack-up for the FPD-Link IV devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high-frequency or high-level inputs and outputs to minimize unwanted noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypassing should be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least 2 $\times$  the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 47- $\mu$ F to 100- $\mu$ F range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate CSI-2 signals away from the single-ended or differential FPD RX input traces to prevent coupling from the CSI-2 signals to the RX inputs. The following sections provide important details for routing the FPD-Link IV traces, PoC filter, and CSI-2 traces.

#### 10.1.1 Ground

TI recommends that a consistent ground plane reference for the high speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the DS90UB971-Q1 to the GND plane with vias.

#### 10.1.2 Routing FPD-Link IV Signal Traces and PoC Filter

Routing the FPD-Link IV signal traces between the D<sub>OUT</sub> pins and the connector as well as connecting the PoC filter to these traces are the most critical pieces of a successful DS90UB971-Q1 PCB layout. [Figure 10-1](#) shows an example PCB layout configured for interface to remote sensor modules over coaxial cables. The layout example also uses a footprint of a through-hole HFM FAKRA connector provided by Rosenberger (P/N: AMS10A-40MZ5-Y).

The following list provides essential recommendations for routing the FPD-Link IV signal traces between the DS90UB971-Q1 output pins (D<sub>OUT</sub>) and the FAKRA connector, and connecting the PoC filter.

- The routing of the FPD-Link IV traces may be all on the top layer (as shown in the example) or partially embedded in middle layers if EMI is a concern
- The AC-coupling capacitors should be on the top layer and very close to the DS90UB971-Q1 receiver input pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the D<sub>OUT+</sub> trace between the AC-coupling capacitor and the FAKRA connector as a 50- $\Omega$  single-ended micro-strip with tight impedance control ( $\pm 10\%$ ). Calculate the proper width of the trace for a 50- $\Omega$

impedance based on the PCB stack-up. Ensure that the trace can carry the PoC current for the maximum load presented by the remote sensor module.

- The PoC filter should be connected to the DOUT+ trace through the first RF inductor ( $L_4$ ). The  $L_4$  should be touching the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under PoC network pads. The anti-pad should be a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to  $50\ \Omega$  as possible.
- Route the DOUT– trace loosely coupled to the DOUT+ trace for the length similar to the DOUT+ trace length when possible. This will help the differential nature of the receiver to cancel out any common-mode noise that may be present in the environment that may couple on to the DOUT+ and DOUT– signal traces. When routing on inner layers, length matching for single ended traces does not provide as significant benefit.

When configured for STP and routing differential signals to the DS90UB971-Q1 receiver inputs, the traces should maintain  $100\text{-}\Omega$  differential impedance routed to the connector. When choosing to implement a common mode choke for common mode noise reduction, take care to minimize the effect of any mismatch. [Figure 10-2](#) shows an example PCB layout for STP configuration for the DS90UB971-Q1.

### 10.1.3 Routing CSI-2 Signal Traces

Routing the CSI-2 signal traces between the CSI-2 pins and the CSI-2 connector is also important for a successful DS90UB971-Q1 PCB layout. [Figure 10-3](#) shows essential details for routing the CSI-2 traces. Additional recommendations are given in the following list:

1. Route CSI\_D0N, CSI\_D0P, CSI\_D1N, and CSI\_D1P pairs as differential coupled striplines with controlled  $100\text{-}\Omega$  differential impedance ( $\pm 10\%$ )
2. Keep the trace length difference between CSI-2 traces to 5 mils of each other.
3. Length matching should be near the location of mismatch.
4. Each pair should be separated at least by 5 times the signal trace width.
5. Keep away from other high-speed signals.
6. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be  $\geq 135$  degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on one or two inner layers.
8. Keep the number of signal vias to a minimum — TI recommends keeping the via count to the maximum of two per CSI-2 trace.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

## 10.2 Layout Examples

The layout examples provided show a combo layout which can support either a coax or STP configuration based on and AC capacitor stuffing option.

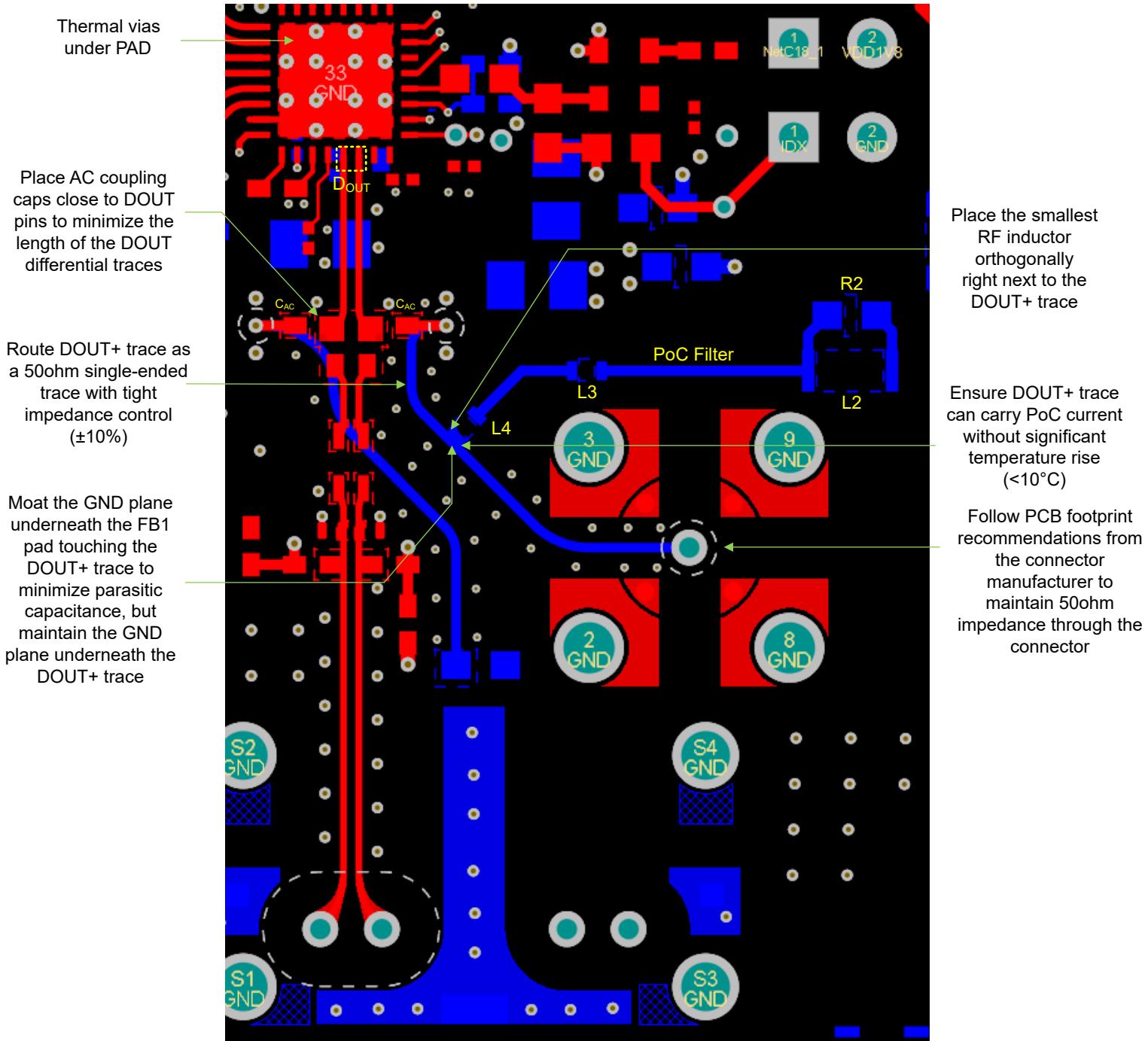


Figure 10-1. FPD-Link IV Signal Traces and PoC Filter PCB Layout Example

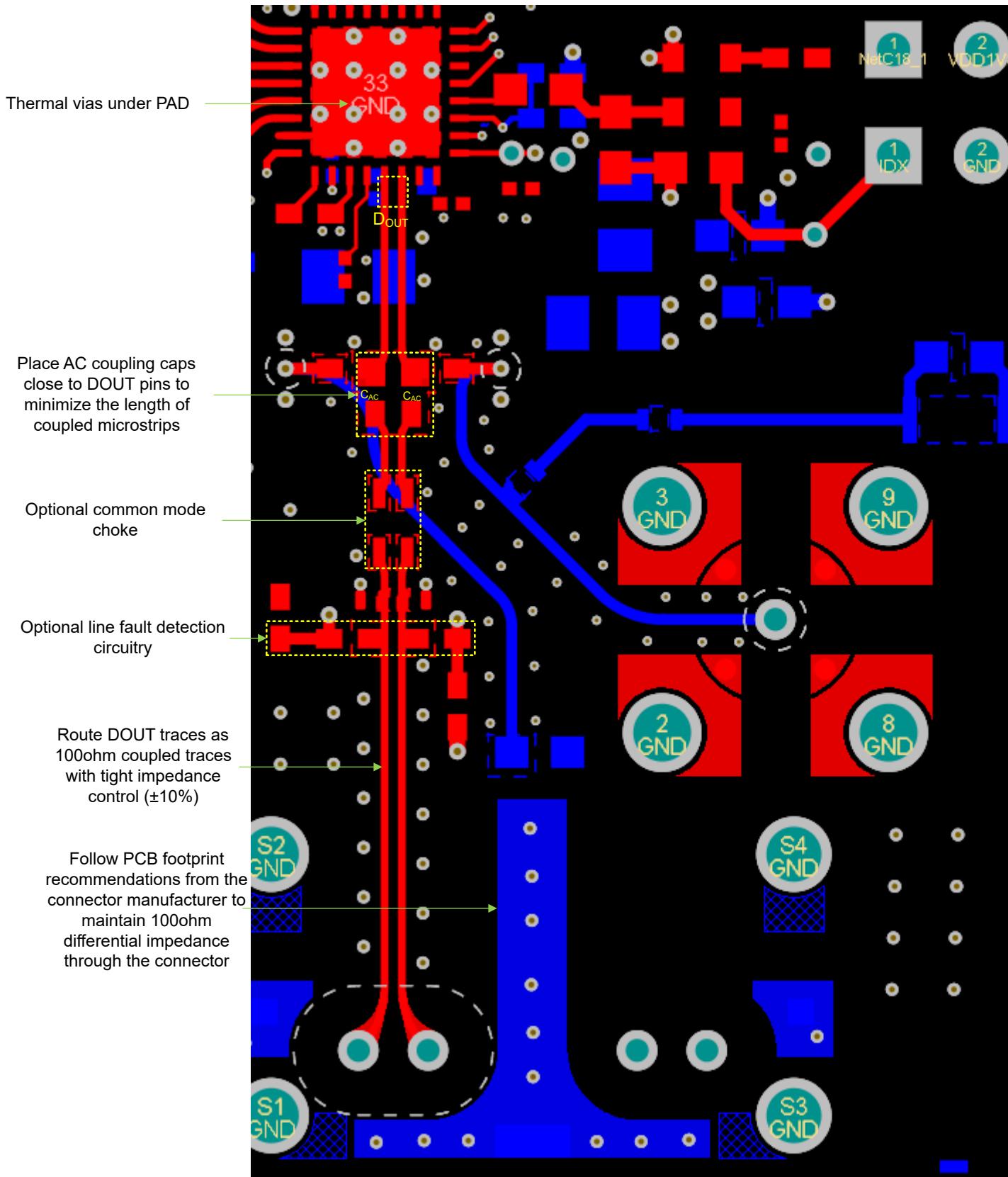


Figure 10-2. FPD-Link IV Differential Signal Traces PCB Layout Example

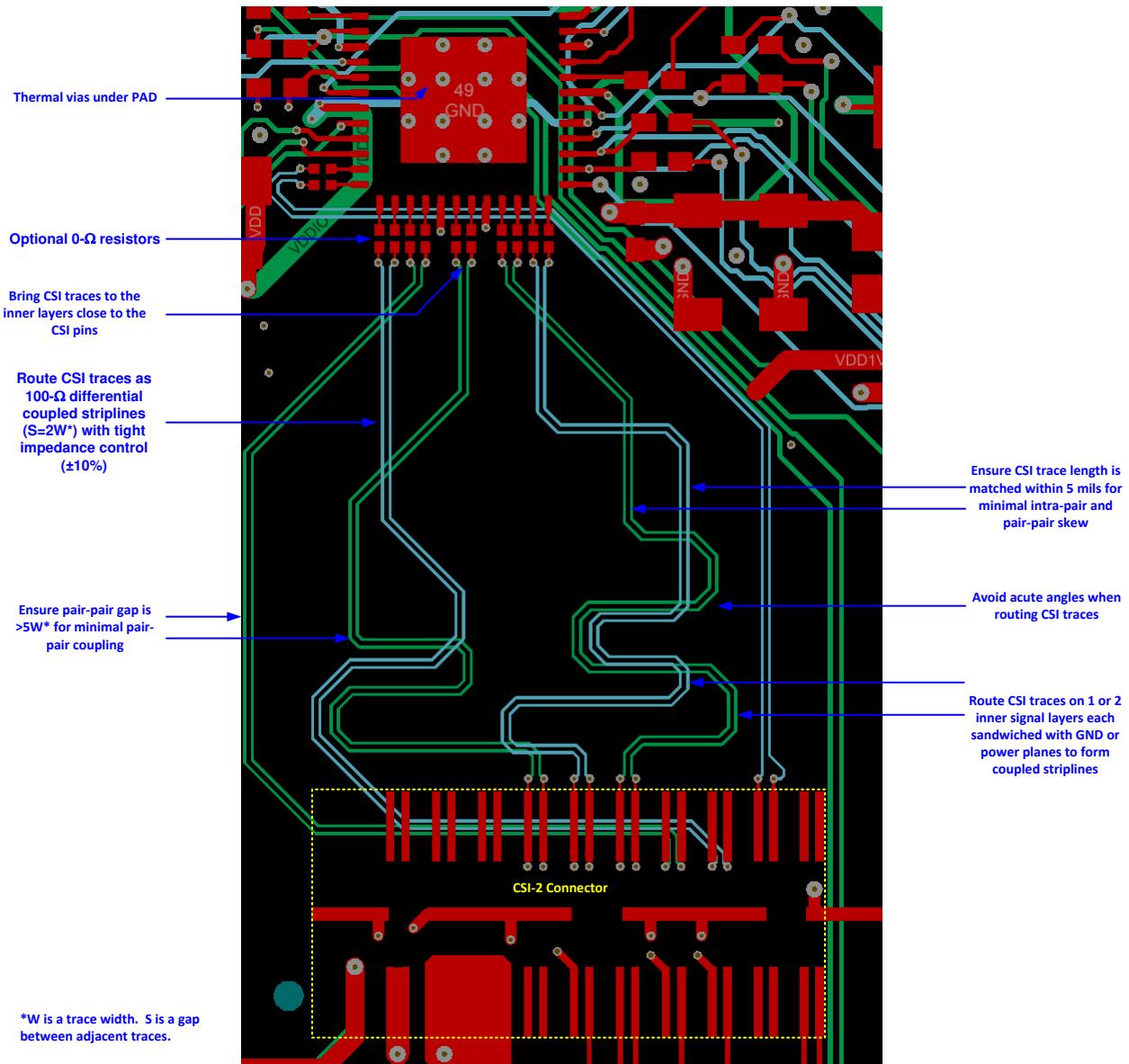


Figure 10-3. CSI-2 Traces PCB Layout Example

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Package Option Addendum

### Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(4)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking
DS90UB971RH BTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	Contact TI	Contact TI	-40 to 115	UB971Q
DS90UB971RH BRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	Contact TI	Contact TI	-40 to 115	UB971Q

- (1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

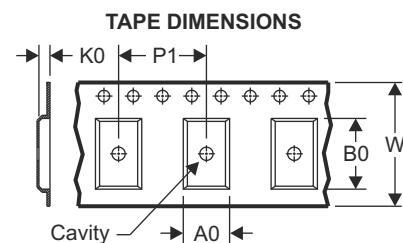
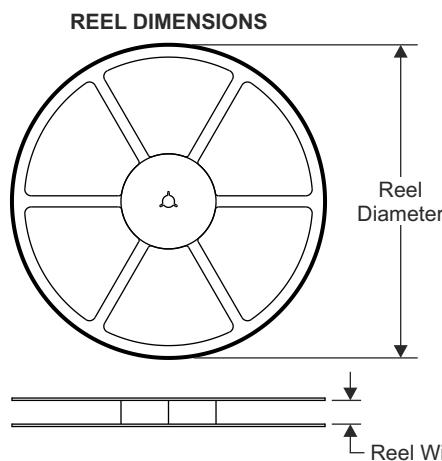
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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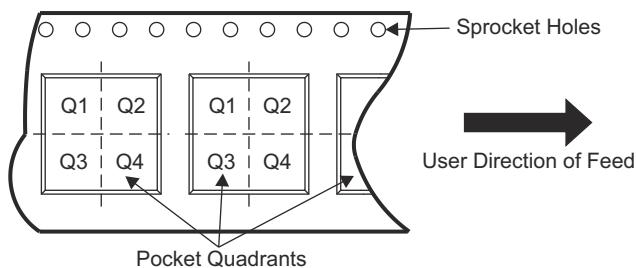
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## 12.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

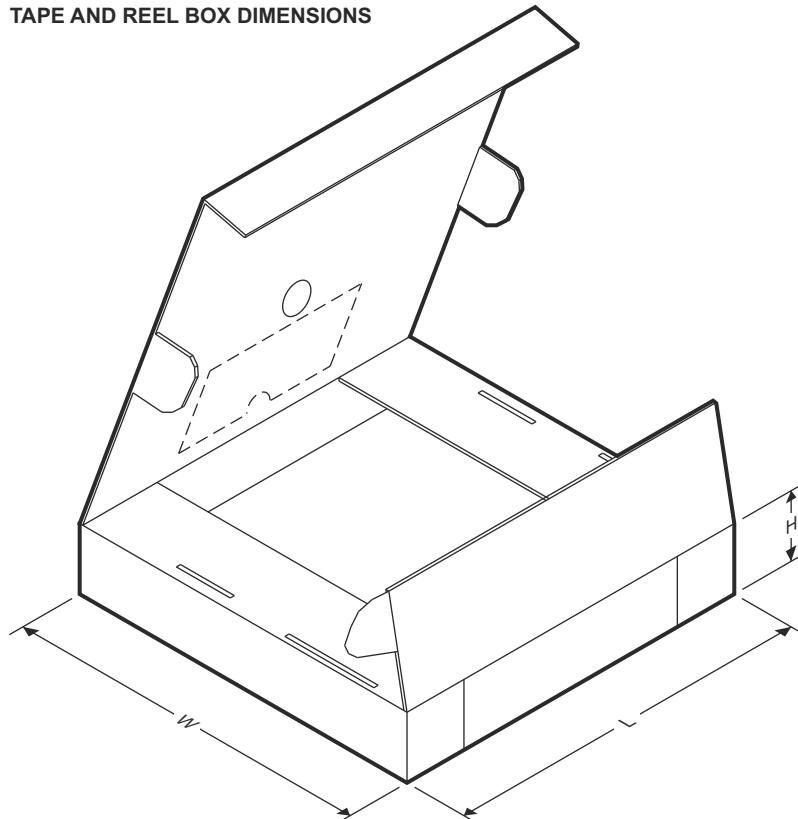


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB971RHBTQ1	VQFN	RHB	32	250	180	12.4	5.3	5.3	1.1	8	12	Q2
DS90UB971RHBRQ1	VQFN	RHB	32	3000	330	12.4	5.3	5.3	1.1	8	12	Q2

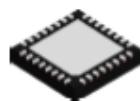
DS90UB971-Q1

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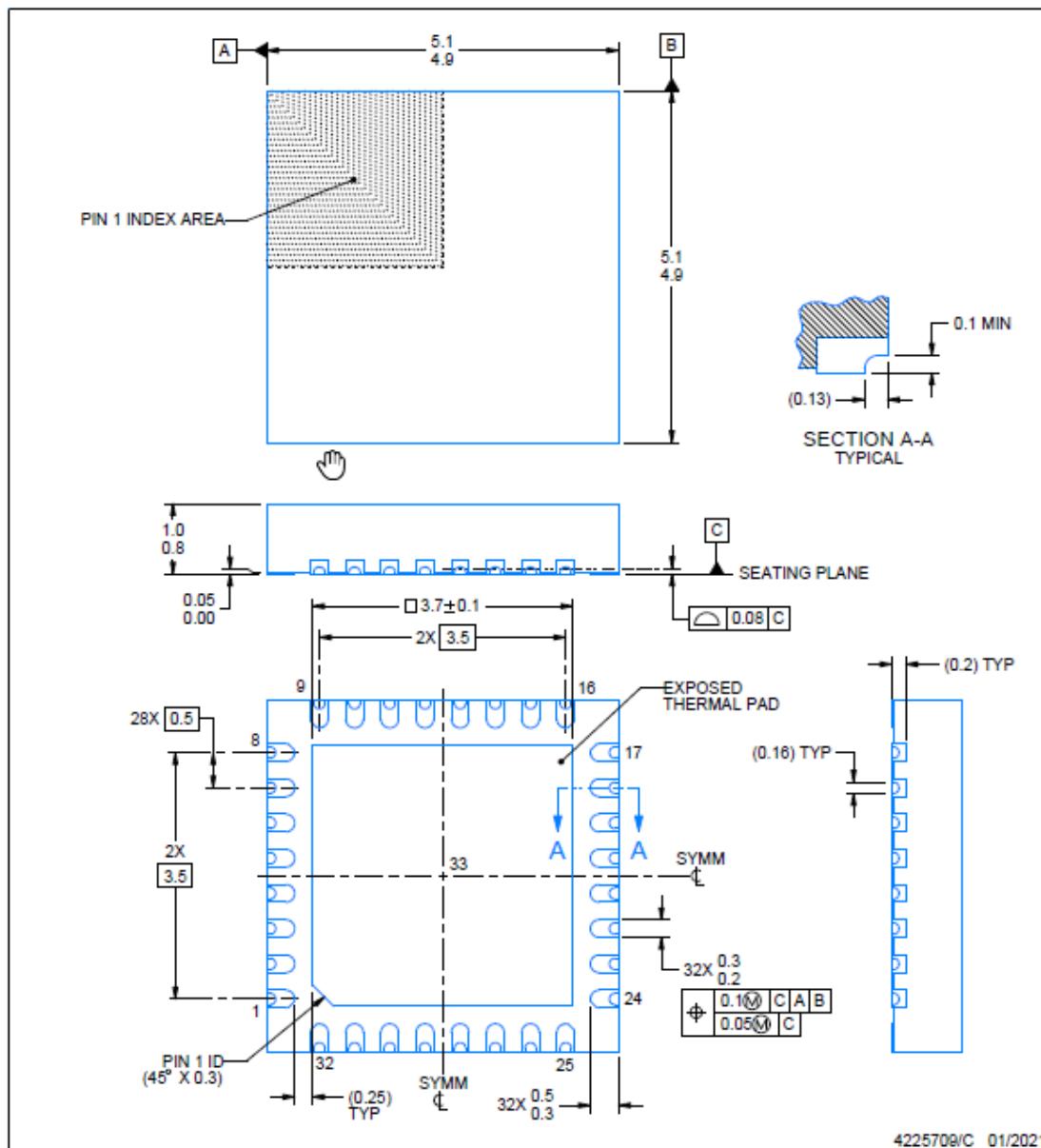
## TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB971RHBTQ1	VQFN	RHB	32	250	210	185	35
DS90UB971RHBRQ1	VQFN	RHB	32	3000	367	367	35

**RHB0032U****PACKAGE OUTLINE****VQFN - 1 mm max height**

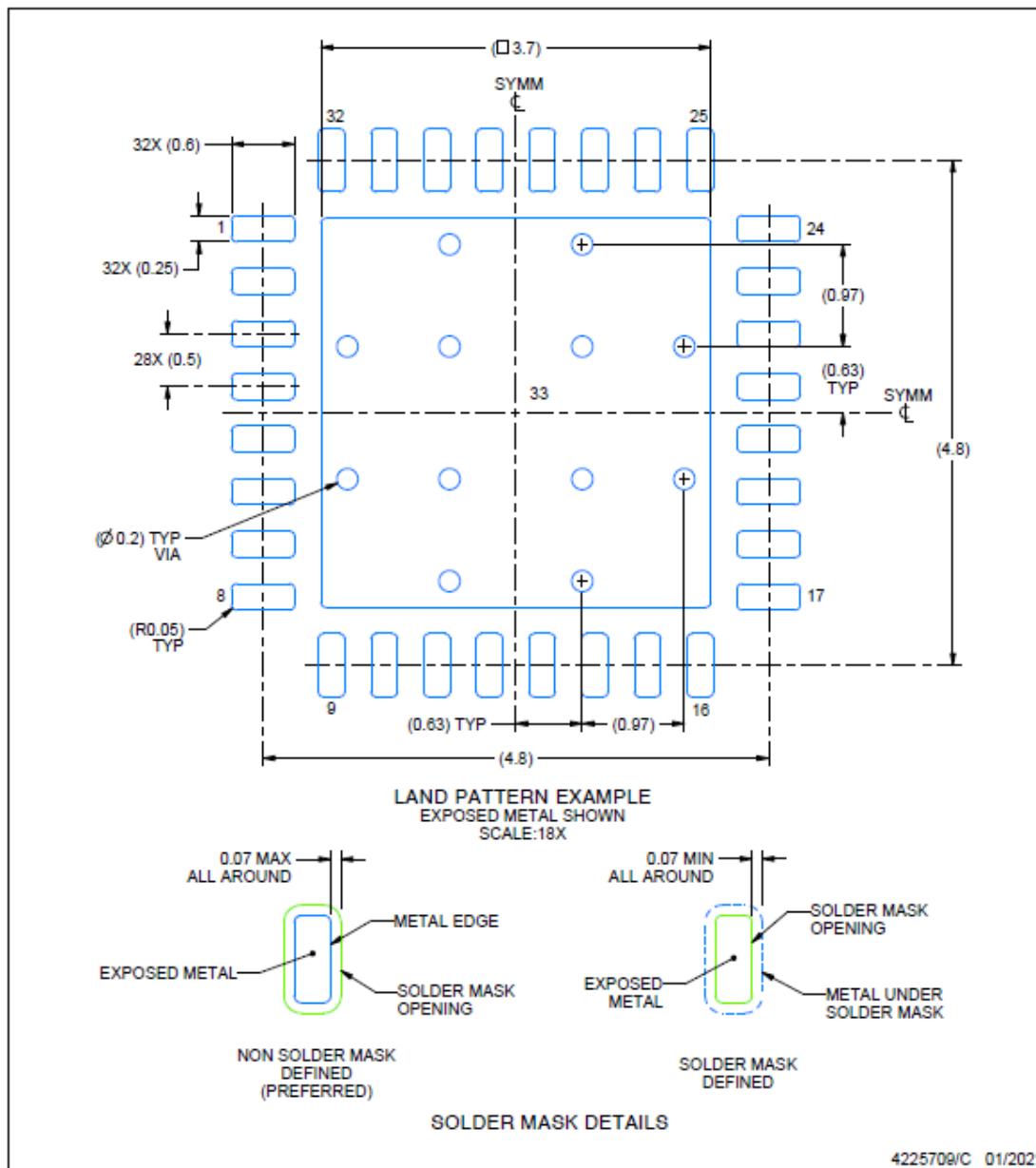
PLASTIC QUAD FLATPACK - NO LEAD

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT****RHB0032U****VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

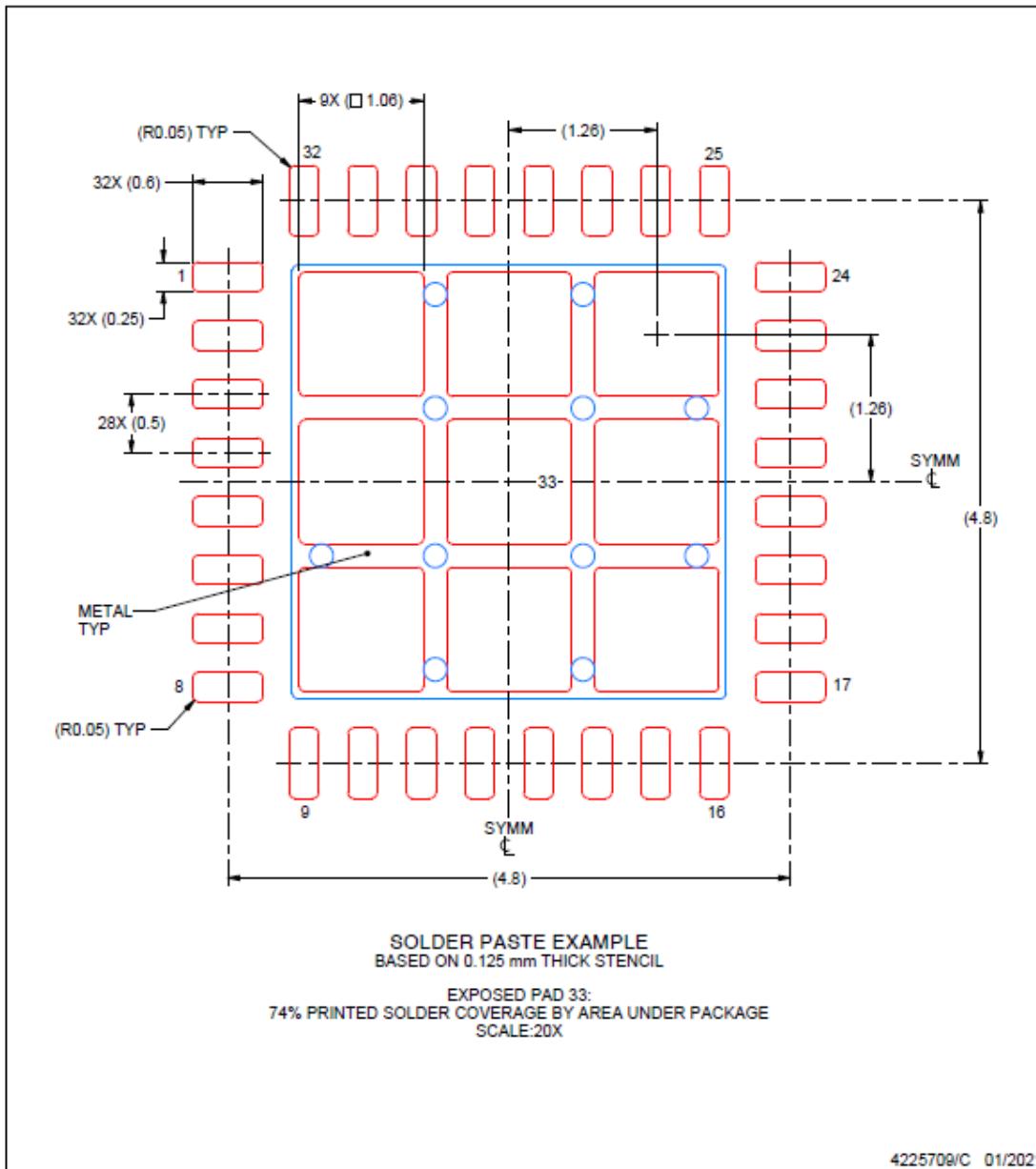


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN****RHB0032U****VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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