

DS90UB9702-Q1 Automotive FPD-Link™ IV Deserializer Hub With DPHY CSI-2 Output Ports for 8MP+ Cameras & Other Sensors

1 Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 2: -40°C to $+105^{\circ}\text{C}$
- Deserializer aggregates data from up to 4 sensors simultaneously
 - Supports 7/8MP+ imagers
 - Line rate at 7.55 Gbps
 - Single-ended coaxial or Shielded Twisted-Pair (STP) cable
 - Power-over-Cable (PoC) support
- CSI v2.1 Compliant system interface
 - Supports up to 2 MIPI CSI-2 output ports and 1 replication port
 - CSI Port 0: MIPI CSI-2 output port
 - CSI Port 1: MIPI CSI-2 output port
 - CSI Port 2: replication port
 - 16 Virtual channels and VC-ID remapping
- MIPI DPHY v2.1 compatible
 - Up to 4 data lanes with 2 clocks per port
 - Up to 2.5 Gbps per lane, 10 Gbps per port
- Quad CMLOUT output ports for off-board processing
 - 4 x CMLOUT ports replicated from 4 x FPD RX ports
 - Capable of driving another deserializer at the same line rate
- 10 GPIO Pins for sensor synchronization and diagnostics
- Dual I₂C ports
- Frozen frame detection
- Automatic receive equalization
- Compatible with DS90UB971-Q1, DS90UB981-Q1, DS90UB953-Q1, DS90UB953A-Q1, DS90UB951-Q1, DS90UB935-Q1, DS90UB933-Q1, and DS90UB913A-Q1 serializers
- Low Power Sleep Mode with GPIO-state retention

2 Applications

- Automotive Driver Assistance Systems (ADAS)
- Security and surveillance
- Industrial and consumer remote cameras
- Medical imaging systems

3 Description

The DS90UB9702-Q1 is an FPD-Link deserializer that delivers robust ultra-high-speed 7.55 Gbps forward channel and 47.1875 Mbps bidirectional control channel for connecting up to four raw data sensors to central processing units over an automotive coaxial or STP cable. When coupled with DS90UB971-Q1 serializer, the deserializer receives video data from imagers supporting ultra-high resolutions (8MP+/40fps) or multiple sensors in various topologies.

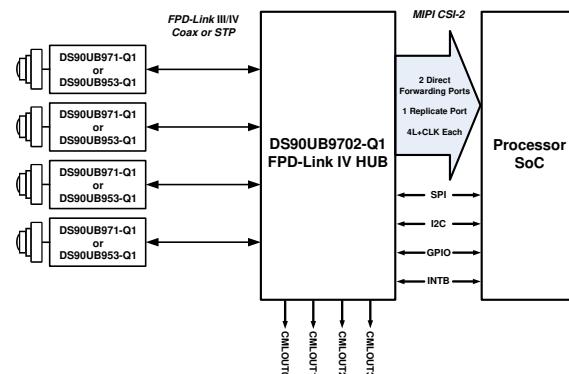
Data is received and aggregated into two MIPI CSI-2 DPHY outputs for interfacing with a downstream processor. An additional CSI port is used for port replication. The flexible MIPI CSI-2 outputs support multiple virtual channels interleaving per port to differentiate multiple sensors, exposures, and data types. This functionality features aggregate and replicate modes and supports input-to-output port as well as virtual channel (VC-ID) remapping.

Advanced data protection and diagnostic features support overall system functional safety. Multiple levels of data integrity checking and protection in conjunction with programmable health status interrupt helps ensure robust sensor module and link operation in vehicles.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DS90UB9702-Q1	VQFN (88)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.


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Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2021	*	RTM Release

5 Pin Configuration and Functions

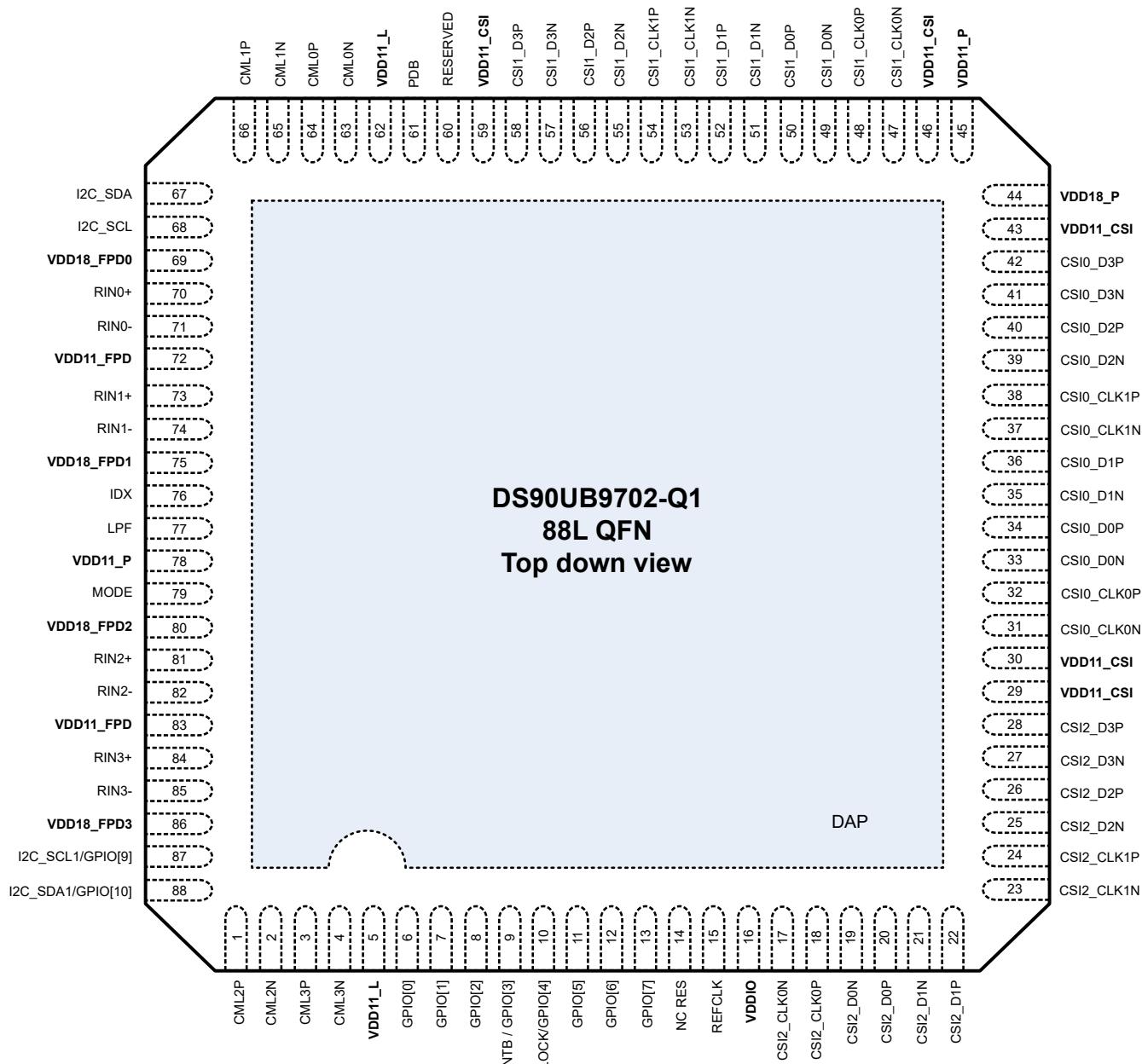


Figure 5-1. RUR Package, 88-Pin VQFN, (Top View)

Table 5-1. Pin Functions

PIN	I/O TYPE	DESCRIPTION
NAME	NO.	
MIPI DPHY/CSI-2		
CSI0_CLKON/P	31, 32	O, DPHY
		CSI0 Differential clock If unused, leave this pin unconnected.
CSI0_D0N/P	33, 34	O, DPHY
		CSI0 Differential data pair 0 If unused, leave this pin unconnected.
CSI0_D1N/P	35, 36	O, DPHY
		CSI0 Differential data pair 1 If unused, leave this pin unconnected.
CSI0_D2N/P	39, 40	O, DPHY
		CSI0 Differential data pair 2 If unused, leave this pin unconnected.

Table 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
CSI0_D3N/P	41, 42	O, DPHY	CSI0 Differential data pair 3 If unused, leave this pin unconnected.
CSI1_CLK0N/P	47, 48	O, DPHY	CSI1 Differential clock If unused, leave this pin unconnected.
CSI1_D0N/P	49, 50	O, DPHY	CSI1 Differential data pair 0 If unused, leave this pin unconnected.
CSI1_D1N/P	51, 52	O, DPHY	CSI1 Differential data pair 1 If unused, leave this pin unconnected.
CSI1_D2N/P	55, 56	O, DPHY	CSI1 Differential data pair 2 If unused, leave this pin unconnected.
CSI1_D3N/P	57, 58	O, DPHY	CSI1 Differential data pair 3 If unused, leave this pin unconnected.
CSI2_CLK0N/P	17, 18	O, DPHY	CSI2 Differential Clock If unused, leave this pin unconnected.
CSI2_D0N/P	19, 20	O, DPHY	CSI2 Differential data pair 0 If unused, leave this pin unconnected.
CSI2_D1N/P	21, 22	O, DPHY	CSI2 Differential data pair 1 If unused, leave this pin unconnected.
CSI2_D2N/P	25, 26	O, DPHY	CSI2 Differential data pair 2 If unused, leave this pin unconnected.
CSI2_D3N/P	27, 28	O, DPHY	CSI2 Differential data pair 3 If unused, leave this pin unconnected.
CSI0_CLK1N/P	37, 38	O, DPHY	Receive data is CSI-2 configured with DPHY outputs as one differential clock lane (CSI0_CLK0P/N) and up to four differential data lanes (CSI0_D0P/N: CSI0_D3P/N) or two clock lanes (CSI0_CLK0P/N, CSI0_CLK1P/N) and two differential data lanes for each clock. If unused, leave this pin unconnected.
CSI1_CLK1N/P	53, 54	O, DPHY	Receive data is CSI-2 configured with DPHY outputs as one differential clock lane (CSI1_CLK0P/N) and up to four differential data lanes (CSI1_D0P/N: CSI1_D3P/N) or two clock lanes (CSI1_CLK0P/N, CSI1_CLK1P/N) and two differential data lanes for each clock. When in replicate mode data lanes CSI1_D2P/N and CSI1_D3P/N are associated with clock lane CSI1_CLK1P/N to provide the replicated output. If unused, leave this pin unconnected.
CSI2_CLK1N/P	23, 24	O, DPHY	Receive data is CSI-2 configured with DPHY outputs as one differential clock lane (CSI2_CLK0P/N) and up to four differential data lanes (CSI2_D0P/N: CSI2_D3P/N) or two clock lanes (CSI2_CLK0P/N, CSI2_CLK1P/N) and two differential data lanes for each clock. If unused, leave this pin unconnected.

FPD-LINK IV INTERFACE

RIN0-/+	71, 70	I/O	FPD-Link IV Input/Output. The pin must be AC-coupled with a capacitor. If using coax configuration, use a 100nF AC coupling capacitor for RIN0+ and terminate RIN0- to GND with a 47nF capacitor and 50Ω resistor. If using STP configuration, connect both RIN0+ and RIN0- with 100nF AC-coupling capacitors. If port is unused, set RX_PORT_CTL register bit N to 0 to disable and leave the pins floating.
RIN1-/+	74, 73	I/O	FPD-Link IV Input/Output. The pin must be AC-coupled with a capacitor. If using coax configuration, use a 100nF AC coupling capacitor for RIN1+ and terminate RIN1- to GND with a 47nF capacitor and 50Ω resistor. If using STP configuration, connect both RIN01+ and RIN1- with 100nF AC-coupling capacitors. If port is unused, set RX_PORT_CTL register bit N to 0 to disable and leave the pins floating.
RIN2-/+	82, 81	I/O	FPD-Link IV Input/Output. The pin must be AC-coupled with a capacitor. If using coax configuration, use a 100nF AC coupling capacitor for RIN2+ and terminate RIN2- to GND with a 47nF capacitor and 50Ω resistor. If using STP configuration, connect both RIN2+ and RIN2- with 100nF AC-coupling capacitors. If port is unused, set RX_PORT_CTL register bit N to 0 to disable and leave the pins floating.
RIN3-/+	85, 84	I/O	FPD-Link IV Input/Output. The pin must be AC-coupled with a capacitor. If using coax configuration, use a 100nF AC coupling capacitor for RIN3+ and terminate RIN3- to GND with a 47nF capacitor and 50Ω resistor. If using STP configuration, connect both RIN3+ and RIN3- with 100nF AC-coupling capacitors. If port is unused, set RX_PORT_CTL register bit N to 0 to disable and leave the pins floating.

GPIO PINS (GENERAL PURPOSE INPUT OUTPUT)

GPIO[0]	6	I/O, LVCMOS, PD	General Purpose Input/Output 0. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.
GPIO[1]	7	I/O, LVCMOS, PD	General Purpose Input/Output 1. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.

Table 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
GPIO[2]	8	I/O, LVCMOS, PD	General Purpose Input/Output 2. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.
INTB(GPIO[3])	9	I/O, Open Drain	Interrupt output, can be reprogrammed to General Purpose Input/Output 3. This pin is open drain. Recommended Pull-up with 4.7 kΩ to VDDIO. If unused, leave this pin unconnected.
LOCK(GPIO[4])	10	I/O, LVCMOS, PD	Logic OR of all receiver LOCK, can be reprogrammed to General Purpose Input/Output 4. If unused, leave this pin unconnected.
GPIO[5]	11	I/O, LVCMOS, PD	General Purpose Input/Output 5. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.
GPIO[6]	12	I/O, LVCMOS, PD	General Purpose Input/Output 6. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.
GPIO[7]	13	I/O, LVCMOS, PD	General Purpose Input/Output 7. The status of this pin is held during low power sleep mode. If unused, leave this pin unconnected.
I2C_SCL1(GPIO[9])	87	I/O, Open Drain	I2C Clock Port 1, can be reprogrammed to open drain General Purpose Output 9. Only output is supported if configured as a GPIO. Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
I2C_SDA1/ GPIO[10]	88	I/O, Open Drain	I2C Data Port 1, can be reprogrammed to open drain General Purpose Output 10. Only output is supported if configured as a GPIO. Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
I2C PINS			
I2C_SDA	67	I/O, Open Drain	I2C Data Port 0 Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
I2C_SCL	68	I/O, Open Drain	I2C Clock Port 0 Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
I2C_SCL1(GPIO[9])	87	I/O, Open Drain	I2C_SCL1 pin, can be reprogrammed to open drain General Purpose Input/Output 9. Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
I2C_SDA1/ GPIO[10]	88	I/O, Open Drain	I2C Data Port 1, can be reprogrammed to open drain General Purpose Input/Output 10. Recommend a 4.7 kΩ Pull-up Resistor to VDDIO. If unused, leave this pin unconnected.
IDX	76	S	I2C Serial Control Bus Device ID Address Connect to external pull-up to VDD18 and pull-down to GND to create a voltage divider. Refer to Section 8.5.2 .
CONTROL PINS			
MODE	79	S	Mode selection Connect to external pull-up to VDD18 and pull-down to GND to create a voltage divider. Refer to Table 8-16 .
PDB	61	I, LVCMOS, PD	Power-down mode Connect this pin with a 10kΩ pull-up resistor to 1.8V and a 10uF cap to GND. PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down. Refer to Section 10.1.3
STATUS PINS			
INTB(GPIO[3])	9	I/O, Open Drain	Interrupt output, can be reprogrammed to General Purpose Input/Output 3. The default state of this pin is open drain. Recommended Pull-up with 4.7 kΩ to VDDIO. If unused, leave this pin unconnected.
LOCK(GPIO[4])	10	I/O, LVCMOS, PD	Logic OR of all receiver LOCK, can be reprogrammed to General Purpose Input/Output 4. If unused, leave this pin unconnected.
POWER AND GROUND			
VDDIO	16	P	1.8 V (±5%) OR 3.3V (±10%) LVCMOS I/O Power Requires 0.1 μF and 0.01 μF capacitors to GND
VDD11_CSI VDD11_CSI VDD11_CSI VDD11_CSI VDD11_CSI	29 30 43 46 59	P	1.1 V (±5%) Power Supplies Requires a 10uF to GND shared between all the pins, and 1uF, 0.1 μF, and 0.01 μF capacitors to GND at each VDD pin.
VDD11_L VDD11_L	5 62	P	1.1 V (±5%) Power Supplies Requires a 1uF to GND shared between both pins, and 0.1 μF and 0.01 μF capacitors to GND at each VDD pin.
VDD11_FPD VDD11_FPD	72 83	P	1.1 V (±5%) Power Supplies Requires a 10uF to GND shared between both pins, and 1uF, 0.1 μF, and 0.01 μF capacitors to GND at each VDD pin.

Table 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VDD11_P VDD11_P	45 78	P	1.1 V ($\pm 5\%$) Power Supplies Requires a 10uF to GND shared between both pins, and 1uF, 0.1 μ F, and 0.01 μ F capacitors to GND at each VDD pin. Recommend pin 78 to have its own 1.1V supply, not shared with other 1.1V rails.
VDD18_P	44	P	1.8 V ($\pm 5\%$) Power Supplies Requires a 1uF, 0.1 μ F, and 0.01 μ F capacitors to GND at each VDD pin.
VDD18_FPD0 VDD18_FPD1 VDD18_FPD2 VDD18_FPD3	69 75 80 86	P	1.8 V ($\pm 5\%$) Power Supplies Requires a 10uF to GND shared between both pins, and 1uF, 0.1 μ F, and 0.01 μ F capacitors to GND at each VDD pin.
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
OTHERS			
REFCLK	15	I, LVCMOS	Reference clock oscillator input. 25 MHz LVCMOS-level oscillator input (± 100 ppm).
RES	60	I, LVCMOS, PD	Connect to a 10k Ω resistor to GND.
LPF	77	P	Loop Filter: LPF Pin is for connecting the filter capacitor to internal PLL circuits. LPF must have a 100nF capacitor to GND. Place capacitor close to the pin.
CML0P/N	64, 63	O	Serial Output Ports for Off-board Processing. If using coax configuration, use a 100nF AC coupling capacitor for CML0P and terminate CML0N to GND with a 47nF capacitor and 50 Ω resistor. If using STP configuration, connect both CML0P/N with 100nF AC coupling capacitors. If not used, leave floating or terminate both pins with 50 Ω resistors.
CML1P/N	66, 65	O	Serial Output Ports for Off-board Processing. If using coax configuration, use a 100nF AC coupling capacitor for CML1P and terminate CML1N to GND with a 47nF capacitor and 50 Ω resistor. If using STP configuration, connect both CML1P/N with 100nF AC coupling capacitors. If not used, leave floating or terminate both pins with 50 Ω resistors.
CML2P/N	1, 2	O	Serial Output Ports for Off-board Processing. If using coax configuration, use a 100nF AC coupling capacitor for CML2P and terminate CML2N to GND with a 47nF capacitor and 50 Ω resistor. If using STP configuration, connect both CML2P/N with 100nF AC coupling capacitors. If not used, leave floating or terminate both pins with 50 Ω resistors.
CML3P/N	3, 4	O	Serial Output Ports for Off-board Processing. If using coax configuration, use a 100nF AC coupling capacitor for CML3P and terminate CML3N to GND with a 47nF capacitor and 50 Ω resistor. If using STP configuration, connect both CML3P/N with 100nF AC coupling capacitors. If not used, leave floating or terminate both pins with 50 Ω resistors.
NC RES	14	I/O, LVCMOS	This pin is RESERVED and should be left floating.

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- P = Power Supply
- G = Ground
- DPHY = MIPI DPHY Interface
- LVCMOS = LVCMOS pin
- I = Input
- O = Output
- I/O = Input/Output
- S = Strap Input
- PD, PU = Internal Pull-Down/Pull-Up (All strap pins have weak internal pull-ups or pull-downs determined by IOZ specification. If the default strap value is needed to be changed then an external 1 k Ω resistor should be used.)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Supply voltage	VDD18_CSI, VDD18_P1 , VDD18_P0, VDD18_FPD0, VDD18_FPD1	-0.3	2.16	V	
Supply voltage	VDD11_CSI, VDD11_D , VDD11_FPD0, VDD11_FPD1	-0.3	1.32	V	
Supply voltage	VDDIO	-0.3	3.96	V	
FPD-Link IV input voltage	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	Device powered up (All supplies within recommended operating conditions)	-0.3	2.75	V
		Device powered down, Transient Voltage	-0.3	1.45	V
		Device powered down, DC Voltage	-0.3	1.32	V
CSI-2 voltage	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLK0P, CSI0_CLK0N, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P, CSI1_D2N, CSI1_D3P, CSI1_D3N, CSI1_CLK1P, CSI1_CLK1N, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLK2P, CSI2_CLK2N,	-0.3	1.32	V	
LVCMOS IO voltage	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, REFCLK, PDB	-0.3	$V_{(VDDIO)} + 0.3$	V	
Configuration input voltage	MODE, IDX	-0.3	$V_{(VDD18)} + 0.3$	V	
Open-Drain voltage	GPIO3/INTB, GPIO9, GPIO10, I2C_SDA, I2C_SCL, I2C_SDA1, I2C_SCL1	-0.3	3.96	V	
Junction temperature, T_J			150	°C	
Storage temperature, T_{stg}		-65	150	°C	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	ESD Rating (IEC 61000-4-2, powered-up only), R _D =330 Ω, C _S =150 pF	Contact Discharge: RIN+/RIN-	±6	kV
		ESD Rating (IEC 61000-4-2, powered-up only), R _D =330 Ω, C _S =150 pF	Contact Discharge: CMLOUT+/CMLOUT-	±4	kV
		ESD Rating (ISO10605), R _D =330 Ω, 2 kΩ, C _S =150 pF and 330 pF	Contact Discharge: RIN+/RIN-	±6	kV
		ESD Rating (ISO10605), R _D =330 Ω, 2 kΩ, C _S =150 pF and 330 pF	Contact Discharge: CMLOUT+/CMLOUT-	±4	kV
		ESD Rating (IEC 61000-4-2, powered-up only), R _D =330 Ω, C _S =150 pF	Air Discharge: RIN+/RIN-	±15	kV
		ESD Rating (IEC 61000-4-2, powered-up only), R _D =330 Ω, C _S =150 pF	Air Discharge: CMLOUT+/CMLOUT-	±8	kV
		ESD Rating (ISO10605), R _D =330 Ω, 2 kΩ, C _S =150 pF and 330 pF	Air Discharge: RIN+/RIN-	±15	kV
		ESD Rating (ISO10605), R _D =330 Ω, 2 kΩ, C _S =150 pF and 330 pF	Air Discharge: CMLOUT+/CMLOUT-	±8	kV
		Media Dependent Interface Pins (RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-, CMLOUT0+, CMLOUT0-, CMLOUT1+, CMLOUT1-, CMLOUT2+, CMLOUT2-, CMLOUT3+, CMLOUT3-)		±7	kV
		ESD (HBM) per AEC Q100-002	All other pins	±2	kV
		ESD (CDM) per AEC Q100-001	Charged-device model (CDM) ESD Classification Level C6, per AEC Q100-011	±1.25	kV

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V _(VDD18)	1.71	1.8	1.89	V
	V _(VDD11)	1.045	1.1	1.155	
LVCMOS I/O supply voltage	V _(VDDIO) - 1.8V	1.71	1.8	1.89	V
	V _(VDDIO) - 3.3V	3.0	3.3	3.6	V
VDD _(I2C)	1.8V Operation	1.71	1.8	1.89	V
	3.3V Operation	3.0	3.3	3.6	V
Open drain voltage	INTB = V _{INTB} , I ₂ C pins = V _{I2C}	1.71		3.6	V
Operating free air temperature, T _A		-40	25	105	°C
MIPI D-PHY data rate (per CSI-2 lane)		400		2500	Mbps
MIPI D-PHY CSI-2 HS clock frequency		200		1250	MHz
Reference clock oscillator frequency			25		MHz
Spread-spectrum reference clock modulation percentage	REFCLK, Center spread	-0.25		0.25	%
	REFCLK, Down spread	-0.5		0	%
Local I ₂ C Clock Frequency, f _{SCL}				1	MHz

6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply noise	V _{VDD11} (10 Hz - 50 MHz), sinusoidal at supply pin			25	mV _{P-P}
	V _{VDD18} (10 Hz - 50 MHz), sinusoidal at supply pin			50	
	V _{VDDIO} , 1.8 V Operation (10 Hz - 50 MHz), sinusoidal at supply pin			50	
	V _{VDDIO} , 3.3 V Operation (10 Hz - 50 MHz), sinusoidal at supply pin			100	
	V _{I₂C} , 1.8 V Operation (10 Hz - 50 MHz), sinusoidal at supply pin			50	
	V _{I₂C} , 3.3 V Operation (10 Hz - 50 MHz), sinusoidal at supply pin			100	

6.4 Thermal Information

THERMAL METRIC		DS90UB9702-Q1	UNIT
		QFN	
		88 PINS	
R _{θJA}	Junction-to-ambient thermal resistance (standard)	18.4	°C/W
R _{θJA}	Junction-to-ambient thermal resistance (enhanced) 45 thermal vias, 12mil vias 1oz plating	13.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	6.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.1	°C/W
Y _{JB}	Junction-to-board characterization parameter	4.3	°C/W

6.5 DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
TOTAL POWER CONSUMPTION						
P _{T1}	Total power consumption	(4) FPD-Link IV 7.55 Gbps, CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2220	mW
P _{T2}	Total power consumption	(3) FPD-Link IV 7.55 Gbps, (1) FPD-Link III 3.775 Gbps, CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2302	mW
P _{T3}	Total power consumption	(2) FPD-Link IV 7.55 Gbps, (2) FPD-Link III 3.775 Gbps, CSI-2 3 ports, 2500 Mbps/lane, no CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2443	mW
P _{T4}	Total power consumption	(2) FPD-Link IV 7.55 Gbps, (2) FPD-Link III 3.775 Gbps, CSI-2 3 ports, 2500 Mbps/lane, retimed CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2450	mW
P _{T5}	Total power consumption	(4) FPD-Link III , CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2450	mW
P _{T6}	Total power consumption	(4) FPD-Link IV 7.55 Gbps, CSI-2 3 ports, 2500 Mbps/lane, retimed CMLOUT	V _(VDD18) V _(VDD11) V _(VDDIO)		2450	mW

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T7}	Total power consumption	(2) FPD-Link IV 7.55 Gbps, (1) FPD-Link III 3.775 Gbps, (1) FPD-Link III 1.4Gbps, CSI-2 3 ports, 2500 Mbps/lane, no CMLOUT	$V_{(VDD18)}$ $V_{(VDD11)}$ $V_{(VDDIO)}$		2441		mW
P_{T8}	Total power consumption - Low Power	LP - GPIO Hold, VDD11 removed	$V_{(VDD18)}$ $V_{(VDD11)}$ $V_{(VDDIO)}$		100		mW
P_{T9}	Total power consumption - PDB = L	PDB = L	$V_{(VDD18)}$ $V_{(VDD11)}$ $V_{(VDDIO)}$		1092		mW

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{DD1}	(4) FPD-Link IV 7.55 Gbps, CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	VDD18	390	mA		
I _{DD1}		VDD11	1230			
I _{DD1}		VDDIO	20			
I _{DD1}		VDD11_CSI-29	58			
I _{DD1}		VDD11_CSI-30, 43	142			
I _{DD1}		VDD11_CSI-46, 59	139			
I _{DD1}		VDD11_P-45,78	78			
I _{DD1}		VDD11_FPD01- 72	155			
I _{DD1}		VDD11_FPD23- 83	150			
I _{DD1}		VDD11_L-5,62	508			
I _{DD1}		VDD18_FPD0-6 9	90			
I _{DD1}		VDD18_FPD1-7 5	103			
I _{DD1}		VDD18_FPD2-8 0	91			
I _{DD1}		VDD18_FPD3-8 6	90			
I _{DD1}		VDD18_P-44	16			
I _{DD2}	(3) FPD-Link IV 7.55 Gbps, (1) FPD-Link III 3.775 Gbps, CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	VDD18	447	mA		
I _{DD2}		VDD11	1200			
I _{DD2}		VDDIO	20			
I _{DD2}		VDD11_CSI-29	58			
I _{DD2}		VDD11_CSI-30, 43	142			
I _{DD2}		VDD11_CSI-46, 59	139			
I _{DD2}		VDD11_P-45,78	78			
I _{DD2}		VDD11_FPD01- 72	155			
I _{DD2}		VDD11_FPD23- 83	120			
I _{DD2}		VDD11_L-5,62	508			
I _{DD2}		VDD18_FPD0-6 9	90			
I _{DD2}		VDD18_FPD1-7 5	103			
I _{DD2}		VDD18_FPD2-8 0	91			
I _{DD2}		VDD18_FPD3-8 6	147			
I _{DD2}		VDD18_P-44	16			

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{DD3}	Supply current	(2) FPD-Link IV 7.55 Gbps, (2) FPD-Link III 3.775 Gbps, CSI-2 3 ports, 2500 Mbps/lane, no CMLOUT	VDD18			504	mA
I_{DD3}	Supply current		VDD11			1228	
I_{DD3}	Supply current		VDDIO			20	
I_{DD3}	Supply current		VDD11_CSI-29			139	
I_{DD3}	Supply current		VDD11_CSI-30, 43			142	
I_{DD3}	Supply current		VDD11_CSI-46, 59			139	
I_{DD3}	Supply current		VDD11_P-45,78			56	
I_{DD3}	Supply current		VDD11_FPD01-72			155	
I_{DD3}	Supply current		VDD11_FPD23-83			89	
I_{DD3}	Supply current		VDD11_L-5,62			508	
I_{DD3}	Supply current		VDD18_FPD0-69			90	
I_{DD3}	Supply current		VDD18_FPD1-75			103	
I_{DD3}	Supply current		VDD18_FPD2-80			148	
I_{DD3}	Supply current		VDD18_FPD3-86			147	
I_{DD3}	Supply current		VDD18_P-44			16	
I_{DD4}	Supply current	(2) FPD-Link IV 7.55 Gbps, (2) FPD-Link III 3.775 Gbps, CSI-2 3 ports, 2500 Mbps/lane, retimed CMLOUT	VDD18			504	mA
I_{DD4}	Supply current		VDD11			1340	
I_{DD4}	Supply current		VDDIO			20	
I_{DD4}	Supply current		VDD11_CSI-29			139	
I_{DD4}	Supply current		VDD11_CSI-30, 43			142	
I_{DD4}	Supply current		VDD11_CSI-46, 59			139	
I_{DD4}	Supply current		VDD11_P-45,78			107	
I_{DD4}	Supply current		VDD11_FPD01-72			155	
I_{DD4}	Supply current		VDD11_FPD23-83			89	
I_{DD4}	Supply current		VDD11_L-5,62			569	
I_{DD4}	Supply current		VDD18_FPD0-69			90	
I_{DD4}	Supply current		VDD18_FPD1-75			103	
I_{DD4}	Supply current		VDD18_FPD2-80			148	
I_{DD4}	Supply current		VDD18_FPD3-86			147	
I_{DD4}	Supply current		VDD18_P-44			16	

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{DD5}	Supply current	(4) FPD-Link III , CSI-2 2 ports, 2500 Mbps/lane, no CMLOUT	VDD18			618	mA
I_{DD5}	Supply current		VDD11			1065	
I_{DD5}	Supply current		VDDIO			20	
I_{DD5}	Supply current		VDD11_CSI-29			58	
I_{DD5}	Supply current		VDD11_CSI-30, 43			142	
I_{DD5}	Supply current		VDD11_CSI-46, 59			139	
I_{DD5}	Supply current		VDD11_P-45,78			40	
I_{DD5}	Supply current		VDD11_FPD01-72			89	
I_{DD5}	Supply current		VDD11_FPD23-83			89	
I_{DD5}	Supply current		VDD11_L-5,62			508	
I_{DD5}	Supply current		VDD18_FPD0-69			147	
I_{DD5}	Supply current		VDD18_FPD1-75			160	
I_{DD5}	Supply current		VDD18_FPD2-80			148	
I_{DD5}	Supply current		VDD18_FPD3-86			147	
I_{DD5}	Supply current		VDD18_P-44			16	
I_{DD6}	Supply current	(4) FPD-Link IV 7.55 Gbps, CSI-2 3 ports, 2500 Mbps/lane, retimed CMLOUT	VDD18			390	mA
I_{DD6}	Supply current		VDD11			1422	
I_{DD6}	Supply current		VDDIO			20	
I_{DD6}	Supply current		VDD11_CSI-29			139	
I_{DD6}	Supply current		VDD11_CSI-30, 43			142	
I_{DD6}	Supply current		VDD11_CSI-46, 59			139	
I_{DD6}	Supply current		VDD11_P-45,78			128	
I_{DD6}	Supply current		VDD11_FPD01-72			155	
I_{DD6}	Supply current		VDD11_FPD23-83			150	
I_{DD6}	Supply current		VDD11_L-5,62			569	
I_{DD6}	Supply current		VDD18_FPD0-69			90	
I_{DD6}	Supply current		VDD18_FPD1-75			103	
I_{DD6}	Supply current		VDD18_FPD2-80			91	
I_{DD6}	Supply current		VDD18_FPD3-86			90	
I_{DD6}	Supply current		VDD18_P-44			16	

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{DD7}	Supply current	(2) FPD-Link IV 7.55 Gbps, (1) FPD-Link III 3.775 Gbps, (1) FPD-Link III 1.4Gbps, CSI-2 3 ports, 2500 Mbps/lane, no CMLOUT	VDD18			504	mA
I_{DD7}	Supply current		VDD11			1229	mA
I_{DD7}	Supply current		VDDIO			20	mA
I_{DD7}	Supply current		VDD11_CSI-29			139	mA
I_{DD7}	Supply current		VDD11_CSI-30, 43			142	mA
I_{DD7}	Supply current		VDD11_CSI-46, 59			139	mA
I_{DD7}	Supply current		VDD11_P-45,78			56	mA
I_{DD7}	Supply current		VDD11_FPD01- 72			155	mA
I_{DD7}	Supply current		VDD11_FPD23- 83			90	mA
I_{DD7}	Supply current		VDD11_L-5,62			508	mA
I_{DD7}	Supply current		VDD18_FPD0-6 9			90	mA
I_{DD7}	Supply current		VDD18_FPD1-7 5			103	mA
I_{DD7}	Supply current		VDD18_FPD2-8 0			148	mA
I_{DD7}	Supply current		VDD18_FPD3-8 6			147	mA
I_{DD7}	Supply current		VDD18_P-44			16	mA
I_{DD8}	Supply Current - Low Power	LP - GPIO Hold, VDD11 removed	VDD18			40	mA
I_{DD8}	Supply Current - Low Power		VDD11			0	
I_{DD8}	Supply Current - Low Power		VDDIO			7	
I_{DDZ}	Shutdown current	PDB = LOW	VDD18			56	mA
I_{DDZ}	Shutdown current		VDD11			836	mA
I_{DDZ}	Shutdown current		VDDIO			7	mA

1.8V LVCMOS I/O

V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}, V_{(VDDIO)} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO[10,9,7:0]	$V_{(VDDIO)} - 0.45$	$V_{(VDDIO)}$	V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}, V_{(VDDIO)} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO[10,9,7:0], INTB	GND	0.45	V
V_{IH}	High-level input voltage	$V_{(VDDIO)} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO[7:4,2:0], PDB, REFCLK	$0.65 \times V_{(VDDIO)}$	$V_{(VDDIO)}$	V
V_{IL}	Low-level input voltage			GND	$0.35 \times V_{(VDDIO)}$	V
I_{IH}	Input high current	$V_{IN} = V_{(VDDIO)} = 1.71 \text{ to } 1.89 \text{ V, internal pull down enabled}$	PDB, REFCLK	22	58	μA
I_{IH}	Input high current	$V_{IN} = V_{(VDDIO)} = 1.71 \text{ to } 1.89 \text{ V, internal pull down enabled}$	GPIO[7:4,2:0]	45	115	μA
I_{IH}	Input high current	$V_{IN} = V_{(VDDIO)} = 1.71 \text{ to } 1.89 \text{ V, internal pull down disabled}$	GPIO[7:4,2:0]		20	μA
I_{IL}	Input low current	$V_{IN} = 0$	GPIO[7:4,2:0], PDB, REFCLK	-20	3.5	μA
$I_{IN-STRAP}$	Strap pin input current	$V_{IN} = 0 \text{ to } V_{(VDDIO)}$	MODE, IDX	-1	1	μA
I_{OS}	Output short circuit current	$V_{OUT} = 0 \text{ V}$	GPIO[10,9,7:0]	-35		mA

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I _{OZ}	TRI-STATE output current	V _{OUT} = 0 V or V _(VDDIO) , PDB = LOW	GPIO[7:4, 2:0]	-20		20	µA
I _{OZ}	TRI-STATE output current	V _{OUT} = 0 V or V _(VDDIO) , PDB = LOW	GPIO[10,9,3]	-40		40	µA
3.3V LVCMOS I/O							
V _{OH}	High-level output voltage	I _{OH} = -4 mA, V _(VDDIO) = 3.0 V to 3.6 V	GPIO[10,9,7:0]	2.4		V _(VDDIO)	V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _(VDDIO) = 3.0 V to 3.6 V	GPIO[10,9,7:0], INTB	GND		0.4	V
V _{IH}	High-level input voltage	V _(VDDIO) = 3.0 V to 3.6 V	GPIO[7:4,2:0], REFCLK	2		V _(VDDIO)	V
			PDB	1.17		V _(VDDIO)	V
V _{IL}	Low-level input voltage	V _(VDDIO) = 3.0 V to 3.6 V	GPIO[7:4,2:0], REFCLK	GND		0.8	V
			PDB	GND		0.63	V
I _{IH}	Input high current	V _{IN} = V _(VDDIO) = 3.0 to 3.6 V, internal pull down enabled	PDB,REFCLK	42		108	µA
I _{IH}	Input high current	V _{IN} = V _(VDDIO) = 3.0 to 3.6 V, internal pull down enabled	GPIO[7:4, 2:0]	85		215	µA
I _{IH}	Input high current	V _{IN} = V _(VDDIO) = 3.0 to 3.6 V, internal pull down disabled	GPIO[7:4,2:0]			30	µA
I _{IL}	Input low current	V _{IN} = 0	GPIO[7:4, 2:0]. PDB, REFCLK	-20		3.5	µA
I _{OS}	Output short circuit current	V _{OUT} = 0 V	GPIO[10,9,7:0]		-65		mA
I _{OZ}	TRI-STATE output current	V _{OUT} = 0 V or V _(VDDIO) , PDB = LOW	GPIO[7:4, 2:0]	-20		30	µA
I _{OZ}	TRI-STATE output current	V _{OUT} = 0 V or V _(VDDIO) , PDB = LOW	GPIO[10,9,3]	-40		50	µA
OPEN DRAIN OUTPUT							
V _{OL}	Low-level output voltage	I _{OL} = 2 mA, V _(VDDIO) = 1.71 V to 1.89 V	GPIO[10:9], INTB, I _{2C} _SDA, I _{2C} _SCL, I _{2C} _SDA1, I _{2C} _SCL1	GND		0.45	V
I _{IN}	Leakage current	V _{IN} = V _(VDDIO)	I _{2C} _SDA, I _{2C} _SCL,	-10		10	µA
I _{IN}	Leakage current	V _{IN} = V _(VDDIO)	GPIO[10:9], INTB, I _{2C} _SDA1, I _{2C} _SCL1	-20		20	µA
I_{2C} DC SPECIFICATIONS							
V _{IH}	Input high-level	V _(I_{2C}) = 1.71 V to 1.89 V	I _{2C} _SDA, I _{2C} _SCL, I _{2C} _SDA1, I _{2C} _SCL1	0.7 × V _(I_{2C})		V _(I_{2C})	V
V _{IH}	Input high-level	V _(I_{2C}) = 3.0 V to 3.6 V	I _{2C} _SDA, I _{2C} _SCL, I _{2C} _SDA1, I _{2C} _SCL1	0.7 × V _(I_{2C})		V _(I_{2C})	V

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V _{IL}	Input low-level	V _(I₂C) = 1.71 V to 1.89 V	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	GND	0.3 × V _(I₂C)	V	
V _{IL}	Input low-level	V _(I₂C) = 3.0 V to 3.6 V	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	GND	0.3 × V _(I₂C)	V	
V _{HYS}	Input hysteresis		I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1		100		mV
V _{OL1}	Output low-level	Standard-mode/Fast-mode I _{OL} = 3 mA, V _(I₂C) = 3.0 V to 3.6 V	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	0	0.4	V	
		Fast-mode Plus I _{OL} = 20 mA, V _(I₂C) = 3.0 V to 3.6 V	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	0	0.4	V	
V _{OL2}	Output low-level	Fast-mode/Fast-mode Plus I _{OL} = 2 mA, V _(I₂C) = 1.71 V to 1.89 V	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	0	0.2 × V _(I₂C)	V	
I _{OL}	Output low-level current	Standard/Fast Mode	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	3			mA
		Fast Plus Mode	I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1	20			
I _{IN}	Input current	V _{IN} = 0 or V _(I₂C)	I ₂ C_SDA, I ₂ C_SCL	-10	10	μA	
I _{IN}	Input current	V _{IN} = 0 or V _(I₂C)	I ₂ C_SDA1, I ₂ C_SCL1	-20	20	μA	
C _{IN}	Input capacitance		I ₂ C_SDA, I ₂ C_SCL, I ₂ C_SDA1, I ₂ C_SCL1		5	pF	
VOLTAGE AND TEMPERATURE SENSING							
V _{ACC-INT}	Voltage sensor accuracy - Internal	Monitor 1.1 V, 1.8 V +/-5% monitored power nodes	internal voltage monitoring	-1.5	1.5	%	
V _{ACC-EXT}	Voltage sensor accuracy - External	0.4 V - 1.1 V	GPIO pins monitoring external voltage	-1.5	1.5	%	
T _{ACC}	Temperature sensor accuracy T _{junction}	-40°C to 150°C			±5	°C	
FPD-LINK IV DC SPECIFICATIONS							
V _{ID}	Differential Input Voltage	FPD-Link III	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	100			mV

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V _{ID}	Differential Input Voltage	FPD-Link IV	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	120			mV
V _{IN}	Single ended Input Voltage	FPD-Link III	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	50			mV
V _{IN}	Single ended Input Voltage	FPD-Link IV	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	60			mV
R _T	Internal Termination Resistor	Single-ended RIN+ or RIN-	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	40	50	60	Ω
	Internal Termination Resistor	Differential across RIN+ and RIN-	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	80	100	120	Ω

FPD-LINK IV BIDIRECTIONAL CONTROL CHANNEL

V _{OUT-BC}	FPD-Link III / DVP Back channel single ended output voltage	R _L = 50 Ω, coaxial configuration, forward channel disabled	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	190	220	275	mV
V _{OUT-BC}	FPD-Link IV Back channel single ended output voltage	R _L = 50 Ω, coaxial configuration, forward channel disabled	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	183	210	250	mV
V _{OD-BC}	FPD-Link III / DVP Back channel differential output voltage (RIN+) - (RIN-)	R _L = 100 Ω, coaxial configuration, forward channel disabled	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	380	440	550	mV
V _{OD-BC}	FPD-Link IV Back channel differential output voltage (RIN+) - (RIN-)	R _L = 100 Ω, coaxial configuration, forward channel disabled	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	366	420	500	mV
V _{CM-BC}	Back channel common voltage to DC Gnd (RIN+) or (RIN-)	common mode voltage	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-			550	mV
E _{BCJ}	Back Channel Output Jitter	Back channel output jitter measured with 400 kHz -3 dB CDR BW	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-			0.3	UI _{BC}
E _{BCH}	Back Channel Output Eye Height	Single-ended RIN+ or RIN-, 47.1875 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	130	160		mV _{P-P}
E _{BCW}	Back Channel Output Eye Width	Single-ended RIN+ or RIN-, 47.1875 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-			0.8	UI

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
f_{BC}	Back channel bit time	FPD-Link III: 3.775 Gbps Synchronous clock mode; BC 47.1875 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		21.2		ns
		FPD-Link IV: 7.55 Gbps Synchronous clock mode; BC 47.1875 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		21.2		ns
		FPD-Link III: 4.16 Gbps Non-synchronous clock mode; BC 9.4375 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		106		ns
		FPD-Link IV: 7.55 Gbps Non-synchronous clock mode; BC 9.4375 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		106		ns
		FPD-Link III: DVP Non-synchronous clock mode; BC 2.3594 Mbps	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		424		ns

D-PHY HSTX Driver DC Specifications

V_{CMTX}	HS transmit static common mode voltage		CS10_D0P, CS10_D0N, CS10_D1P, CS10_D1N, CS10_D2P, CS10_D2N, CS10_D3P, CS10_D3N, CS10_CLKP, CS10_CLKN, CS11_D0P, CS11_D0N, CS11_D1P, CS11_D1N, CS11_D2P/N, CS11_D3P, CS11_D3N, CS11_CLKP, CS11_CLKN, CS12_D0P, CS12_D0N, CS12_D1P, CS12_D1N, CS12_D2P, CS12_D2N, CS12_D3P, CS12_D3N, CS12_CLKP, CS12_CLKN	150	200	250	mV
$ \Delta V_{CMTX(1,0)} $	V_{CMTX} mismatch when output is 1 or 0					5	mV
$ V_{OD} $	HS transmit differential voltage			140	200	270	mV
$ \Delta V_{OD} $	V_{OD} mismatch when output is 1 or 0					14	mV
V_{OHHS}	HS output high voltage					360	mV
Z_{os}	Single ended output impedance			40	50	62.5	Ω
ΔZ_{os}	Mismatch in single ended output impedance					20	%

6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
D-PHY LPTX Driver DC Specifications							
V _{OH}	Output high-level	Applicable when the supported data rate is > 1.5 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	0.95	1.1	V	mV
V _{OL}	Output low-level			-50	50	mV	
Z _{O LP}	Output impedance			110		Ω	

6.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
GPIO LVCMOS I/O AC SWITCHING CHARACTERISTICS							
t _{CLH}	LVCMOS low-to-high transition-time	V _{VDDIO} = 1.71 V to 1.89 V OR V _{VDDIO} = 3.0 V to 3.6 V C _L = 8pF (lumped load) Default Registers	GPIO10,9,[7:0]	2.5		ns	
t _{CHL}	LVCMOS high-to-low transition-time		GPIO10,9,[7:0]	2.5		ns	
t _{PDB}	PDB reset pulse width	Power supplies applied and stable	PDB	2		ms	
FPD-LINK IV / III AC SPECIFICATIONS							
f _{FC}	Forward channel line rate	FPD-Link IV	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	7.55		Gbps	
f _{FC}	Forward channel line rate	FPD-Link IV	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	3.775		Gbps	
f _{FC}	Forward channel line rate	FPD-Link III	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	2.0	4.85	Gbps	
f _{FC}	Forward channel line rate	FPD-Link III DVP	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	0.7	1.867	Gbps	

6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
t_{DDLT}	Deserializer Data Lock Time FPD-Link IV	AEQ full range	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		20	400	ms
t_{DDLT}	Deserializer Data Lock Time FPD-Link IV	AEQ range +/-3	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		15	30	ms
t_{DDLT}	Deserializer Data Lock Time FPD-Link III	AEQ full range	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		20	400	ms
t_{DDLT}	Deserializer Data Lock Time FPD-Link III	AEQ range +/-3	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		15	30	ms
t_{DDLT}	Deserializer Data Lock Time FPD-Link III DVP	AEQ full range	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		20	400	ms
t_{DDLT}	Deserializer Data Lock Time FPD-Link III DVP	AEQ range +/-3	RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-		15	30	ms
REFCLK							
f_{MOD}	Spread Spectrum Clocking Modulation Frequency			30	33		kHz
f_{DEV}	Spread Spectrum Clocking Deviation Frequency FPD-Link IV CDR	center spread		-0.25	0.25		%
f_{DEV}	Spread Spectrum Clocking Deviation Frequency FPD-Link IV CDR	down spread			0.5		%
f_{DEV}	Spread Spectrum Clocking Deviation Frequency FPD-Link III CDR	center spread		-0.5	0.5		%
f_{DEV}	Spread Spectrum Clocking Deviation Frequency FPD-Link III CDR	down spread			1.0		%
f_{REFCLK}	REFCLK clock frequency		REFCLK	25			MHz
JIT_{REFCLK}	Allowable REFCLK clock jitter, CLKOUT is not used	Total jitter measured in the 0.2 MHz - 10 MHz frequency band with 2 MHz CDR JTF bandwidth at BER of 10^{-12}	REFCLK		200		ps
$JIT_{REFCLK-CLKOUT}$	Allowable REFCLK clock jitter if CLKOUT is used	Total jitter measured in the 0.2 MHz - 10 MHz frequency band with 2 MHz CDR JTF bandwidth at BER of 10^{-12}	REFCLK		130		ps
$JIT_{GPIO-CLKOUT}$	GPIO-CLKOUT forwarded REFCLK jitter	Total jitter measured in the 0.2 MHz - 10 MHz frequency band with 2 MHz CDR JTF bandwidth at BER of 10^{-12}	GPIO programmed as CLKOUT		200		ps

6.7 AC Electrical Characteristics MIPI D-PHY

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
MIPI D-PHY HSTX AC SPECIFICATIONS						
$\Delta V_{CMTX(LF)}$	Common-mode voltage variations LF	Above 450 MHz Between 50 and 450 MHz	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	15	mV	
				25	mV	
MIPI D-PHY LPTX AC SPECIFICATIONS						
T_{RLP}/T_{FLP}	15%-85% rise time and fall time		CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	25	ns	
T_{REOT}	30%-85% rise time and fall time			35	ns	
$\delta V/\delta t_{SR}$	Slew rate @ $C_{LOAD} = 70\text{pF}$	50pF test fixture C_{LOAD}	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	150	mV/n s	

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
C _{LOAD}	Load Capacitance	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	0	70		pF
MIPI D-PHY CLOCK TIMING SPECIFICATIONS						
U _{INST}	UI instantaneous	400 Mbps to 2.5 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN,	0.4	2.5	ns
ΔUI	UI variation	UI ≥ 1 ns	CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	-0.1	0.1	UI _{HS}
		0.4 ns < UI < 1 ns	-0.05	0.05	UI _{HS}	
MIPI D-PHY DATA-CLOCK TIMING SPECIFICATIONS						

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT	
$t_{\text{SKEW(TX)}}$	Tx Data to Clock Skew	Data rate 400 Mbps to 1 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	-0.15	0.15	UI _{HS}	
		Data rate: >1 Gbps to 2.5 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	-0.2	0.2	UI _{HS}	
$T_{\text{EYE_TX}}$	Transmitter Eye Width, Test 1.5.7	Data rate: >1.5 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	0.5			UI

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V _{DIF_TX}	Transmitted Eye Height, Test 1.5.7	Data rate: >1.5 Gbps		40		mV

MIPI D-PHY SKEW-CALIBRATION TIMING SPECIFICATIONS

T _{SKEWCAL_S_YNC}	Time that the transmitter drives the skew-calibration sync pattern, FFFFh	Data rate: > 1.5 Gbps	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	16	UI _{HS}
T _{SKEWCAL}	Time that the transmitter drives the skew-calibration pattern in the initial skew-calibration mode			100	μs
				32768	UI _{HS}
				10	μs

MIPI D-PHY TIMING SPECIFICATIONS

t _{CLK-POST}	HS exit		CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	60 + 52 × UI	ns
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6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{CLK-PRE}$	Time HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		8		UI
$t_{CLK-PREPARE}$	Clock lane HS entry	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		38	95	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		60		ns

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{CLK-PREPARE} + t_{CLK-ZERO}$	$t_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the clock	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		300		ns
t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ to the start of the LP-11 state following a HS burst	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		$105 + 12 \times UI$		ns
$t_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		100		ns

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{HS-PREPARE}$	Data lane HS entry	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN	40 + 4 × UI		85 + 6 × UI	ns
$t_{HS-PREPARE} + t_{HS-ZERO}$	$t_{HS-PREPARE} +$ time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		145 + 10 × UI		ns
$t_{HS-TRAIL}$	Data lane HS exit	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		max(n × 8 × UI, 60 + 4 × UI)		ns

6.7 AC Electrical Characteristics MIPI D-PHY (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT	
t_{LPX}	Transmitted length of LP state	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		50			ns
t_{INIT}	Initialization period	CSI0_D0P, CSI0_D0N, CSI0_D1P, CSI0_D1N, CSI0_D2P, CSI0_D2N, CSI0_D3P, CSI0_D3N, CSI0_CLKP, CSI0_CLKN, CSI1_D0P, CSI1_D0N, CSI1_D1P, CSI1_D1N, CSI1_D2P/N, CSI1_D3P, CSI1_D3N, CSI1_CLKP, CSI1_CLKN, CSI2_D0P, CSI2_D0N, CSI2_D1P, CSI2_D1N, CSI2_D2P, CSI2_D2N, CSI2_D3P, CSI2_D3N, CSI2_CLKP, CSI2_CLKN		100			μs

6.8 Recommended Timing for the Serial Control BusOver I²C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0	100	kHz	
		Fast-mode	>0	400	kHz	
		Fast-mode Plus	>0	1	MHz	
t_{LOW}	SCL Low Period	Standard-mode	4.7			μs
		Fast-mode	1.3			μs
		Fast-mode Plus	0.5			μs
t_{HIGH}	SCL High Period	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs

6.8 Recommended Timing for the Serial Control Bus (continued)

Over I²C supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
$t_{HD:DAT}$	Data hold time	Standard-mode	0	3.45	μs	
		Fast-mode	0	0.9	μs	
		Fast-mode Plus	0	0.45	μs	
$t_{SU:DAT}$	Data set up time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU:STO}$	Set up time for STOP condition	Standard-mode	4			μs
		Fast-mode	0.6			μs
		Fast-mode Plus	0.26			μs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			μs
		Fast-mode	1.3			μs
		Fast-mode Plus	0.5			μs
t_r	SCL and SDA rise time	Standard-mode		1000		ns
		Fast-mode		300		ns
		Fast-mode Plus		120		ns
t_f	SCL and SDA fall time	Standard-mode		300		ns
		Fast-mode		300		ns
		Fast-mode Plus		120		ns
C_b	Capacitive load for each bus line	Standard-mode		400		pF
		Fast-mode		400		pF
		Fast-mode Plus		550		pF
$t_{VD:DAT}$	Data valid time	Standard-mode		3.45		μs
		Fast-mode		0.9		μs
		Fast-mode Plus		0.45		μs
$t_{VD:ACK}$	Data valid acknowledge time	Standard-mode		3.45		μs
		Fast-mode		0.9		μs
		Fast-mode Plus		0.45		μs
t_{SP}	Input filter	Standard-mode		50		ns
		Fast-mode		20		ns
		Fast-mode Plus		6		ns
t_{SCK}	SPI Clk period		40			ns
t_{SPWH}	SPI Clk logic '1' period		16			ns
t_{SPWL}	SPI Clk logic '0' period		16			ns
t_{CSH}	CS# logic '1' time before new cycle		2			us
t_{CSDOD}	CS# logic '1' to logic '0' active time before cycle		2			us
t_{CSSC}	CS# active to SCK rising edge		2			us
t_{SCCS}	SCLK falling edge to CS# '0' to '1' end of cycle		2			us
t_{PI_ST}	PICO setup time before SCK transition		4			ns
t_{PI_HD}	PICO hold time after SCK transition		4			ns
t_{PO_DD}	POCI time from SCK transition to output			4		ns
t_{PO_HD}	POCI hold time after SCK transition			3		ns

7 Timing Diagrams



Figure 7-1. LVC MOS Transition Times

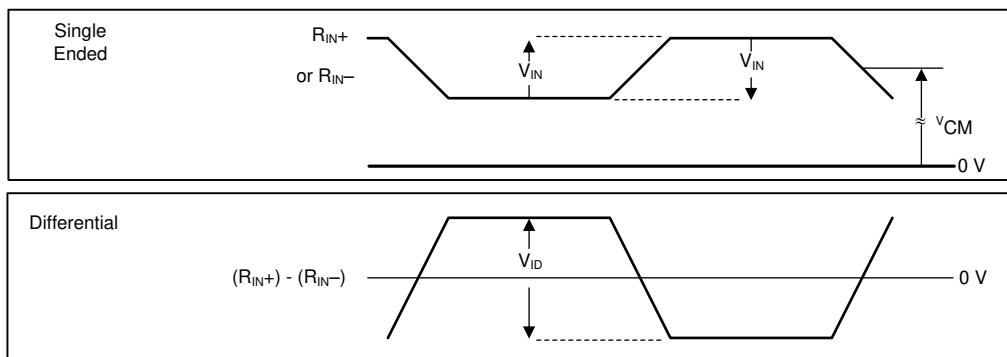


Figure 7-2. FPD-Link Receiver VID, VIN , VCM

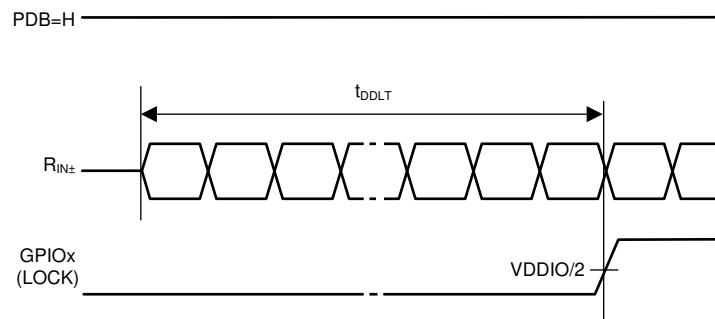


Figure 7-3. Deserializer Data Lock Time

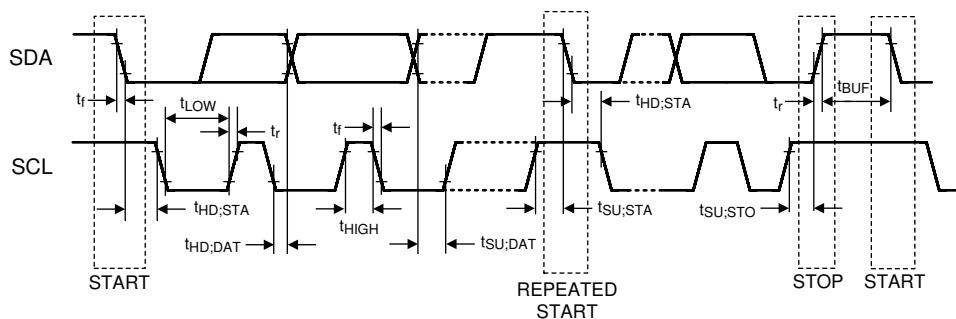
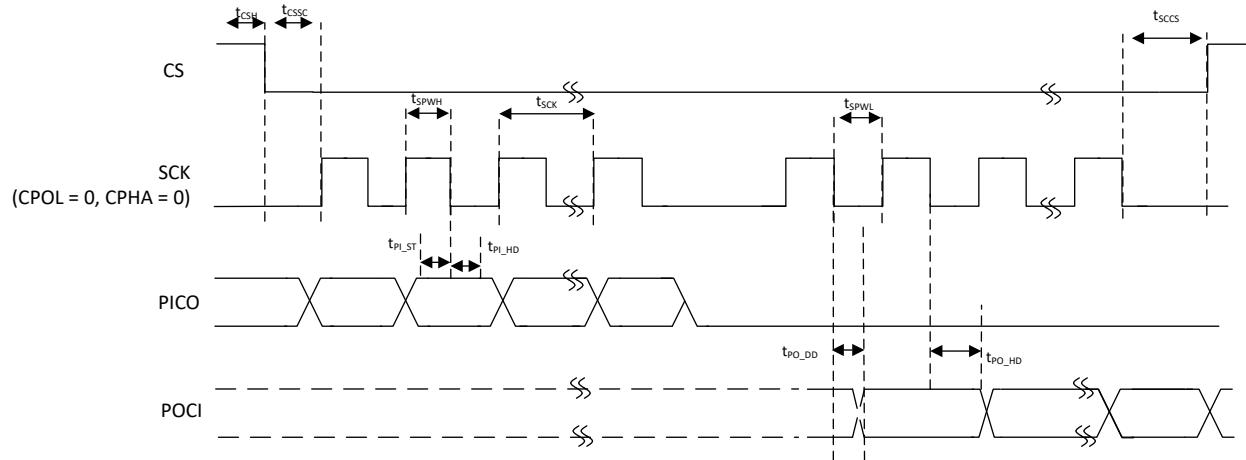
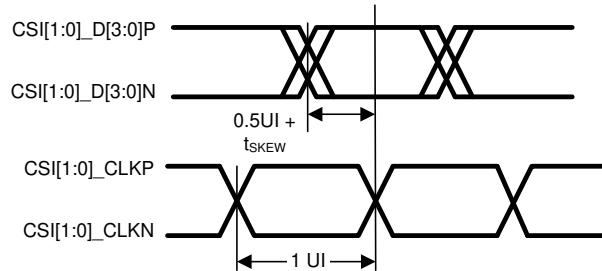
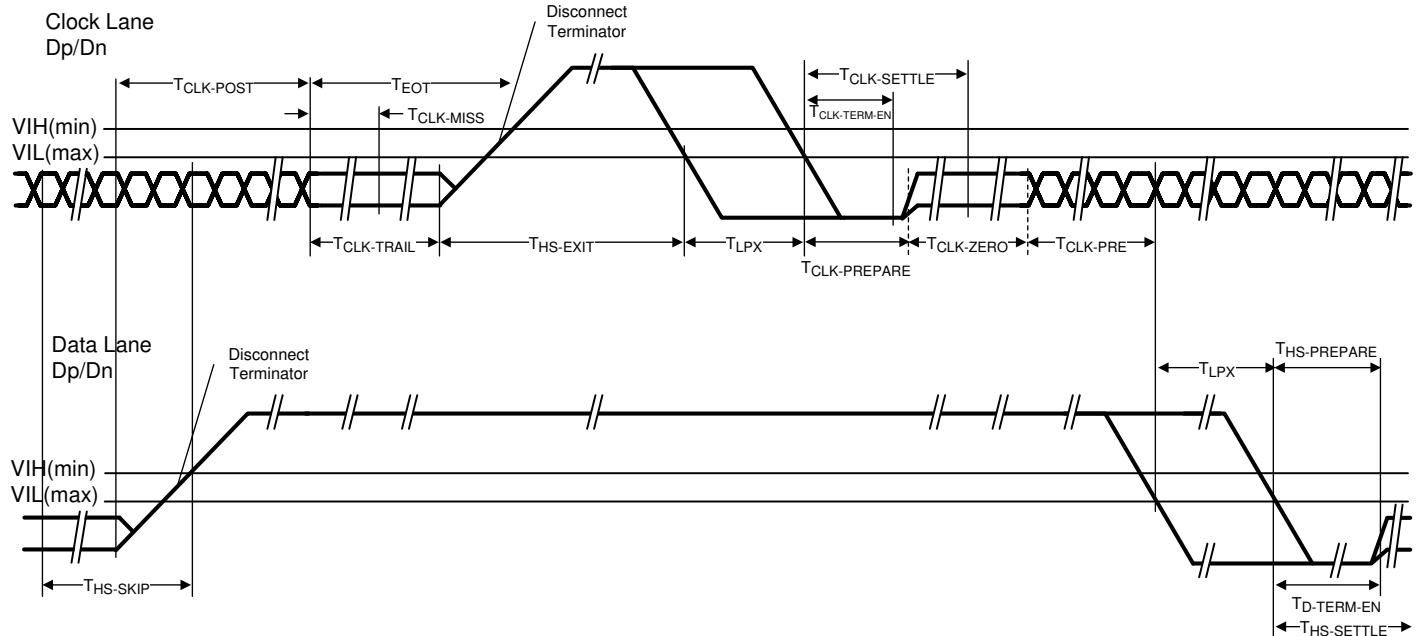


Figure 7-4. I2C Serial Control Bus Timing

**Figure 7-5. SPI Timing Diagram****Figure 7-6. Clock and Data Timing in HS Transmission****Figure 7-7. High Speed Data Transmission Burst**

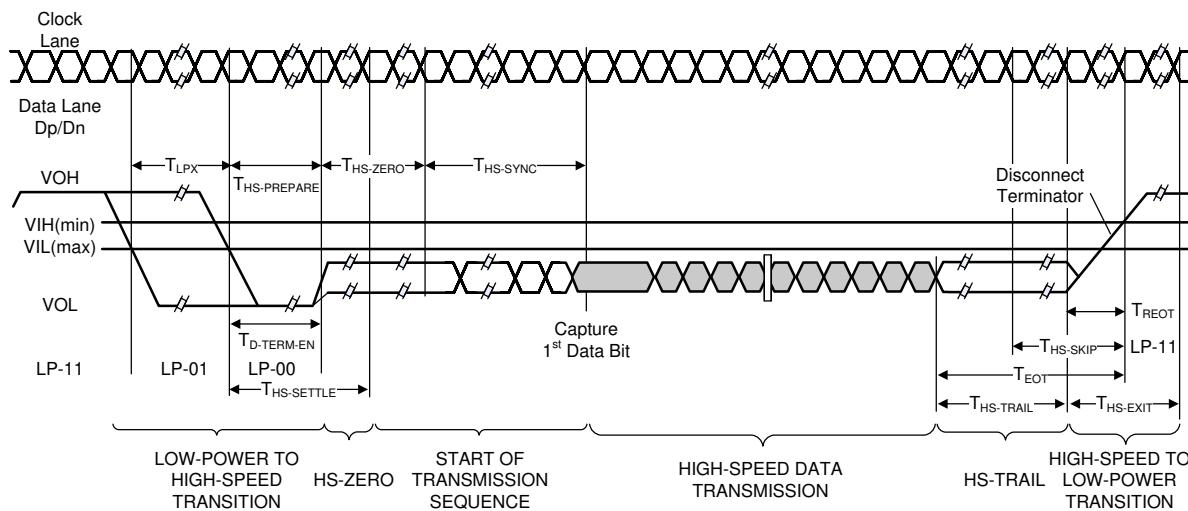


Figure 7-8. Switching the Clock Lane between Clock Transmission and Low-Power Mode

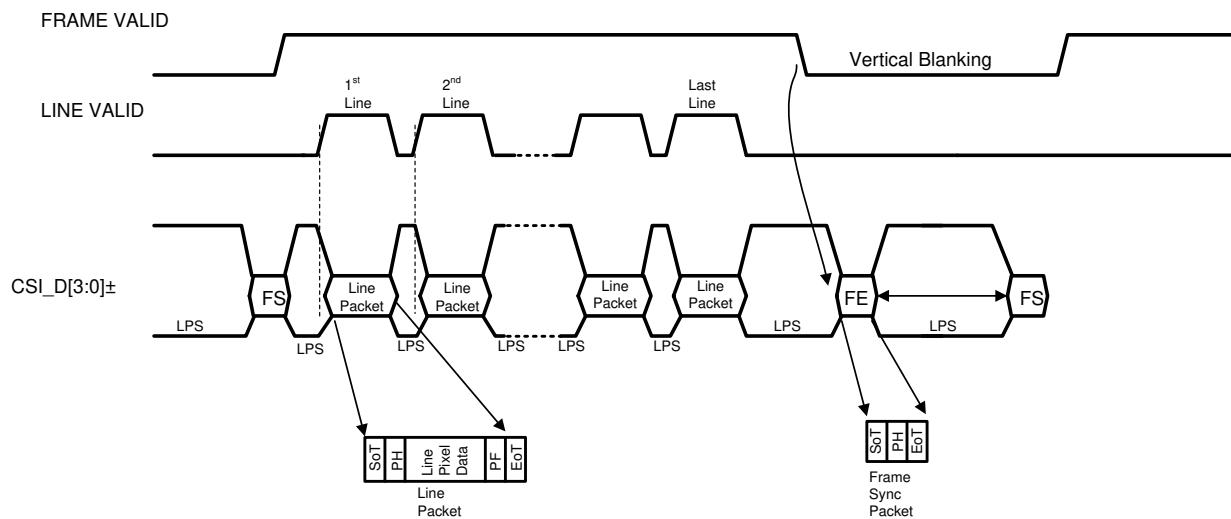


Figure 7-9. Long Line Packets and Short Frame Sync Packets

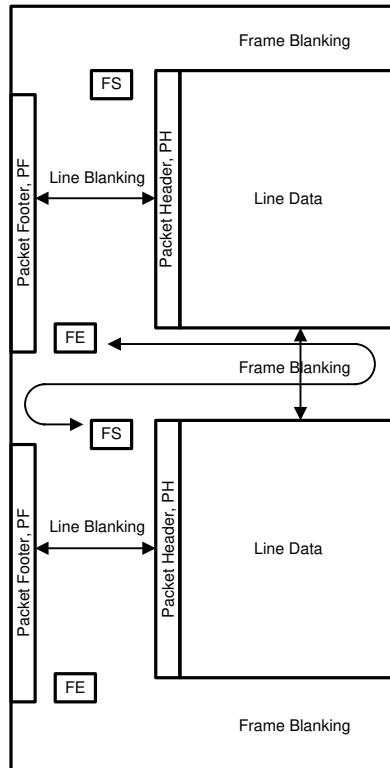
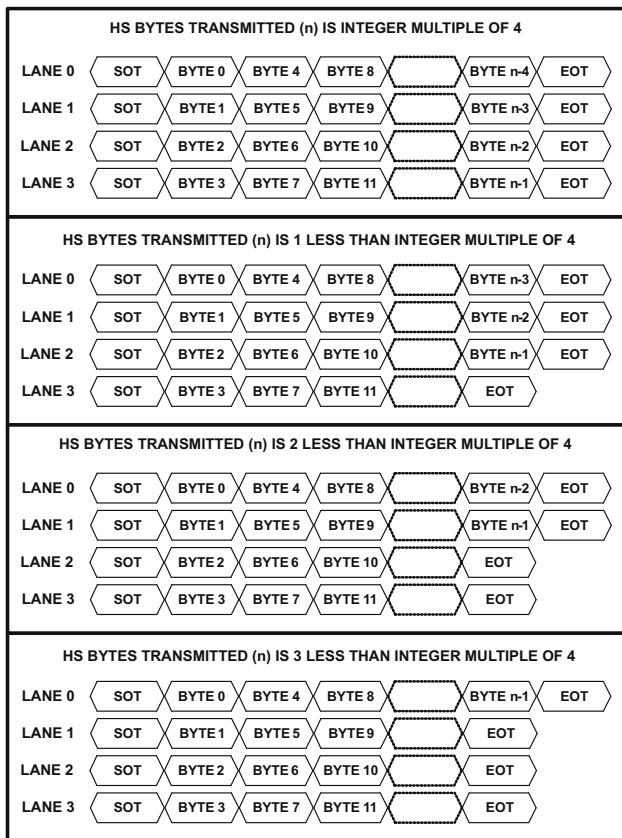
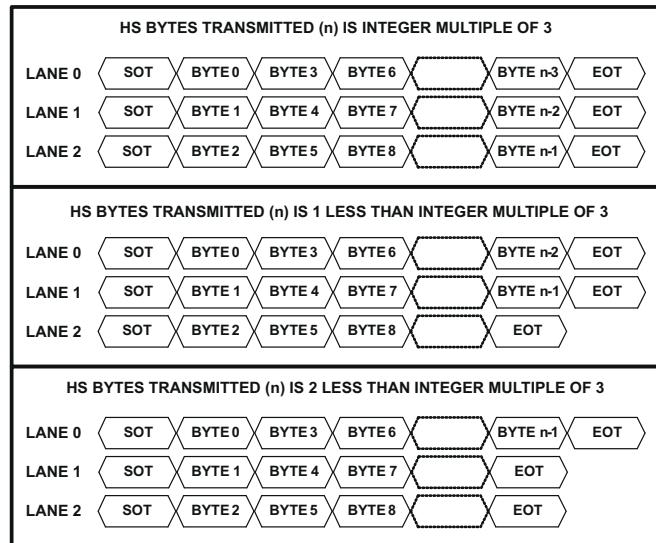


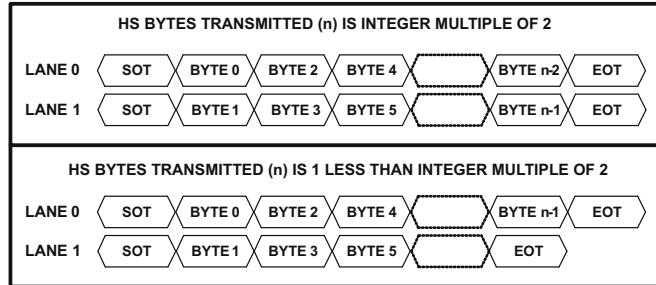
Figure 7-10. CSI-2 General Frame Format (Single Rx / VC)



4 CSI-2 Data Lane Configuration (default)



3 CSI-2 Data Lane Configuration



2 CSI-2 Data Lane Configuration

Figure 7-11. 4 MIPI Data Lane Configuration

8 Detailed Description

8.1 Overview

The deserializer accepts four camera inputs from a FPD-Link IV interface. The device combines data streams from multiple camera sources onto one or two MIPI CSI-2 port(s) with up to 4 data lanes per port. An additional CSI-2 output port can be used for replication of CSI-2 data from CSI-2 port 0 or CSI-2 port 1.

8.2 Functional Block Diagram

The deserializer aggregates up to four inputs acquired from a FPD-Link IV stream and transmitted over a MIPI camera serial interface (CSI-2). When coupled with FPD-Link IV or FPD-Link III serializers, the deserializer receives data streams from one or multiple imagers to be sent over to CSI transmitters.

The deserializer receives up to 7.55 Gbps of forward channel FPD-Link data from a compatible serializer. Data sent in the forward channel includes video payload, I2C, and information on diagnostics. This deserializer also provides up to 47.1875 Mbps of back channel data to the serializer, which consists of I2C, GPIO, and diagnostics information.

The deserializer provides two direct MIPI CSI-2 ports and one replicate MIPI CSI-2 port, configured for up to 4 lanes per port up to 2.5 Gbps per lane. It supports multiple data formats (programmable as RAW, YUV, RGB) and different camera resolutions. The CSI-2 TX module accommodates both image data and non-image data (including synchronization or embedded data packets).

The CSI-2 output interface combines each of the camera data streams into packets designated for each virtual channel. The output generated is composed of virtual channels to separate different streams to be interleaved. Each virtual channel is identified by a unique channel identification number in the packet header.

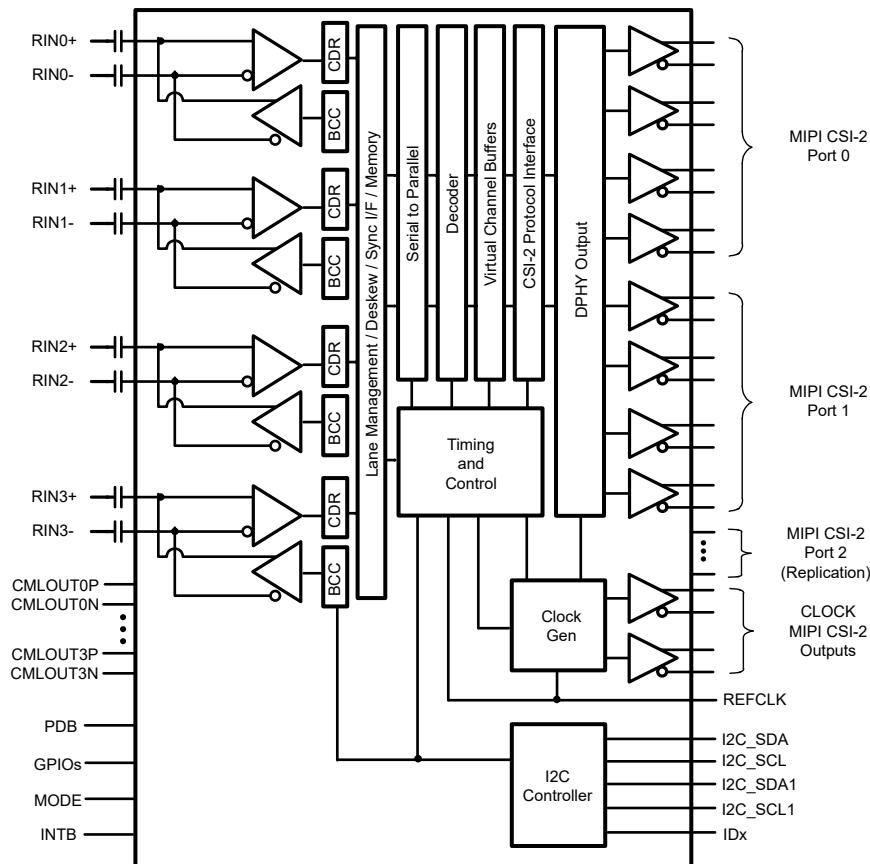


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Adaptive Equalizer

The receiver inputs provide an adaptive equalization filter in order to compensate for signal degradation from the interconnect components. In order to determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, ISI, and crosstalk need to be taken into consideration. The deserializer includes adaptive EQ control circuitry that adjusts various EQ parameters including gain, sampling position, DC offset, etc. This AEQ adaption continuously monitors cable characteristics for long-term cable aging and temperature changes and attempts to optimize the equalization setting. The adaptive equalizer algorithms does not require an unclocking event or errors to occur to achieve the optimal setting.

8.3.2 GPIO Support

The deserializer supports 10 GPIO pins which are programmable for use in multiple options through the GPIOx_PIN_CTL registers. Reg 0x01[5] (GPIO_HOLD_B) must be set to b'1. [Table 8-1](#) provides a list of alternatives each GPIO pin can be configured.

Table 8-1. GPIO Function

Pin Name	Default Value	Alternate1	Alternate2	Alternate3	Alternate4	Alternate5	Alternate6	Alternate7	Alternate8	Alternate9
GPIO[0]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync		INTB	CLKOUT	ExtVol0
GPIO[1]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync		INTB	CLKOUT	ExtVol1
GPIO[2]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync		INTB	CLKOUT	LineFault0
INTB/ GPIO[3]	INTB	GPIO	LOCK	PASS	LV/FV	FrameSync		INTB	CLKOUT	
LOCK/ GPIO[4]	OR RIN LOCK	GPIO	LOCK	PASS	LV/FV	FrameSync	PICO	INTB	CLKOUT	
GPIO[5]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync	POCI	INTB	CLKOUT	LineFault1
GPIO[6]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync	SCK	INTB	CLKOUT	LineFault2
GPIO[7]	GPIO	GPIO	LOCK	PASS	LV/FV	FrameSync	CS	INTB	CLKOUT	LineFault3
I2C_SC L1/ GPIO[9]	I2C_SC L1	GPIO	LOCK	PASS	LV/FV			INTB		
I2C_SC L1/ GPIO[10]	I2C_SC L1	GPIO	LOCK	PASS	LV/FV			INTB		

8.3.2.1 Alternative 1: GPIO

The deserializer supports 10 pins which are programmable for use in multiple options through the GPIOx_PIN_CTL registers. Note that GPIO[9] and GPIO[10] can only be configured as an output.

8.3.2.1.1 GPIO Configuration

Each GPIO pin has an input disable and a pulldown disable control bit. By default, the GPIO pin input paths are enabled and the internal pulldown circuit for the GPIO is enabled. For GPIO[0:2] and GPIO[4:7], the GPIO_INPUT_CTL (reg 0x0F) and GPIO_PD_CTL (reg 0xBE) registers allow control of the input enable and the pulldown respectively, GPIO[3] does not have an internal pull-down resistor. GPIO[9:10] do not have input functionality and can only be operated as outputs. For most applications, there is no need to modify the default register settings for the pull down resistors. The status HIGH or LOW of GPIO[0:7] may be read through the GPIO_PIN_STS. This register read operation provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

Individual GPIO output pin control is programmable through the GPIOx_PIN_CTL (reg 0x10-0x17, 0x89, 0x8A). To enable any of the GPIO as output, set bit 0 to b'1 in the respective register GPIOx_PIN_CTL after clearing the corresponding input enable bit in reg 0x0F and reg 0x8B.

```
WriteI2C(0x01, 0x20) # Release GPIO_HOLD
WriteI2C(0x0F, 0x00) # Set GPIOs as outputs
WriteI2C(0x10, 0x13) # Drive GPIO0 high
WriteI2C(0x11, 0x13) # Drive GPIO1 high
WriteI2C(0x12, 0x13) # Drive GPIO2 high
WriteI2C(0x15, 0x13) # Drive GPIO5 high
WriteI2C(0x16, 0x13) # Drive GPIO6 high
WriteI2C(0x17, 0x13) # Drive GPIO7 high
```

8.3.2.1.2 Forward Channel GPIO

When paired with a DS90UB971-Q1, DS90UB953(A)-Q1, or a DS90UB935-Q1, the deserializer can output GPIO data received from the forward channel. Each GPIO pin can be programmed for output mode and mapped to a serializer GPIO. The sampling frequency of the GPIOs is determined by the number of GPIOs used in the forward channel:

- If one linked GPIO is used, then the GPIO will be sampled every FPD-Link frame
- If two linked GPIOs are used, then the GPIOs will be sampled every two FPD-Link frames
- If four linked GPIOs are used, then the GPIOs will be sampled every five FPD-Link frames

When pairing with a DS90UB971-Q1 serializer, the sampling frequency and jitter are as follow:

Table 8-2. 7.55Gbps Forward Channel GPIO Timing

Number of Linked GPIOs	Typical Sampling Frequency (MHz)	Maximum Recommended Forward Channel GPIO Frequency (MHz)
1	188.75	47.1875
2	94.375	23.594
4	37.75	9.4375

When pairing with a DS90UB953(A)-Q1 or DS90UB935-Q1 serializer, the sampling frequency and jitter are as follow:

Table 8-3. 3.775Gbps Forward Channel GPIO Timing

Number of Linked GPIOs	Typical Sampling Frequency (MHz)	Maximum Recommended GPIO Frequency (MHz)
1	94.375	23.594
2	47.1875	11.797
4	18.875	4.719

When paired with a DS90UB951-Q1 serializer, the sampling frequency and jitter are as follow:

Table 8-4. 4.85Gbps Forward Channel GPIO Timing

Number of Linked GPIOs	Typical Sampling Frequency (MHz)	Maximum Recommended Forward Channel GPIO Frequency (MHz)
1	121.25	30.31
2	60.625	15.16
4	24.25	6.06

DS90UB913A-Q1 and DS90UB933-Q1 do not support forward channel GPIO.

8.3.2.1.3 Back Channel GPIO

The deserializer can input data on the GPIO pins to send on the back channel to all of its compatible remote serializers. Each GPIO pin can be programmed for input mode. In addition, the back channel for each FPD-Link IV port can be programmed to send any of the 10 GPIO pin data. Up to 4 GPIOs from the deserializer can be

sent mapped per back channel. The same GPIO pin can be connected to multiple back channel GPIO signals. The follow table provides the latency and typically jitter for the back channel GPIOs:

Table 8-5. Back Channel GPIO Timing

Back Channel Rate (MHz)	Sampling Frequency (kHz)	Maximum Recommended GPIO Frequency (kHz)	Typical Latency (μs)	Typical Jitter (μs)
47.1875	1572.92	393.23	1.27	.64
9.4375	314.58	78.65	6.36	3.18
2.3594	78.65	19.66	25.43	12.7

8.3.2.2 Alternative 2: LOCK

The GPIO pins can be configured to indicate LOCK status for each RX port. The LOCK status can be set to indicate whether a specific RX port is locked, or logical OR or AND of the enabled RX ports. Refer to GPIOx_PIN_CTL (reg 0x10-0x17, 0x89, 0x8A) to set a specific GPIO to indicate RX LOCK status.

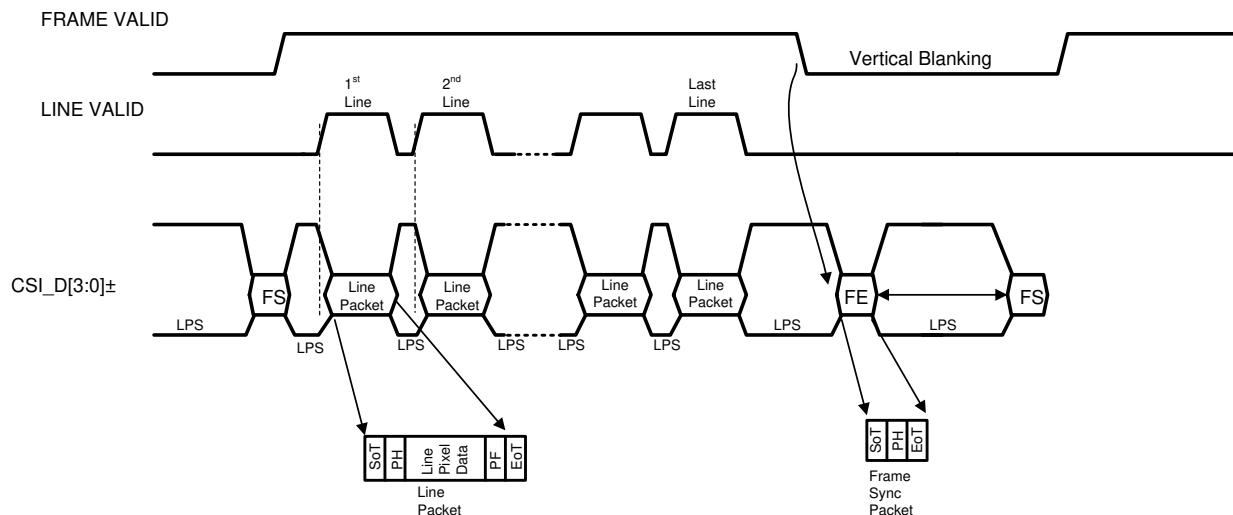
8.3.2.3 Alternative 3: PASS

PASS criteria can be set to indicate if a specific number of frames are received in a row, or if parity errors do not exceed the threshold value. The number of required valid video frames is programmable through the PASS_THRESH field in the PORT_PASS_CTL (reg 0x7D) register. The threshold can be programmed from 0 to 3 video frames. If set to 0, Pass will typically be indicated as soon as the FPD-Link receiver reports LOCK to the incoming signal. If set greater than 0, the receiver will require that number of valid frames before indicating PASS. Determination of valid frames will be dependent on the control bits in PORT_PASS_CTL. In the case of a parity error, when PASS_PARITY_ERR is set to b'1 forwarding will be enabled one frame early. To ensure at least one good frame occurs following a parity error the counter should be set to 2 or higher when PASS_PARITY_ERR is b'1.

The GPIO pins can be configured to indicate PASS status for each RX port or each CSI-2 port. Refer to GPIOx_PIN_CTL (reg 0x10-0x17, 0x89, 0x8A) to set a specific GPIO to indicate PASS status.

8.3.2.4 Alternative 4: Line Valid/Frame Valid (LV/FV)

The GPIO pins can be configured to indicate line valid and frame valid signals for a given RX port. When the RX port is connected to a DS90UB971-Q1, DS90UB953-Q1, DS90UB953A-Q1 or DS90UB935-Q1, line valid signal is high when a line packet is received, and frame valid signal is high when a frame is received. Refer to [Figure 8-2](#) for timing diagram of line valid and frame valid in relations to the CSI-2 data.

**Figure 8-2. Line Packets and Frame Sync Packets**

When the RX port is connected to a DS90UB933-Q1 or a DS90UB913A-Q1, frame valid is equivalent to a Vertical Sync (VSYNC) while the line valid is equivalent to a Horizontal Sync (HSYNC) input. Refer to GPIOx_PIN_CTL (reg 0x10-0x17, 0x89, 0x8A) to set a specific GPIO to indicate LV or FV.

8.3.2.5 Alternative 5: FrameSync

A frame synchronization signal (FrameSync) can be sent via the back-channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the deserializer and mapping that GPIO to a back channel GPIO on one or more of the FPD-Link ports.

The second option is to have the deserializer internally generate a FrameSync signal to send via GPIO to one or more of the attached Serializers.

FrameSync signaling on the four back channels is synchronous. Thus, the FrameSync signal arrives at each of the four serializers with limited skew.

8.3.2.5.1 External FrameSync Control

In External FrameSync mode, an external signal is input to the deserializer via one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached serializers via a GPIO signal in the back channel.

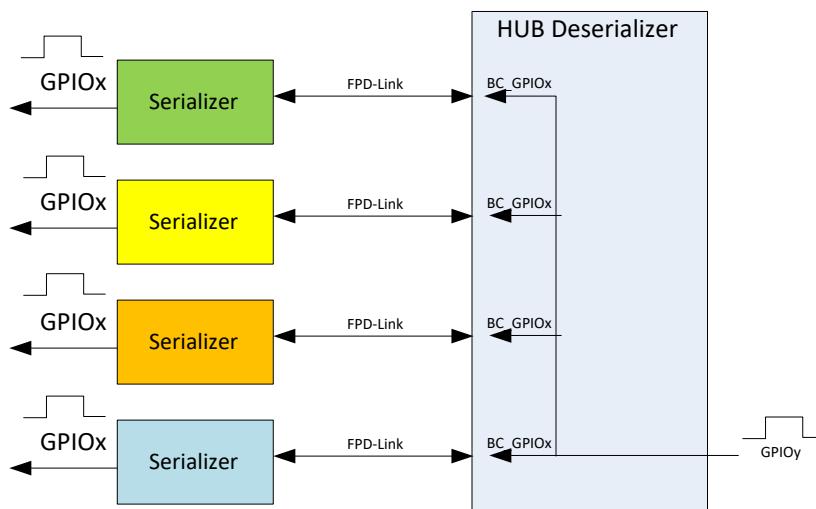


Figure 8-3. External FrameSync

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL register to a value between 0x8 (GPIO0 pin) to 0xF (GPIO7 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on a port's BC_GPIOx signal, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register should be programmed for that port to select the FrameSync signal.

8.3.2.5.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD-Link IV Serializers via a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL 0x18, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x19–0x1A registers. The resolution of the FrameSync generator clock (FS_CLK_PD) is equivalent to the back channel frame period. Table 8-6 shows the back channel frame period for different back channel rates.

Table 8-6. Back Channel Frame Period Table

Back Channel Rate (Mbps)	Back Channel Frame Period FS_CLK_PD (us)
47.1875	0.636
9.4375	3.18

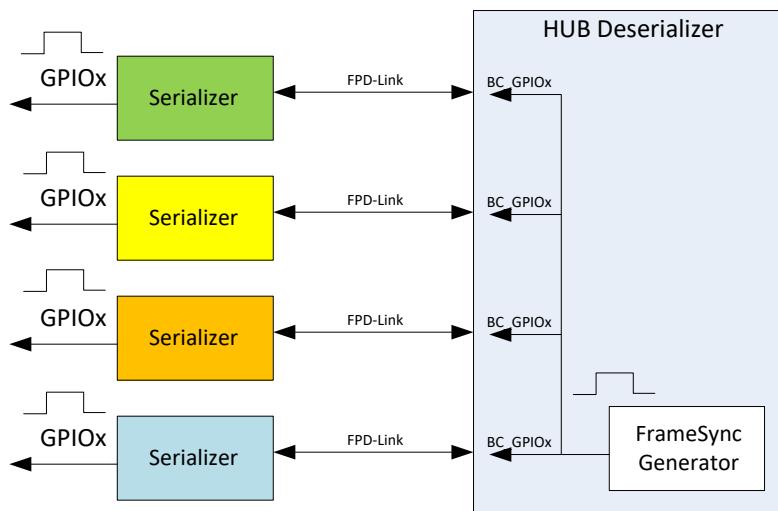
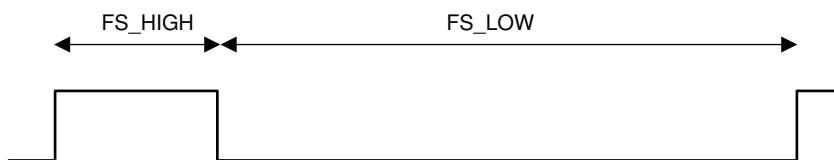
Table 8-6. Back Channel Frame Period Table (continued)

Back Channel Rate (Mbps)	Back Channel Frame Period FS_CLK_PD (us)
2.3594	12.72

The total period of the FrameSync in counts is equal to (1 sec / desired frame sync frequency in HZ) / FS_CLK_PD in sec.

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions. Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the 25 MHz oscillator used as the reference clock.

**Figure 8-4. Internal FrameSync**

$FS_LOW = FS_LOW_TIME * FS_CLK_PD$
 $FS_HIGH = FS_HIGH_TIME * FS_CLK_PD$
 where FS_CLK_PD is the resolution of the FrameSync generator clock

Figure 8-5. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable High/Low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 2.3594 Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=0x0
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD (back channel frame period) of 12.72 us.

The total period of the FrameSync is (1 sec / 60 hz) / 12.72 μ s or approximately 1,310 counts.

For a 10% duty cycle, set the high time to 131 (0x0083) cycles, and the low time to 1,179 (0x049B) cycles:

- FS_HIGH_TIME_1: 0x19=0x00
- FS_HIGH_TIME_0: 0x1A=0x83
- FS_LOW_TIME_1: 0x1B=0x04
- FS_LOW_TIME_0: 0x1C=0x9B

8.3.2.5.2.1 Code Example for Internally Generated FrameSync

```

WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # FrameSync signal; Device Status; Enabled
WriteI2C(0x19,0x00) # FS_HIGH_TIME_1
WriteI2C(0x1A,0x83) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x04) # FS_LOW_TIME_1
WriteI2C(0x1C,0x9B) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
# On Serializer
WriteI2C(0x0E,0xF0) # GPIO_INPUT_CTL: Set remote GPIOs as outputs

```

8.3.2.6 Alternative 6: SPI

The deserializer GPIO[4], GPIO[5], GPIO[6], and GPIO[7] can be configured to a local 4 wire SPI interface. The SPI interface is a peripheral interface that includes POCI (Peripheral Out Controller In), PICO (Peripheral In Controller Out), SCK (synchronous clock for data transfer), and CS (Chip Select). SPI is only available for local writes to the deserializer. It cannot be used across the link. Remote SPI transactions to the serializer or the remote peripherals is not available. When SPI is enabled, I2C port 1 will not be available.

To enter SPI mode, the GPIO hold mode should be disabled by setting the GPIO_HOLD_B field in RESET_CTL (reg 0x01) to b'1, and then SPI_MODE_EN field in GENERAL_CFG (reg 0x02) should be set to b'1.

SPI Controller timing should be evaluated and account for SPI Tck rate, PCB layout matching SCK to Data, and the SPI Peripheral timing parameters. The Setup time and Hold time of the Peripheral input is evaluated for SPI Write cycles. The Setup time and Hold time of the Controller input is evaluated for SPI Read cycles. Note: the SPI Write PICO data line, and SPI Read POCI data line are independent.

8.3.2.7 Alternative 7: Interrupt (INTB)

The GPIO pins can be configured as interrupt output pins. By default, GPIO[3] is set as an interrupt pin. To enable interrupts on other pins, set the output source in GPIOx_PIN_CTL for the desired GPIO. Interrupts can be brought out as controlled by the INTERRUPT_CTL (reg 0x23) and INTERRUPT_STS (reg 0x24). The main interrupt control registers provide control and status for interrupts from the individual sources. Sources include each RX port as well as the two independent CSI-2 transmit ports. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion. For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the interrupt pin does not indicate the interrupt condition.

8.3.2.8 Alternative 8: CLKOUT

The GPIO pins can be configured as CLKOUT pins to provide the reference clock output of 25MHz. This feature is useful when there are multiple deserializer on the same board. The CLKOUT of device can be routed to the REFCLK of another deserializer. To enable CLKOUT on a GPIO, set the output source in GPIOx_PIN_CTL for the desired GPIO.

8.3.2.9 Alternative 9: External Analog Monitoring

The GPIO pins can be configured to sense external voltages and various line faults. When a GPIO is set as an external analog monitor pin, it disregards the setting in `GPIOx_PIN_CTL`. `GPIO[0]` and `GPIO[1]` can be used to monitor external voltages. `GPIO[2]`, `GPIO[5]`, `GPIO[6]`, and `GPIO[7]` can be used to monitor line fault. Refer to [Section 8.3.5.5.3](#) and [Section 8.3.5.6](#) for more information.

8.3.3 Channel Monitor Loop-Through Output Driver

The deserializer includes an internal Channel Monitor Loop-through output on the `CMLOUTP/N` pins. The `CMLOUTP/N` supplies a buffered loop-through output driver for each RX receiver channels, thus providing the recovered input of the deserializer signal. The `CMLOUTP/N` pins can be used to drive another deserializer running at the same forward channel rate. If doing more than one hop (multiple `CMLOUT` loop-thru chains), all the deserializers will need to have a common reference clock. This feature is only supported when using FPD-Link IV CDR.

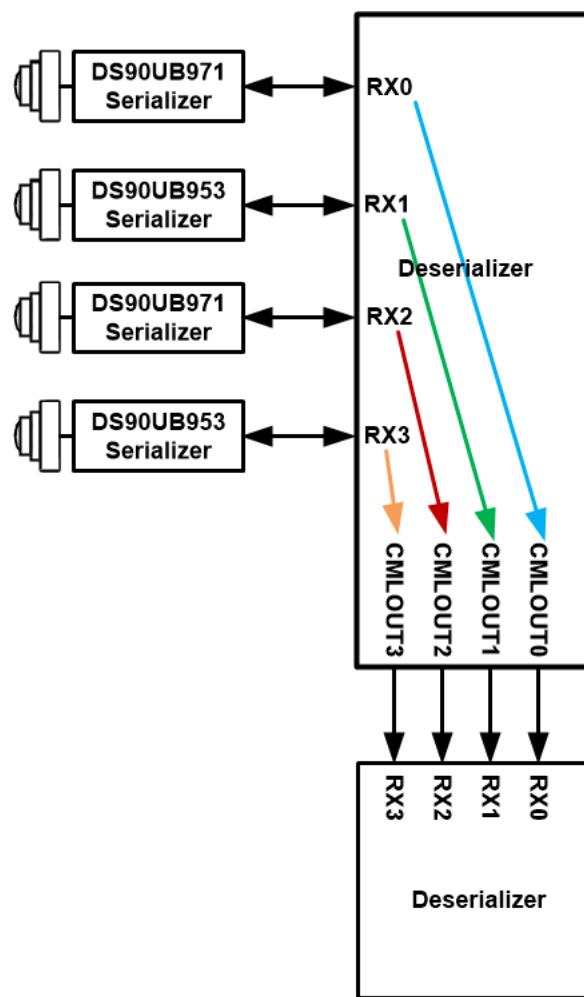


Figure 8-6. Example CMLOUT Connection

The deserializer receiving the imager data and outputting the same forward channel data needs to be configured to enable loop-thru driver. The deserializer receiving the `CMLOUT` loop-thru data needs to be configured to turn off the back channel by setting register `0x58 = 0x00` for each RX port.

Follow the example code below to enable `CMLOUT` for `RX0` in FPD-Link III mode (3.775Gbps rate). The `CMLOUT` should only be enabled after `LOCK` is established between the serializer and deserializer. Note that the steps for enabling each port require setting bit 7 within the `0xE1` register without changing the default values in the other bits within the register (which may vary from device to device or port to port based on trim). So

each port must be enabled individually with the below steps selecting only one RX port at a time. If the RX port which is forwarded through CMLOUT loses LOCK, or if a soft reset is issued to the device via register 0x01, then CMLOUT should be disabled and re-enabled to prevent any FIFO errors in the forwarded CMLOUT stream.

FPD-Link III (3.775Gbps) CMLOUT Enable Example:

```
WriteI2C(0x4C,0x01)    # FPD4 RX Port Select
regE1 = ReadI2C(0xE1)  # Read back trim value from 0xE1
regE1 = regE1 | 0x80   # Set bit 7 = 1 without modifying other bits in the register
WriteI2C(0xE1,regE1)   # Enable CMLOUT clock tree
WriteI2C(0xE2,0x40)    # Set CMLOUTDIV = 2 for FPD III mode
WriteI2C(0xE0,0xFF)    # Enable CMLOUT FPD Rx
```

FPD-Link IV (7.55Gbps) CMLOUT Enable Example:

```
WriteI2C(0x4C,0x01)    # FPD4 RX Port Select
regE1 = ReadI2C(0xE1)  # Read back trim value from 0xE1
regE1 = regE1 | 0x80   # Set bit 7 = 1 without modifying other bits in the register
WriteI2C(0xE1,regE1)   # Enable CMLOUT clock tree
WriteI2C(0xE0,0xFF)    # Enable CMLOUT FPD Rx
```

8.3.4 MIPI Camera Serial Interface 2 (CSI-2)

8.3.4.1 CSI-2 Protocol

The deserializer implements High-Speed mode to forward CSI-2 Low Level Protocol data compliant with CSI-2 version 2.1. This includes features as described in the Low Level Protocol section of the MIPI CSI-2 Specification. It supports short and long packet formats.

The feature set of the protocol layer implemented by the CSI-2 TX is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to sixteen interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start and line end information
- Descriptor for the type, pixel depth and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

[Figure 8-7](#) shows the CSI-2 protocol layer with short and long packets.

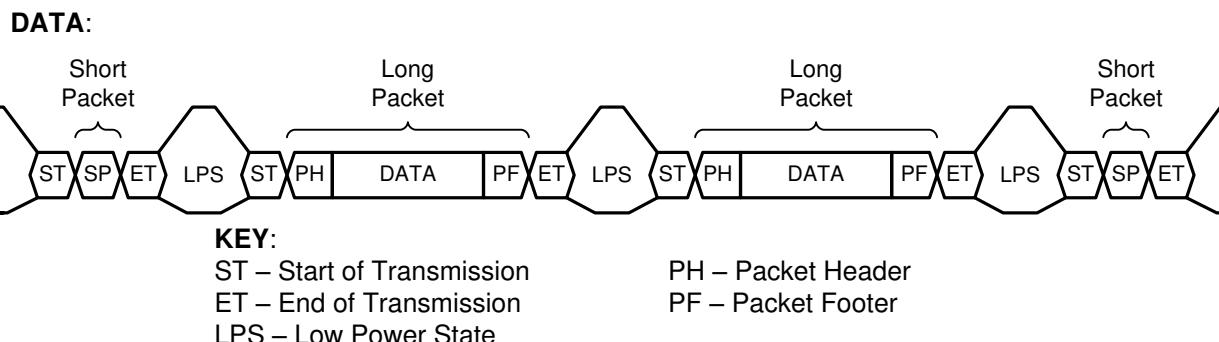
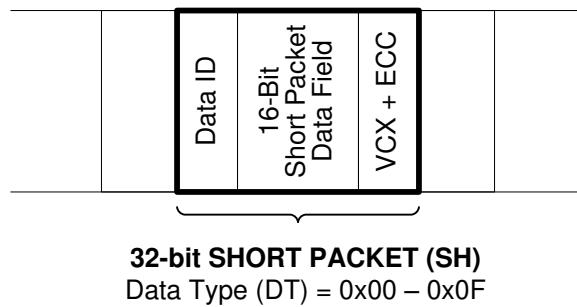


Figure 8-7. CSI-2 Protocol Layer With Short and Long Packets

Note DS90UB9702-Q1 DPHY ports do not support ULPS. To support lower power consumption when the ports are unused, they may be disabled in register 0x33.

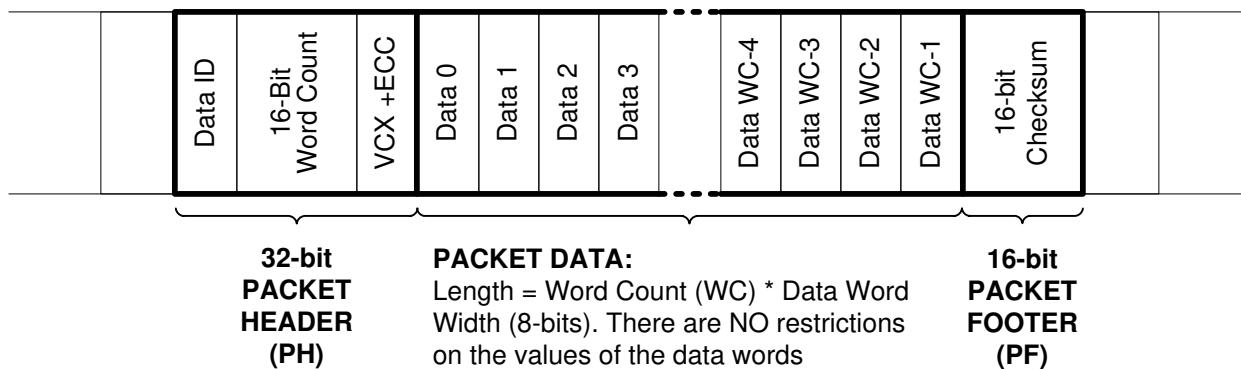
8.3.4.2 CSI-2 Short Packet

The short packet provides frame or line synchronization. [Figure 8-8](#) shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

**Figure 8-8. CSI-2 Short Packet Structure**

8.3.4.3 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and a 2-bit VCX and 6-bit ECC. The packet footer has one element, a 16-bit checksum. [Figure 8-9](#) shows the structure of a long packet.

**Figure 8-9. CSI-2 Long Packet Structure****Table 8-7. CSI-2 Long Packet Structure Description**

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	VCX + ECC	2 + 6	2-bit virtual channel extension (VCX) and 6-bit ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC * 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

8.3.4.4 CSI-2 Data Identifier

The deserializer MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in [Figure 8-10](#). The least significant 2-bit of the virtual channel ID is contained in the 2 MSbs of the data identifier byte, and the most significant 2-bit of the virtual channel ID is in the VCX field in the long packet. The receiver extract the virtual channel ID from the data identifier and VCX. The value of the data type is contained in the 6 LSbs of the data identifier byte.

In DVP mode, for each RX Port, register defines with which channel and data type the context is associated:

- RAW1x_VC[7:6] field defines the associated virtual ID transported by the CSI-2 protocol from the camera sensor.
- RAW1x_ID[5:0] field defines the associated data type. The data type is a combination of the data type transported by the CSI-2 protocol.

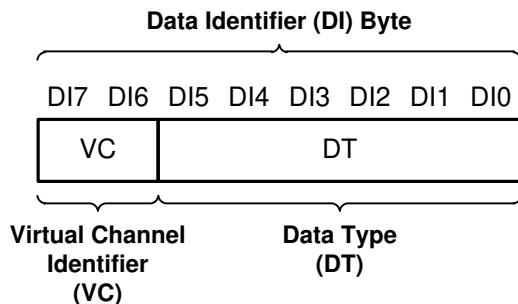


Figure 8-10. CSI-2 Data Identifier Structure

8.3.4.5 CSI-2 Virtual Channel Mapping

The CSI-2 protocol layer transports virtual channels. The purpose of virtual channels is to separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. Therefore, a CSI-2 TX context can be associated with a virtual channel and a data type. Virtual channels are defined by a 4-bit field. This channel identification number is encoded in the 4-bit code.

The CSI-2 TX transmits the channel identifier number and multiplexes the interleaved data streams. The CSI-2 TX supports up to sixteen concurrent virtual channels.

The deserializer provides per-port Virtual Channel ID mapping. If the deserializer is in CSI-2 mode, for each FPD-Link input port, separate mapping may be done for each input VC-ID to any of the sixteen VC-ID values. The mapping is controlled by the VC_ID_MAP (0xA0 - 0xA7) registers. This function sends the output as a time-multiplexed CSI-2 stream, where the video sources are differentiated by the virtual channel. Virtual channel IDs are 4-bit long and can support channel ID ranging from 0 to 15. For example, 0xA0[3:0] remaps incoming virtual channel of 0; 0xA0[7:4] remaps incoming virtual channel of 1, and 0xA7[7:4] remaps virtual channel of 15.

FPD-Link III CSI-2 serializers are compliant to CSI-2 v1.3 and only have 2-bit virtual channel identifiers. The deserializer will interpret these 2-bit values as 4-bit values by duplicating the two bits. Therefore the 2-bit values are interpreted as 4-bit values as follows:

- 2-bit VCID 0 becomes 4-bit VCID 0
- 2-bit VCID 1 becomes 4-bit VCID 5
- 2-bit VCID 2 becomes 4-bit VCID A
- 2-bit VCID 3 becomes 4-bit VCID F

In DVP mode, only four virtual channels are supported: 0, 1, 2, and 3. The VC-ID of the incoming video data is set in RAW10_VC (reg 0x70[7:6]) in RAW10 mode and RAW12_VC (reg 0x71[7:6]) in RAW12 mode.

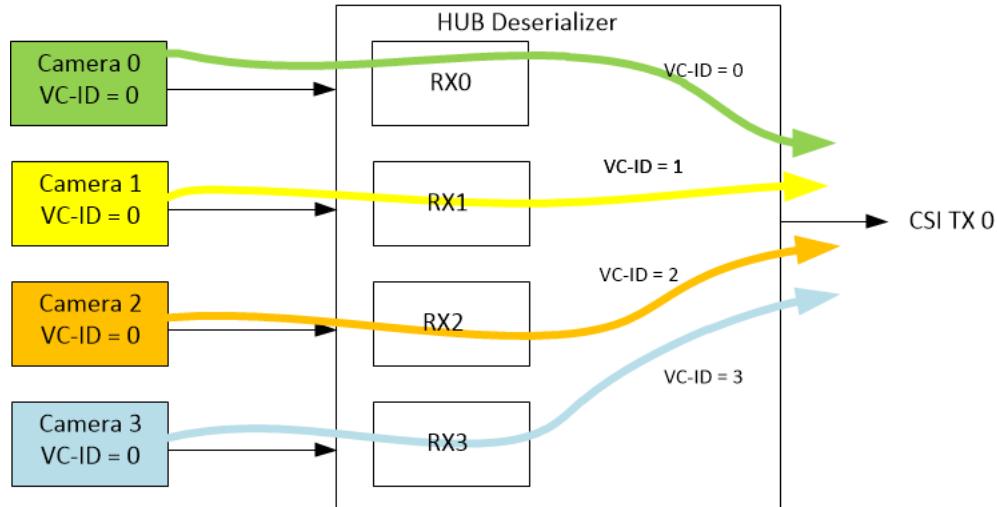
8.3.4.5.1 Example 1

The deserializer is receiving data from cameras attached to each port. Each port is sending a video stream using VC-ID of 0. The deserializer can be configured to re-map the incoming VC-IDs to ensure each video stream has a unique ID. The direct implementation would map incoming VC-ID of 0 for RX Port 0, VC-ID of 1 for RX Port 1, VC-ID of 2 for RX Port 2, and VC-ID of 3 for RX Port 3. In this configuration, first select the RX port via register 0x4C (i.e. Reg 0x4C = 0x01 indicates read/write from RX Port 0). Then set register 0xA0[3:0] to the desired VC-ID to be outputted. Repeat this process for all the RX ports.

```

WriteI2C(0x4C,0x01) #Select RX0
WriteI2C(0xA0,0x10) #Remap VC-ID 0 to VC-ID 0
WriteI2C(0x4C,0x11) #Select RX1
WriteI2C(0xA0,0x11) #Remap VC-ID 0 to VC-ID 1
WriteI2C(0x4C,0x24) #Select RX2
WriteI2C(0xA0,0x12) #Remap VC-ID 0 to VC-ID 2
WriteI2C(0x4C,0x36) #Select RX3
WriteI2C(0xA0,0x13) #Remap VC-ID 0 to VC-ID 3

```

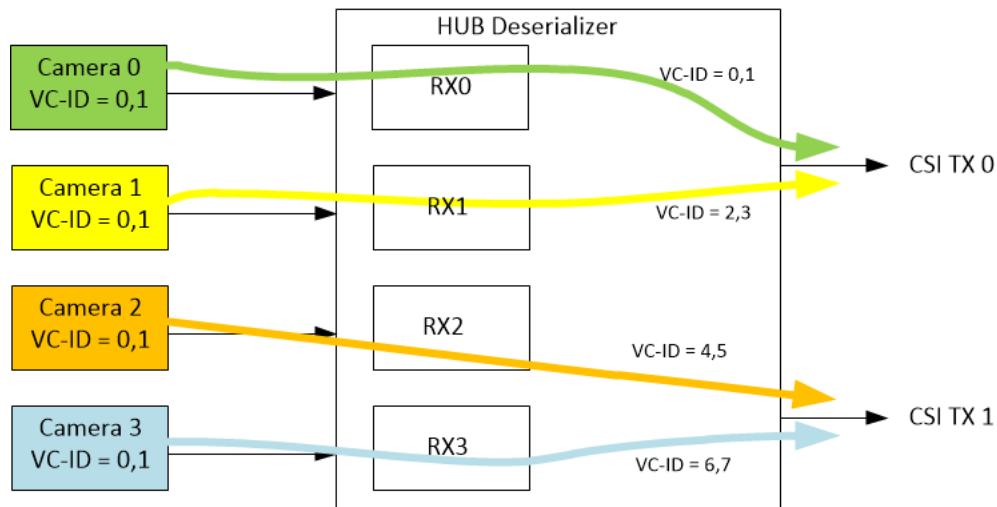
**Figure 8-11. VC-ID Mapping Example 1****8.3.4.5.2 Example 2**

The deserializer is receiving data from cameras attached to each port. Each port is sending a video stream using VC-ID of 0 and 1. The deserializer can be configured to re-map the incoming VC-IDs and distribute to different CSI Transmitters. This implementation maps incoming VC-IDs of 0 and 1 to 0 and 1 for RX0, 2 and 3 for RX1, 4 and 5 for RX2, and 6 and 7 for RX3. RX Ports 0 and 1 are assigned to CSI Transmitter 0 and RX Ports 2 and 3 are assigned to CSI Transmitter 1. In this configuration, first select the RX port via register 0x4C (i.e. Reg 0x4C = 0x01 indicates read/write from RX Port 0). Then set register 0xA0[3:0], which re-maps VC-ID of 0, to a new VC-ID; similarly, set register 0xA0[7:4], which re-maps VC-ID of 1, the desired VC-ID to be outputted. Repeat this process for all the RX ports.

```

WriteI2C(0x4C,0x01) #Select RX0
WriteI2C(0xA0,0x10) #Remap VC-ID 0 to VC-ID 0, VC-ID 1 to VC-ID 1
WriteI2C(0x4C,0x12) #Select RX1
WriteI2C(0xA0,0x32) #Remap VC-ID 0 to VC-ID 2, VC-ID 1 to VC-ID 3
WriteI2C(0x4C,0x24) #Select RX2
WriteI2C(0xA0,0x54) #Remap VC-ID 0 to VC-ID 4, VC-ID 1 to VC-ID 5
WriteI2C(0x4C,0x36) #Select RX3
WriteI2C(0xA0,0x76) #Remap VC-ID 0 to VC-ID 6, VC-ID 1 to VC-ID 7

```

**Figure 8-12. VC-ID Mapping Example 2**

8.3.4.6 CSI-2 Skew Calibration

The deserializer supports initial and periodic skew calibration of the CSI-2 TX output ports. This feature is required when operating at a DPHY CSI-2 output rate of above 1.5Gbps. Skew calibration can be enabled in CSI_CAL_EN field in CSI_CTL (reg 0x33). Additional skew calibration parameters can be controlled in CSI_CTL2 (reg 0x34). A single skew calibration pattern will be sent the transmitter goes to an idle state, whereas periodic pattern will send following each FrameEnd packet. The length of the pattern is adjustable in CSI_CAL_LEN.

8.3.4.7 CSI-2 Transmitter Frequency

The CSI-2 transmitters may operate at 400 Mbps, 800 Mbps, 1.2Gbps, 1.5Gbps, 1.6 Gbps, or 2.5Gbps. All CSI-2 transmitters will be running at the same rate. The transmitter frequency should not be changed while transmitter is operational. The examples below show how to set different CSI rates:

```
# Set CSI Transmitter to 400Mbps
WriteI2C(0x1F,0x03)
WriteI2C(0xC9,0x10)
WriteI2C(0xB0,0x1C)
WriteI2C(0xB1,0x92)
WriteI2C(0xB2,0xA0)
```

```
# Set CSI Transmitter to 800Mbps
WriteI2C(0x1F,0x02)
WriteI2C(0xC9,0x10)
WriteI2C(0xB0,0x1C)
WriteI2C(0xB1,0x92)
WriteI2C(0xB2,0x90)
WriteI2C(0xB1,0x4F)
WriteI2C(0xB2,0x2A)
WriteI2C(0xB1,0x4B)
WriteI2C(0xB2,0x2A)
```

```
# Set CSI Transmitter to 1200Mbps
board.WriteI2C(0x1F,0x01)
board.WriteI2C(0xC9,0x18)
board.WriteI2C(0xB0,0x1C)
board.WriteI2C(0xB1,0x92)
board.WriteI2C(0xB2,0x90)
```

```
# Set CSI Transmitter to 1500Mbps
WriteI2C(0x1F,0x00)
WriteI2C(0xC9,0x0F)
WriteI2C(0xB0,0x1C)
WriteI2C(0xB1,0x92)
WriteI2C(0xB2,0x80)
```

```
# Set CSI Transmitter to 1600Mbps
WriteI2C(0x1F,0x00)
WriteI2C(0xC9,0x10)
WriteI2C(0xB0,0x1C)
WriteI2C(0xB1,0x92)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x4B)
WriteI2C(0xB2,0x2A)
```

```
# Set CSI Transmitter to 2500Mbps
WriteI2C(devAddr,0x1F,0x10)
WriteI2C(devAddr,0xC9,0x19)
WriteI2C(devAddr,0xB0,0x1C)
WriteI2C(devAddr,0xB1,0x92)
WriteI2C(devAddr,0xB2,0x80)
```

8.3.4.8 CSI-2 Video Buffers

The deserializer implements four video line buffer/FIFO, one for each RX channel. The video buffers provide storage of data payload and forward requirements for sending multiple video streams on the CSI-2 transmit ports. The total line buffer memory size is a 16-kB block for each RX port.

The CSI-2 transmitter waits for an entire packet to be available before pulling data from the video buffers. Contact TI for details on how to calculate aggregation bandwidth for multi-sensor applications.

8.3.4.9 CSI-2 Line Count and Line Length

In CSI-2 mode, the deserializer counts the number of long packets to determine line count on LINE_COUNT_1/0 (reg 0x73 and reg 0x74). For line length, deserializer generates the word count field in the CSI-2 header on LINE_LEN_1/0 (reg 0x75 and reg 0x76). The unit for line length is in byte and can be converted to pixel by multiplying the value in byte by 8 bits/byte and dividing the result by number of bits per pixel (bpp).

In DVP mode, the line valid count within a frame is used to provide LINE_COUNT_1/0 (reg 0x73 and reg 0x74) and LINE_LEN_1/0 (reg 0x75 and reg 0x76).

8.3.4.10 CSI-2 Forwarding

The deserializer CSI-2 transmitters support aggregation of multiple RX video inputs. The deserializer supports two major types of forwarding methods: best-effort round robin and synchronized forwarding. Round robin forwarding does not require the input cameras to be synchronized and relies on assigning different virtual IDs to differentiate between multiple camera streams. This forwarding method can be further broken into direct and exclusive forwarding. Synchronized forwarding requires the cameras to be synchronized, usually by providing a common FrameSync signal to the cameras. There are three different types of synchronized forwarding, including basic, line-interleave, and line-concatenation forwarding.

8.3.4.10.1 Best-Effort Round Robin CSI-2 Forwarding

By default, the round-robin (RR) forwarding of packets use standard CSI-2 method of video stream determination. No special ordering of CSI-2 packets are specified, effectively relying on the Virtual Channel Identifier (VC) and Data Type (DT) fields to distinguish video streams. Each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel is also supported in this mode.

The forwarding engine forwards packets as they become available to the forwarding engine. In the case where multiple packets may be available to transmit, the forwarding engine typically operates in an RR fashion based on the input port from which the packets are received.

Best-effort CSI-2 RR forwarding has the following characteristics and capabilities:

- Uses Virtual Channel ID to differentiate each video stream
- Separate Frame Synchronization packets for each VC
- No synchronization requirements

This mode of operation allows input RX ports to have different video characteristics and there is no requirement that the video be synchronized between ports. The attached video processor would be required to properly decode the various video streams based on the VC and DT fields.

Best-effort forwarding is enabled by setting the CSIx_RR_FWD bits in the FWD_CTL2 register 0x21.

8.3.4.10.1.1 CSI-2 Direct Forwarding

Direct forwarding is a type of best-effort round robin CSI-2 forwarding. Video stream forwarding is handled by the forwarding control in the deserializer on FWD_CTL1 register 0x20. The forwarding control pulls data from the video buffers for each FPD-Link IV RX port and forwards the data to one of the CSI-2 output interfaces. Forwarding from RX input ports may be disabled using per-port controls. Each of the forwarding engines may be configured to pull data from any of the four video buffers, although the buffer from each RX port may only be assigned to one CSI-2 Transmitter at a time. For example, if the input stream from RX0 can only be sent to

either CSI port 0 or CSI port 1. It cannot be sent to both CSI ports. The code below shows an example of direct forwarding.

```
WriteI2C(0x32,0x03) #Read CSI Port 0, Write CSI Ports 0 and 1
WriteI2C(0x20,0xF0) #Disable RX port forwarding
WriteI2C(0x33,0x03) #Enable CSI ports 0 and 1, set continuous clock
WriteI2C(0x20,0x0C) #Forward RX Port 0 & 1 to CSI Port 0 and RX Port 2 & 3 to CSI Port 1
```

8.3.4.10.1.2 CSI-2 Exclusive Forwarding

Exclusive forwarding is another type of best-effort round robin CSI-2 forwarding. It is used to aggregate the inputs from RX ports to output them to both CSI ports 0 and 1. Instead of directly forwarding the CSI data in FWD_CTL1 register 0x20, which only allows an RX port to be forwarded to either CSI0 or CSI1, the user can optionally forward a combination of RX ports to each CSI port. To enable CSI exclusive forwarding, set 0x20 (FWD_CTL1) to 0x00, 0x21 (FWD_CTL2) to 0x03, and reg 0x3C[7] (EXCLUSIVE_FWD_EN) to b'1. Then the user may control which RX ports to be forwarded to each CSI port from register 0x3B (CSI_EXCLUSIVE_FWD1). Register 0x3B[7:4] controls the forwarding for CSI port 1 and 0x3B[3:0] controls the forwarding for CSI port 0. Note that by enabling exclusive forwarding, both CSI ports 0 and 1 will need to support the CSI-2 bandwidth of all cameras combined.

8.3.4.10.1.2.1 Example

CSI port 0 aggregates and outputs data from RX0, RX1, RX2, and RX3. CSI port 1 aggregates and outputs data from RX2 and RX3. If using direct forwarding by controlling register 0x20 (FWD_CTL1), this would not be achievable since each RX port can only be forwarded to one CSI port. Before enabling this feature, register 0x20 (FWD_CTL1) needs to be set to 0x00 and 0x21 (FWD_CTL2) needs to be set to 0x03. The CSI exclusive forwarding feature allows both CSI0 and CSI1 to output all four RX ports. In this case, CSI0 has masks for RX ports 0, 1, 2, and 3, whereas CSI1 has masks for only RX2 and 3. For each packet sent on CSI0, there will always be transitions into and out of LP11. When masking packets, it would leave CSI1 in LP11 for the duration of the masked packets as shown:

CSI0 : LP11 -> Rx0 -> LP11 -> Rx1 -> LP11 -> Rx2 -> LP11 -> Rx3 -> LP11

CSI1 : LP11 -----> Rx2 -> LP11 -> Rx3 -> LP11

To enable this, first set the reg 0x20 = 0x00, 0x21 = 0x03, and 0x3C[7] = b'1. For reg 0x3B, the user would set 0x3B[3:0] = b'1111 since all the RX ports are being forwarded to CSI0. For CSI1, 0x3B[7:4] would be set to b'1100 since only RX ports 3 and 2 are forwarded.

```
WriteI2C(0x32,0x03) #Read CSI Port 0, Write CSI Ports 0 and 1
WriteI2C(0x20,0xF0) #Disable RX port forwarding
WriteI2C(0x33,0x03) #Enable CSI ports 0 and 1, set continuous clock
WriteI2C(0x20,0x00) #Enable RX port forwarding (needed before enabling exclusive forwarding)
WriteI2C(0x21,0x03) #Enable round robin mode for CSI0 and CSI1
WriteI2C(0x3C,0x9F) #Enable CSI exclusive forwarding
WriteI2C(0x3B,0xCF) #CSI port 0 has data from RX0 - 3, CSI port 1 has data from RX 2 and 3 only
```

8.3.4.10.2 Synchronized Forwarding

In cases with multiple input sources, synchronized forwarding offers synchronization of all incoming data stored within the buffer. If packets arrive within a certain window, the forwarding control may be programmed to attempt to synchronize the video buffer data. In this mode, it attempts to send each channel synchronization packets in order (C0, C1, C2, C3) as well as sending packet data in the same order. In the following sections, Camera 0 (C0), Camera 1 (C1), Camera 2 (C2), and Camera 3 (C3) refers to the camera connected at FPD-Link IV RX port 0, RX port 1, RX port 2, and RX port 3 respectively.

The forwarding engine for each CSI-2 Transmitter can be configured independently and synchronize up to all video sources.

Requirements:

- Video arriving at input ports should be synchronized within approximately 1 video line period

- All enabled ports should have valid, synchronized video
- Each port must have identical video parameters, including number and size of video lines, presence of synchronization packets, etc.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempt to restart sending synchronized video at the next FrameStart indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Status is provided to indicate when the forwarding engine is synchronized. In addition, a flag is used to indicate that synchronization has been lost (status is cleared on a read).

Three options are available for Synchronized forwarding:

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

Synchronized forwarding modes are selected by setting the CSIx_SYNC_FWD controls in the FWD_CTL2 register. To enable synchronized forwarding the following order of operations is recommended:

1. Disable Best-effort forwarding by clearing the CSIx_RR_FWD bits in the FWD_CTL2 register
2. Enable forwarding per Receive port by clearing the FWD_PORTx_DIS bits in the FWD_CTL1 register
3. Enable Synchronized forwarding in the FWD_CTL2 register

8.3.4.10.2.1 Basic Synchronized Forwarding

During Basic Synchronized Forwarding each forwarded frame is an independent CSI-2 video frame including FrameStart (FS), video lines, and FrameEnd (FE) packets. Each forwarded stream may have a unique VC ID. If the forwarded streams do not have a unique VC-ID, the receiving process may use the frame order to differentiate the video stream packets.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempts to restart sending synchronized video at the next FS indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – FS1 – FS2 – FS3 – C0L1 – C1L1 – C2L1 – C3L1 – C0L2 – C1L2 – C2L2 – C3L2 – C0L3 ...

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN – C1LN – C2LN – C3LN – FE0 – FE1 – FE2 – FE3

Notes:

FSx	FrameStart for Camera X
FEx	FrameEnd for Camera X
CxLy	Line Y for Camera X video frame
CxLN	Last line for Camera X video frame

Each packet includes the virtual channel ID assigned to receive port for each camera.

8.3.4.10.2.1.1 Code Example for Basic Synchronized Forwarding

```

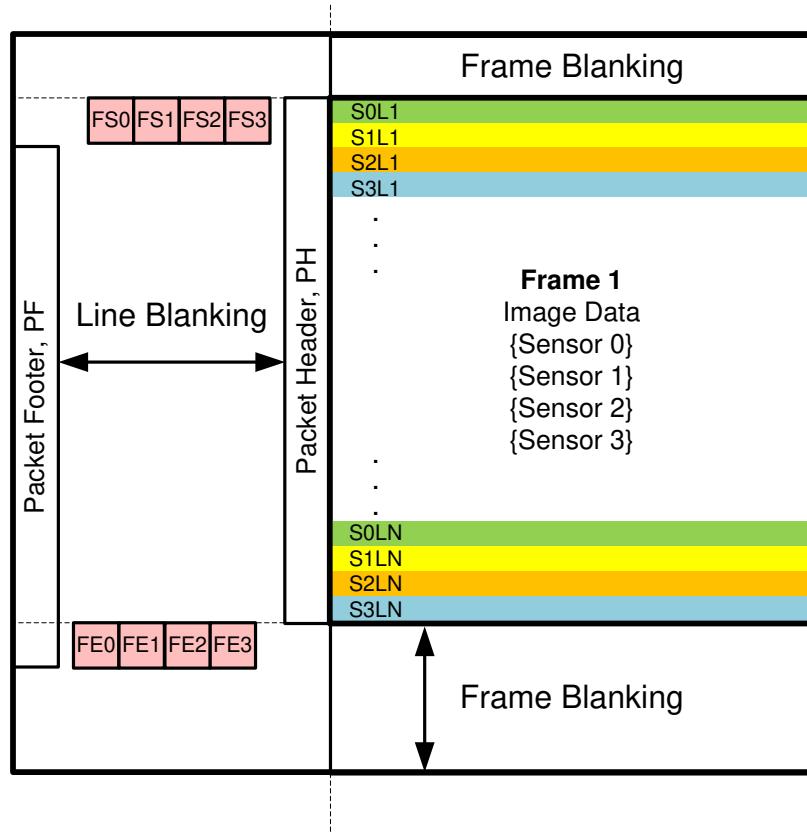
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0xA0,0x00) # RAW10_datatype_yuv422b10_VC0
# "**** RX1 VC=1 ****"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0xA0,0x01) # RAW10_datatype_yuv422b10_VC1
# "**** RX2 VC=2 ****"
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0xA0,0x02) # RAW10_datatype_yuv422b10_VC2
# "**** RX3 VC=3 ****"
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0xA0,0x03) # RAW10_datatype_yuv422b10_VC3
# "CSI_PORT_SEL"

```

```

WriteI2C(0x32,0x01) # CSI0 select
# "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# "****Basic_FWD"
WriteI2C(0x21,0x14) # Synchronized Basic_FWD
# "****FWD PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0

```

**KEY:**

PH – Packet Header

FS – Frame Start

LS – Line Start

PF – Packet Footer + Filler (if applicable)

FE – Frame End

LE – Line End



*Blanking intervals do not provide accurate synchronization timing

Figure 8-13. Basic Synchronized Format**8.3.4.10.2.2 Line-Interleave Forwarding**

In synchronized forwarding, the forwarding engine may be programmed to send only one of each synchronization packet. For example, if forwarding from all four input ports, only one FS, FE packet is sent for each video frame. The synchronization packets for the other ports are dropped. The video line packets for each video stream are sent as individual packets. This effectively merges the frames from N video sources into a single frame that has N times the number of video lines.

In this mode, all video streams must also have the same VC, although this is not checked by the forwarding engine. This is useful when connected to a controller that does not support multiple VCs. The receiving processor must process the image based on order of video line reception.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – C0L1 – C1L1 – C2L1 – C3L1 – C0L2 – C1L2 – C2L2 – C3L2 – C0L3 ...

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN – C1LN – C2LN – C3LN – FE0

Notes:

FSx	FrameStart for Camera X
FEx	FrameEnd for Camera X
CxLy	Line Y for Camera X video frame
CxLN	Last line for Camera X video frame

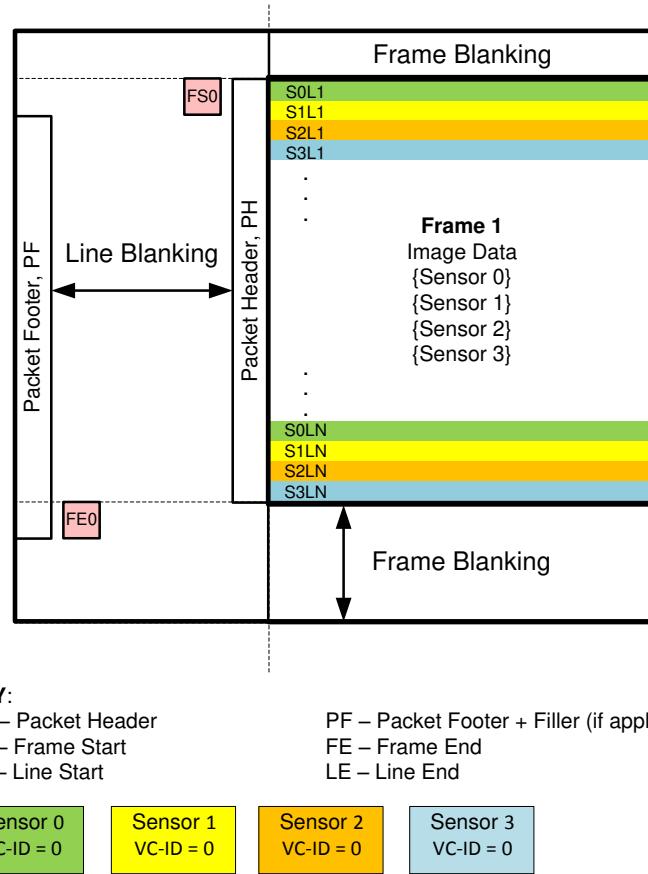
All packets would have the same VC ID.

8.3.4.10.2.2.1 Code Example for Line-Interleave Forwarding

```

WriteI2C(0x4C,0x01) # RX0
WriteI2C(0xA0,0x00) # RAW10_datatype_yuv422b10_VC0
# *** RX1 VC=1 ***
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0xA0,0x01) # RAW10_datatype_yuv422b10_VC1
# *** RX2 VC=2 ***
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0xA0,0x02) # RAW10_datatype_yuv422b10_VC2
# *** RX3 VC=3 ***
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0xA0,0x03) # RAW10_datatype_yuv422b10_VC3
# "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
# "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# *** CSI0_SYNC_FWD synchronous forwarding with line interleaving ***
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
# *** FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0

```



*Blanking intervals do not provide accurate synchronization timing

Figure 8-14. Line-Interleave Format

8.3.4.10.2.3 Line-Concatenated Forwarding

In synchronized forwarding, the forwarding engine may be programmed to merge video frames from multiple sources into a single video frame by concatenating video lines. Each of the cameras for each RX carry different data streams that get concatenated into one CSI-2 stream. For example, if forwarding from all four input ports, only one FS, an FE packet is sent for each video frame. The synchronization packets for the other ports are dropped. In addition, the video lines from each camera are combined into a single line. The controller must separate the single video line into the separate components based on position within the concatenated video line.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS0 – C0L1,C1L1,C2L1,C3L1 – C0L2,C1L2,C2L2,C3L2 – C0L3,C1L3,C2L3,C3L3 ...

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... C0LN,C1LN,C2LN,C3LN – FE0

Notes:

FSx	FrameStart for Camera X
FEx	FrameEnd for Camera X
CxLy	Line Y for Camera X video frame
CxLN	Last line for Camera X video frame

C0L1,C1L1,C2L1,C3L1 indicates concatenation of the first video line from each camera into a single video line. This packet has a modified header and footer that matches the concatenated line data.

Packets would have the same VC ID, based on the VC ID for the lowest number camera port being forwarded.

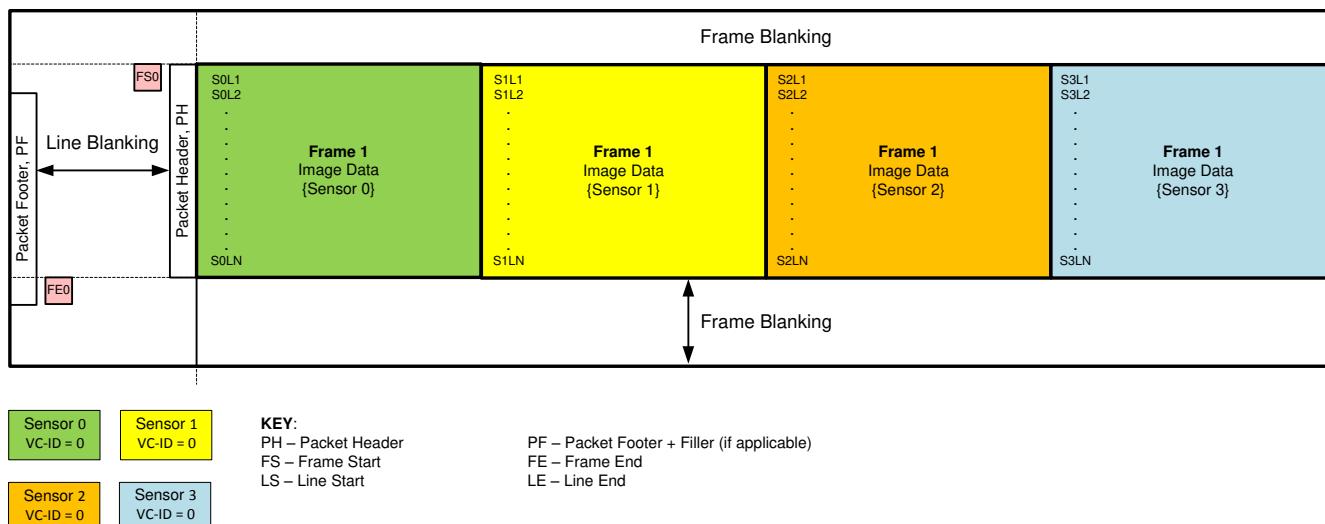
Lines are concatenated on a byte basis without padding between video line data.

8.3.4.10.2.3.1 Code Example for Line-Concatenate Forwarding

```

WriteI2C(0x4C,0x01) # RX0
WriteI2C(0xA0,0x00) # RAW10_datatype_yuv422b10_VC0
# *** RX1 VC=1 ***
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0xA0,0x01) # RAW10_datatype_yuv422b10_VC1
# *** RX2 VC=2 ***
WriteI2C(0x4C,0x24) # RX2
WriteI2C(0xA0,0x02) # RAW10_datatype_yuv422b10_VC2
# *** RX3 VC=3 ***
WriteI2C(0x4C,0x38) # RX3
WriteI2C(0xA0,0x03) # RAW10_datatype_yuv422b10_VC3
# "CSI_PORT_SEL"
WriteI2C(0x32,0x01) # CSI0 select
# "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# *** CSI0_SYNC_FWD synchronous forwarding with line concatenation ***
WriteI2C(0x21,0x3c) # synchronous forwarding with line concatenation
# ***FWD PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0

```



*Blanking intervals do not provide accurate synchronization timing

Figure 8-15. Line-Concatenated Format

8.3.4.11 CSI-2 Replication

When CSI-2 ports 0 or 1 is configured for 1- or 2-lane operation, the unused lanes can be configured to replicate within the same port. To achieve replication within the same port, set reg 0x22[4] to b'1 for CSI port 0 and reg 0x22[5] to b'1 for CSI port 1.

CSI-2 port 2 is used for CSI-2 replication. It can replicate the CSI-2 output from either CSI-2 ports 0 or 1. To enable CSI-2 port 2, set CSI_PORT2_EN field in CSI_PORT2_FIFO_CTRL (reg 0xC7) to b'1. Register 0x3C[6] (REPLICATE_CSI2) can be set to replicate from the other CSI ports. If 0x3C[6] = 0, port 2 replicates data from port 0; if 0x3C[6] = 1, port 2 replicates data from port 1. Note that when using CSI-2 replication that CSI port 2 should be enabled prior to the port it is replicating. Combining CSI-2 exclusive forwarding and CSI-2 port 2 replication can result in three copies of the FPD-Link video data being output on the three CSI-2 output ports, as seen in the example code below.

```

WriteI2C(0x32,0x03) #Read CSI Port 0, Write CSI Ports 0 and 1
WriteI2C(0x20,0xF0) #Disable RX port forwarding
WriteI2C(0xC7,0x10) #Enable CSI port 2

```

```

WriteI2C(0x33,0x03) #Enable CSI ports 0 and 1, set continuous clock
WriteI2C(0x20,0x00) #Enable RX port forwarding (needed before enabling exclusive forwarding)
WriteI2C(0x3C,0x9F) #Enable CSI exclusive forwarding, CSI port 2 replicated from CSI port 0
WriteI2C(0x3B,0xFF) #All RX ports forwarded to CSI ports 0, 1, and 2

```

8.3.4.12 CSI Transmitter Output Control

Two register controls allow control of CSI Transmitter outputs to disable the CSI Transmitter outputs. If the OUTPUT_SLEEP_STATE_SELECT (OSS_SEL) control is set to 0 in the GENERAL_CFG 0x02 register, the CSI Transmitter outputs are forced to the HS-0 state. If the OUTPUT_ENABLE (OEN) register bit is set to 0 in the GENERAL_CFG register, the CSI pins are set to the high-impedance state.

For normal operation (OSS_SEL and OEN both set to 1), the detection of activity on FPD-Link IV inputs determines the state of the CSI outputs. The FPD-Link IV inputs are considered active if the Receiver indicates valid lock to the incoming signal. For a CSI TX port, lock is considered valid if any Received port mapped to the TX port is indicating Lock.

Table 8-8. CSI Output Control Options

PDB pin	OSS_SEL	OEN	FPD-Link IV INPUT	CSI PIN STATE
0	X	X	X	Hi-Z
1	0	X	X	HS-0
1	1	0	X	Hi-Z
1	1	1	Inactive	Hi-Z
1	1	1	Active	Valid

8.3.4.13 CSI-2 Transmitter Programming Sequence

This section provides an example for enabling and disabling CSI-2 ports. Once enabled, it is typically best to leave the CSI-2 Transmitter enabled, and only change the forwarding controls if changes are required to the system. When enabling and disabling the CSI-2 Transmitter, forwarding should be disabled to ensure proper start and stop of the CSI-2 Transmitter.

When enabling and disabling the CSI-2 transmitter, use the following sequence:

To Enable:

1. Re-map Virtual Channel IDs for each RX port (if desired). Refer to [Section 8.3.4.5](#)
2. Select the desired CSI port in CSI_PORT_SEL
3. Set desired CSI output rate. Refer to [Section 8.3.4.7](#)
4. Set CSI Transmit enable, number of lanes, and Continuous clock if desired in CSI_CTL register
5. Enable CSI Periodic Calibration (if desired) in the CSI_CTL2 register
6. Enable forwarding based on desired forwarding method. Refer to [Section 8.3.4.10](#)

To Disable:

1. Select the desired CSI port in CSI_PORT_SEL
2. Disable Forwarding for assigned ports. Refer to [Section 8.3.4.10](#)
3. Disable CSI Periodic Calibration (if enabled) in the CSI_CTL2 register
4. Disable Continuous Clock operation (if enabled) in the CSI_CTL register
5. Clear CSI Transmit enable in CSI_CTL register

8.3.5 Diagnostics

The device supports various diagnostics features including error detection, built-in self test, pattern generation, timestamp, temperature and voltage sensing, line fault detection, frozen frame detection, and an eye monitor tool.

8.3.5.1 Error Detection

The deserializer includes error and status registers to detect various types of errors, including lock to the serializer, forward channel parity errors, back channel CRC errors, and CSI-2 errors. Refer to [Table 8-9](#) for a list of error registers. All the registers here are RX port specific.

Table 8-9. Error and Status Registers for Each RX Port

REGISTER	TYPES OF ERRORS	COMMENTS
RX_PORT_STS1 (0x4D)	Status	0x4D[5]: indicates CRC (BC) error detected 0x4D[2]: indicates parity (FC) error detected 0x4D[0]: indicates lock status
RX_PORT_STS2 (0x4E)	Status	0x4E[5]: indicates encoder error detected 0x4E[4]: indicates buffer error detected 0x4E[3]: indicates CSI error detected
RX_PAR_ERR_HI (0x55), RX_PAR_ERR_LO (0x56)	Parity	0x56: upper 8 bits of parity error count 0x55: lower 8 bits of parity error count
CSI_RX_STS (0x7A)	CSI-2	indicates various CSI errors
CSI_ERR_COUNTER (0x7B)	CSI-2	indicates number of CSI packets with errors

8.3.5.2 Built-In Self Test

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and the back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

When BIST is activated, the deserializer sends register writes to the serializer through the back channel. The control channel register writes configure the Serializer for BIST mode operation. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors the pattern for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

Before enabling BIST, the user must consider the CDR used for the link. If configured for FPD-Link IV CDR, the user must write the value 0x52 to offset 0xBB in indirect RX register.

BIST is configured and enabled by programming the BIST Control register (reg 0xB3). Set 0xB3 = 0x01 to enable BIST and set 0xB3 = 00 to disable BIST. After completion of BIST, the BIST Error Counter may be read to determine if errors occurred during the test. If the deserializer failed to lock to the input signal or lost lock to the input signal, the BIST Error Counter will indicate 0xFF. The maximum normal count value will be 0xFE. The SER_BIST_ACT register bit 0xD0[5] can be monitored during testing to ensure BIST is activated in the serializer.

During BIST, deserializer output activities are gated by BIST_Control[7:6] (BIST_OUT_MODE[1:0]) as follows:

00 : Outputs disabled during BIST

10 : Outputs enabled during BIST

When enabling the outputs by setting BIST_OUT_MODE = 10, the CSI-2 will be inactive by default (LP11 state). To exercise the CSI-2 interface during BIST mode, it is possible to Enable Pattern Generator to send a video data pattern on the CSI-2 outputs.

The BIST clock frequency is controlled by the BIST_CLOCK_SOURCE field in the BIST Control register. This 2-bit value will be written to the Serializer register 0x14[2:1]. A value of 00 will select an external clock. A non-zero value will enable an internal clock of the frequency defined in the Serializer register 0x14. Note that when the deserializer is paired with DS90UB933-Q1 or DS90UB913A-Q1, a setting of 11 may result in a frequency that is too slow for the deserializer to recover. The BIST_CLOCK_SOURCE field is sampled at the start of BIST. Changing this value after BIST is enabled will not change operation.

8.3.5.3 Timestamp

The timestamp feature provides relative skew between the image sensors from the different RX ports. This feature can be set to capture a timestamp for either Start-of-Frame or Start-of-Line of an imager:

- Start-of-Frame: captured when the Frame Start (FS) packet is detected

- Start-of-Line: captured at the start of reception of the Nth line of video data after the start-of-frame. If capturing Start-of-Line, the user must program a line number. The same line number is used for all four channels

Prior to running the timestamp feature, the user must first configure which RX port(s) to enable timestamp from via TS_CONTROL (reg 0x26). The TS_VALIDx bits in TS_STATUS (reg 0x29) indicates if a selected RX port has a valid timestamp. When all the enabled RX ports have a valid timestamp, the TS_READY bit will go high.

The user may access the timestamp values in TIMESTAMP_Px (reg 0x2A - 0x32). Before reading the timestamps, the user must set TS_FREEZE bit for each port in order to prevent overwrite of the timestamps. The freeze condition is released automatically once all frozen timestamps have been read. The user may also clear the freeze bits if they do not read all the timestamp values.

There are two modes for timestamp: Framesync mode and Free-run mode.

8.3.5.3.1 FrameSync Mode

In FrameSync mode, the skew detection timer will reset at the FrameSync positive or negative edge, and only the first start-of-frame or start-of-line will be captured for each RX port. If no start-of-frame or start-of-line occurs in the FrameSync period, TS_VALID will not be indicated for that channel. If multiple start-of-frame or start-of-line events occur within the FrameSync period, additional ones will be ignored.

TS_AS_AVAIL bit in TS_CONFIG (reg 0x25) determines the time in which the timestamps will be available. If this bit is set, the start-of-frame or start-of-line values will be available as soon as all timestamps for the selected RX ports are captured. If this bit isn't set, the timestamps will only be available after the skew detection timer resets.

8.3.5.3.2 Free-run Mode

In Free-run mode, the skew detection timer will not be reset on a FrameSync or other condition. As a result, timestamps are arbitrary and have meaning only relative to other timestamps.

If the frames of each port are somewhat aligned with each other, the deserializer will use TS_LINE_NUM (reg 0x27 - 0x28) to determine when to begin looking for a new set of timestamps. Once all ports have line number greater than TS_LINE_NUM, the circuit will capture all timestamps and begin looking for a new set of timestamps.

If the frames of each port are not aligned enough with each other, the circuit will latch new timestamp data at any start-of-frame/start-of-line, and TS_VALIDx flags will only indicate the most recent timestamp.

8.3.5.3.3 Timestamp Procedures

Follow the below steps to set timestamp parameters:

- Register 0x25: TS_CONFIG to set the polarity, resolution, and modes
- Register 0x26: TS_CONTROL bit 4 to freeze timestamps and clear the TS_READY flag. Bits 3-0 to enable timestamp for specific RX ports
- Registers 0x27 - 0x28: TS_LINE
 - If capturing start-of-line, these registers indicate the line number at which to capture the timestamp.
 - If capturing start-of-frame or in free-run mode, these registers determine when to begin checking for frame start
- Register 0x29: TS_STATUS indicates when timestamps are ready and which RX port(s) has valid timestamp
- Register 0x2A - 0x32: TIMESTAMP_Px indicates timestamp values

8.3.5.4 Pattern Generation

The deserializer supports internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. CSI-2 port 0 and port 1 each have their own pattern generator. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns and accessed by the Pattern Generator page 0 in the indirect register set.

Prior to enabling the Packet Generator, the following should be done:

- Select the desired CSI-2 port in CSI_PORT_SEL.

2. Disable video forwarding by setting bits [5:4] of the FWD_CTL1 register (that is, set register 0x20 to 0x30).
3. Configure CSI-2 Transmitter operating speed using the CSI_PLL_CTL register.
4. Enable the CSI-2 Transmitter using the CSI_CTL register.

8.3.5.4.1 Reference Color Bar Pattern

The Reference Color Bar Patterns are based on the pattern defined in Appendix D of the `mipi_CTS_for_D-PHY_v1-1_r03` specification. The pattern is an eight color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 Reference pattern provides eight color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted) X bytes of 0x33 (mid-frequency pattern) X bytes of 0xF0 (low-frequency pattern, inverted) X bytes of 0x7F (lone 0 pattern) X bytes of 0x55 (high-frequency pattern) X bytes of 0xCC (mid-frequency pattern, inverted) X bytes of 0x0F (low-frequency pattern) Y bytes of 0x80 (lone 1 pattern) In most cases, Y will be the same as X. For certain data types, the last color bar may need to be larger than the others to properly fill the video line dimensions.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 Data Type field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

The pattern generator relies on proper programming by software to ensure the color bar widths are set to multiples of the block (or word) size required for the specified Data Type. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The Pattern Generator is implemented in the CSI-2 Transmit clock domain, providing the pattern directly to the CSI-2 Transmitter. The circuit generates the CSI-2 formatted data.

8.3.5.4.2 Fixed Color Patterns

When programmed for Fixed Color Pattern mode, Pattern Generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the Color Bar Patterns. When sending Fixed Color Patterns, the color bar controls allow alternating between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The Fixed Color patterns assume a fixed block size for the byte pattern to be sent. The block size is programmable through the register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size should be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern would consist of 3-byte pixels and therefore require a 3-byte block size. A 2x12-bit pixel image would also require 3-byte block size, while a 3x12-bit pixel image would require nine bytes (two pixels) to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size for four pixels, so 1x10-bit and 2x10-bit could both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size would be required.

The Fixed Color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image could alternate between four different pixels by using a 12-byte block size. An alternating black and white RGB888 image could be sent with a block size of 6-bytes and setting first three bytes to 0xFF and next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte. The line period is calculated in units of 10 ns, unless the CSI-2 mode is set to 400-Mb operation in which case the unit time dependency is 20 ns.

8.3.5.4.3 Packet Generator Programming

The information in this section provides details on how to program the Pattern Generator to provide a specific color bar pattern, based on data type, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements should include the data type, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN_ACT_LPF – Number of active lines per frame
- PGEN_TOT_LPF – Number of total lines per frame
- PGEN_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes
- CSI-2 DataType field and VC-ID
- Optional: PGEN_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid
- Optional: PGEN_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid
- PGEN_LINE_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame
- PGEN_BAR_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below)

8.3.5.4.3.1 Determining Color Bar Size

The color bar pattern should be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the Mipi CSI-2 specification. For example, RGB888 requires a 3-byte block size which is the same as the pixel size. RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software should compute the required bar size in bytes based on the line size and the number of bars. For the standard eight color bar pattern, that would require the following algorithm:

- Select the desired data type, and a valid length for that data type (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the data type specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar
- Round result down to the nearest integer
- Convert blocks/bar to bytes/bar and program that value into the PGEN_BAR_SIZE register

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and divide by bytes/block.

8.3.5.4.4 Code Example for Pattern Generator

Follow the example here to configure a 1280x720 pattern with 30 fps rate and fixed color bar. The user can also use the Analog LaunchPad GUI to configure the PatGen register settings based on their desired parameters.

```
#Patgen Fixed Colorbar 1280x720p30
WriteI2C(0x33,0x01) # CSI0 enable
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24)
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x0F)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
```

```

WriteI2C(0xB2,0xE0)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x1A)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0C)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x67)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
ReadI2C(0x7A) # Clear errors that may have occurred during PATGEN init
ReadI2C(0x4E) # Clear errors that may have occurred during PATGEN init

```

8.3.5.5 Sensing

An internal 8-bit successive approximation (SAR) ADC is used to sense die temperature, internal supply voltages, and external voltages. This ADC can be set and controlled via the indirect register page SAR ADC.

8.3.5.5.1 Temperature Sensing

The deserializer uses a SAR ADC and a thermal diode to measure the die temperature. The die temperature is read and stored in the TEMP_FINAL (0x13) register on the SAR ADC Register Page. The TEMP_FINAL register has a resolution of 2°C, with an accuracy of +/- 5°C from -40°C to 150°C. The following formula converts the TEMP_FINAL decimal code to Celsius:

$$\text{Temperature } (\text{°C}) = 2 * (\text{TEMP_FINAL}) - 273 \quad (1)$$

The deserializer can also trigger an interrupt when the device temperature exceeds the maximum value of the TEMP_HIGH register or falls below the TEMP_LOW register. The TEMP_HIGH and TEMP_LOW registers can be found on the SAR ADC Register Page. To enable this interrupt's status to be displayed on the INTB pin, set b'6 of the INTERRUPT_CTL (reg 0x23) register on the Main Page to 1. By default, this interrupt will trigger when internal temperatures exceed 140°C or fall below -20°C. These thresholds can be changed by writing to the TEMP_HIGH and TEMP_LOW registers on the SAR ADC Register Page.

Example of enabling the SAR ADC and reading the TEMP_FINAL value:

```

WriteI2C(0xB0,0x28) # Select SAR ADC register page
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x00) # Enable SAR ADC sampling
WriteI2C(0xB1,0x13) # Select TEMP_FINAL register
TEMP_FINAL = ReadI2C(0xB2) # Read temperature

```

8.3.5.5.2 Supply Voltage Sensing

The deserializer can use the internal SAR ADC to monitor the voltage levels of the 1.8 V and 1.1 V supplies. The ADC can read voltages of four different pins. On the SAR ADC Register Page, IV0_FINAL and IV1_FINAL are used to read the 1.8 V supplies with a resolution of 14 mV. IV2_FINAL and IV3_FINAL are used to read the 1.1 V supplies with a resolution of 8 mV.

Table 8-10. Supply Voltage Sensing Register Map

Supply Pin	Nominal Voltage	Register Name	Register Address
VDD18_FPD	1.8 V	IV0_FINAL	0x15
VDD18_P	1.8 V	IV1_FINAL	0x16
VDD11_P	1.1 V	IV2_FINAL	0x17
VDD11_L	1.1 V	IV3_FINAL	0x18

The voltage equation to convert the decimal code for IV0_FINAL and IV1_FINAL (1.8V rail) is as follow:

$$\text{Voltage (V)} = 3 * (1/255) * 1.207 * (\text{IVx_FINAL}) \quad (2)$$

The voltage equation to convert the decimal code for IV2_FINAL and IV3_FINAL (1.1V rail) is as follow: .

$$\text{Voltage (V)} = 1.835 * (1/255) * 1.207 * (\text{IVx_FINAL}) \quad (3)$$

The deserializer can also trigger an interrupt when the supply voltage goes above or below specific voltages. To enable this interrupt's status to be displayed on the INTB pin, set b'6 of the INTERRUPT_CTL (reg 0x23) register on the Main Page to 1. The upper or lower voltage thresholds can be changed by voltage threshold registers on the SAR ADC Register Page. Refer to the following table for the default supply threshold levels and the corresponding registers. These thresholds can be changed by writing to the IVx_HIGH and IVx_LOW registers on the SAR ADC Register Page.

Table 8-11. Default Supply Voltage Threshold Levels

Supply Pin	Upper Voltage Threshold (V)	Upper Voltage Threshold Register Offset	Lower Voltage Threshold	Lower Voltage Threshold Register Offset
VDD18_FPD	1.902	0x39	1.732	0x3A
VDD18_P	1.902	0x3C	1.732	0x3D
VDD11_P	1.164	0x3F	1.060	0x40
VDD11_L	1.164	0x42	1.060	0x43

Example of enabling the SAR ADC and reading the IVx_FINAL value:

```

WriteI2C(0xB0,0x28) # Select SAR ADC register page
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x00) # Enable SAR ADC sampling
WriteI2C(0xB1,0x15) # Select IV0_FINAL register
VDD18_FPD = ReadI2C(0xB2) # Read IV0_FINAL
WriteI2C(0xB1,0x16) # Select IV1_FINAL register
VDD18_P = ReadI2C(0xB2) # Read IV1_FINAL
WriteI2C(0xB1,0x17) # Select IV2_FINAL register
VDD11_P = ReadI2C(0xB2) # Read IV2_FINAL
WriteI2C(0xB1,0x18) # Select IV3_FINAL register
VDD11_L = ReadI2C(0xB2) # Read IV3_FINAL

```

8.3.5.5.3 External Voltage Sensing

The SAR ADC can read the voltages at GPIO0 and GPIO1. These two pins can read voltages up to 1.207 V. If a higher voltage is to be read, an external voltage divider is required. The external voltage monitor registers can be found on the SAR ADC Register Page. In order to read the GPIO voltage, EXT_VOL0 (reg 0x08[0]) must be enabled for GPIO0, and EXT_VOL1 (reg 0x08[1]) must be enabled for GPIO1. The GPIO voltage can read from EXT_VOL0_FINAL (reg 0x1B) for GPIO0 and EXT_VOL1_FINAL (reg 0x1C) for GPIO1.

To calculate the voltage values from decimal code in EXT_VOLx_FINAL, use the following formula:

$$\text{Voltage (V)} = (1/255) * 1.207 * (\text{EXT_VOLx_FINAL}) \quad (4)$$

FPD-Link IV devices can also trigger an interrupt when the voltages the GPIOs go above or below specific voltages. To enable this interrupt's status to be displayed on the INTB pin set bit 6 of the INTERRUPT_CTL (reg 0x23) register on the Main Page to b'1. The registers used to set the upper and lower voltages in FPD-Link IV devices are shown in [Table 8-12](#).

Table 8-12. External Voltage Threshold Register Map

Description	Register Name	Register Address
GPIO0 Upper Threshold	EXT_VOL0_HIGH	0x4C
GPIO0 Lower Threshold	EXT_VOL0_LOW	0x4D
GPIO1 Upper Threshold	EXT_VOL1_HIGH	0x4F
GPIO1 Lower Threshold	EXT_VOL1_LOW	0x50

Example of enabling the SAR ADC and reading the EXT_IVx_FINAL value:

```
WriteI2C(0x01,0x20) # Release GPIO HOLD
WriteI2C(0xB0,0x28) # Select SAR ADC page
WriteI2C(0xB1,0x07)
WriteI2C(0xB2,0x00) # Disable IVx_FINAL
WriteI2C(0xB1,0x08)
WriteI2C(0xB2,0x03) # Enable EXT_VOLx_FINAL
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x00) # Enable SAR_ADC sampling
WriteI2C(0xB1,0x1B)
EXT_VOL0 = ReadI2C(0xB2) # Read EXT_VOL0_FINAL
WriteI2C(0xB1,0x1C)
EXT_VOL1 = ReadI2C(0xB2) # Read EXT_VOL1_FINAL
```

8.3.5.6 Line Fault Detection

Serial line-fault detection is a feature available with which the user can identify faults in the cable and the type of fault present. GPIO[2], GPIO[5], GPIO[6], GPIO[7] can be configured as sensing nodes to detect various line faults, including cable open, RX+ short to GND, RX+ short to battery, and PoC voltage out of tolerance. Line fault detection only supports operation in coax mode. The SAR ADC reads the voltage at sensing nodes and the user can determine the fault condition by mapping the voltage reading to a look-up table containing threshold bands for the different types of faults. Once the threshold bands for different fault types have been determined, the device can be programmed to trigger an interrupt upon sensing a voltage outside of the normal operation threshold.

To correctly determine the type of fault present, a margin of 50mV between fault conditions is needed. The 8-bit SAR ADC used for line-fault detection has an input voltage of 1.207V. Thus, to convert the sensed voltage to decimal code, the voltage is multiplied by 255 and divided by 1.207. A 50mV margin corresponds to a code separation of 10 decimal codes. The threshold bands that determine the type of fault may merge in the presence of errors. See [Table 8-13](#) for sources of error.

Table 8-13. Typical Error Sources

Error Source	Type of Error	Comments
External Resistive Mismatch	DC	Recommend using at least 1% matched resistor
Supply Variation	DC	Around 5% variation
Pin Leakage	DC	Dependent on PVT and pad voltage
ADC Errors (Static Non-linearity)	DC	1 LSB error. Around ± 5 mV
Ground Variation	Transient	± 50 mV
Forward Channel Data Interference	Transient	~ 0 ; Assumed a 0.1uF capacitor connected to the sense node
Back- Channel Data Interference	Transient	~ 0 ; Assumed a 0.1uF capacitor connected to the sense node
Short Resistance	DC	To incorporate imperfect shorts.
Additional Margin		Can include additional 5-10% margin in the thresholds

For more information on how to implement line fault detection, please contact TI for the application report Serial Line Fault Detection.

8.3.5.7 Frozen Frame Detection

The deserializer supports detection of frozen frame in each of the RX input ports. This is achieved by checking CRC for video lines to monitor if an imager is continuously transmitting frames with the same data. The deserializer checks for each horizontal line and compute a CRC, and aggregate all the line CRC of the same virtual channel ID to form a frame CRC. The CRC of the current frame is compared the CRC of the

previous frame to the CRC of the current frame, and if there are more than a certain number of consecutive frames with the same CRC, the frame freeze detection interrupt is flagged. Unlike competitive solutions such as watermarking, the CRC-based frozen frame detection method preserves the integrity of the video data because it does not make any modification to the pixel information from the source. Additionally, CRC-based frozen frame detection allows the serializer to detect a frozen frame directly from an imager directly, and does not require injection of metadata into the active video stream by the attached serializer. This means that the frozen frame detection feature can be implemented using off the shelf imager components with no proprietary watermarking features. The frozen frame detection feature is also backwards compatible with all FPD-Link III ADAS serializer devices, meaning that the frozen frame detection can be implemented with existing legacy camera modules that include DS90UB933-Q1, DS90UB913A-Q1, DS90UB953-Q1, DS90UB951-Q1, or DS90UB971-Q1 serializers.

Follow the below steps to enable frozen frame detection:

- FFD_CTL (reg 0x88):
 - FRAMEFREEZE_THRESHOLD ([2:0]): selects how many of the same frames are continuously received when frame freeze detection interrupt is asserted
 - FRAMEFREEZE_USE_CRC ([3]): set to b'1 to allow for checking of CRC for video lines to detect frame freeze
- FFD_ISR_HI (reg 0xFE): this register indicates if a frozen frame is detected and the virtual channel of the detected frozen frame.
- FFD_ISR_LO (reg 0xFF): this register indicates if a frozen frame is detected and the virtual channel of the detected frozen frame.
- FFD_ICR_HI (reg 0xFC): when a frozen frame is detected from a virtual channel ID set in this register, an interrupt will be alerted in IE_FRAME_FREEZE_DET (reg 0xDB[7])
- FFD_ICR_LO (reg 0xFD): when a frozen frame is detected from a virtual channel ID set in this register, an interrupt will be alerted in IE_FRAME_FREEZE_DET (reg 0xDB[7])

After a frozen frame is detected on one of the deserializer RX ports, the corresponding port must be disabled and re-enabled in order to re-start the frozen frame detection mechanism for detecting subsequent frozen frames. Disable the corresponding port using 0x0C[3:0], and then re-enable the port using 0x0C[3:0] in order to re-arm the frozen frame detection feature for that port.

8.3.5.8 Eye Monitor Tool

The integrated eye monitor analyzes the eye quality of the incoming signal for each FPD-Link port, accessible via I2C and register controlled. This tool allows the user to check and monitor the received signal by providing the eye height and eye width. The eye monitor is only supported when using the FPD-Link IV Receiver. The eye monitor (EOM) tool can be used to perform a full eye diagram capture of the equalized signal. The eye diagram is constructed within a 64×128 array, where each cell in the matrix consists of a 30-bit value representing the total number of margin errors recorded at that particular phase and voltage offset. Contact TI to obtain a full sample code for an EOM sweep.

Before performing EOM, link must be established, and the initial AEQ settings need to be configured. Follow the code below to set initial AEQ once link is obtained.

```

# SET initial EQ
WriteI2C(devAddr, 0xB0, 0x04) #read indirect analog rx0 registers
WriteI2C(devAddr, 0xB1, 0x2C)
eqSelectFPD4 = ReadI2C(devAddr, 0xB2, 1) & 0x3F # read 6-bit EQ
WriteI2C(devAddr, 0xB1, 0xE0)
WriteI2C(devAddr, 0xB2, eqSelectFPD4 | 0x40) #write EQ value

# Override Adapted Initial AEQ Value
WriteI2C(devAddr, 0xB1, 0x85)
WriteI2C(devAddr, 0xB2, 0x00) # [2]:pi_en_ov, [1]:pi_en_q_ov, [0]:pi_ov_en, [4]:odac_en_ov, [7:6]:RSVD
# do for tap1 first
WriteI2C(devAddr, 0xB1, 0x88)
tmp1 = ReadI2C(devAddr, 0xB2) & 0x0F # clear snapshot_sel bits
WriteI2C(devAddr, 0xB2, (tmp1 | 0x20)) # Snapshot selects the Tap1 Accumulator
WriteI2C(devAddr, 0xB1, 0x8A)
WriteI2C(devAddr, 0xB2, 0x80) # Capture the data
WriteI2C(devAddr, 0xB1, 0x8D)
AEQ_Portx_Tap1 = ReadI2C(devAddr, 0xB2)>>2 # [15:8]

```

```

WriteI2C(devAddr, 0xB1, 0x84)
WriteI2C(devAddr, 0xB2, AEQ_Portx_Tap1 | 0x40) # use override bit 6
# repeat for tap2
WriteI2C(devAddr, 0xB1, 0x88)
tmp1 = ReadI2C(devAddr, 0xB2) & 0x0F # clear snapshot_sel bits
WriteI2C(devAddr, 0xB2, (tmp1 | 0x30)) # Snapshot selects the Tap2 Accumulator
WriteI2C(devAddr, 0xB1, 0x8A)
WriteI2C(devAddr, 0xB2, 0x80) # Capture the data
WriteI2C(devAddr, 0xB1, 0x8D)
AEQ_Portx_Tap2 = ReadI2C(devAddr, 0xB2)>>3 # [15:8]
WriteI2C(devAddr, 0xB1, 0x9E)
WriteI2C(devAddr, 0xB2, AEQ_Portx_Tap2 | 0x10) # use override bit 4

```

The x-axis of the eye diagram controls the phase offset and can be set in indirect analog register I_PHASE_ADJ (0xC1[5:0]). The value of I_PHASE_ADJ is in two's complement format and can range from -31 to +31. The interval between each step is 4.13ps. When paired with a DS90UB971-Q1, TI recommends sweeping the x-axis from -15 to +15. When paired with a DS90UB953/935-Q1, TI recommends sweeping the x-axis from -31 to +31 to capture the full eye. In order to set the x-axis value, follow the below code. E_offset is the x-axis step value:

```

if e_offset > 63 :
    e_offset = e_offset - 64
elif e_offset < 0:
    e_offset = e_offset + 64
else:
    e_offset = e_offset
WriteI2C(devAddr, 0xB1, 0xC1)
WriteI2C(devAddr, 0xB2, e_offset)

```

The y-axis controls the amplitude offset and can be set in indirect registers EQ_CTRL_SEL_17 and EQ_CTRL_SEL_18 (reg 0x89 and 0x8A). The y-axis value can range from 0 to 127, with 63 being the highest amplitude and 64 being the lowest amplitude. 0 is the zero crossing at 0V and can go up to 63, and 127 is one step below 0 and can go down to 64. The interval between each step is 6.25mV. TI recommends sweeping the y-axis from [0:31] and [96:127] to capture the full signal amplitude. In order to set the y-axis value, follow the below code. Ref01 in the code is the y-axis step value:

```

if ref01 > 127:
    ref01 = ref01 - 128
elif ref01 < 0:
    ref01 = ref01 + 128
else:
    ref01 = ref01

WriteI2C(devAddr, 0xB1, 0x89)
WriteI2C(devAddr, 0xB2, ((~ref01+1) & 0x7F) | 0x80)
WriteI2C(devAddr, 0xB1, 0x8A)
WriteI2C(devAddr, 0xB2, ref01)

```

Once the desired x-axis and y-axis values are set, the user must first start the margin error counter by setting analog indirect 0x8B[3] = b'1. Then the user can read the value in analog indirect registers 0x90[5:0], 0x91[7:0], 0x92[7:0], 0x93[7:0]. The values indicated in these regiseters can be used to compute a 30-bit margin error. The smaller the value, the fewer margin errors the cell has, with 0 being the smallest value. The user can convert the values read in the registers to the margin error by implementing the following code:

```

WriteI2C(devAddr, 0xB1, 0x8B)
tmp1 = ReadI2C(devAddr, 0xB2)
WriteI2C(devAddr, 0xB2, tmp1 | 0x08) # Starts XOR Counter
# Read XOR Counter 7:0
WriteI2C(devAddr, 0xB1, 0x93)
Value_7_0 = ReadI2C(devAddr, 0xB2)

# Read XOR Counter 15:8
WriteI2C(devAddr, 0xB1, 0x92)
Value_15_8 = (ReadI2C(devAddr, 0xB2)) << 8

# Read XOR Counter 23:16
WriteI2C(devAddr, 0xB1, 0x91)
Value_23_16 = (ReadI2C(devAddr, 0xB2)) << 16

```



```

# Read XOR Counter 29:24
WriteI2C(devAddr, 0xB1, 0x90)
Value_29_24 = (ReadI2C(devAddr, 0xB2) & 0x3F) << 24

Value_Port = Value_29_24 + Value_23_16 + Value_15_8 + Value_7_0

WriteI2C(devAddr, 0xB1, 0x8B)
WriteI2C(devAddr, 0xB2, tmp1 & 0xF7) # Stop XOR Counter

```

When a full eye is captured, the user can get an image as shown, the green areas are the areas where there's no error margin (open eye).

8.4 Device Functional Mode

The deserializer receives data from sensors or imagers on its FPD-Link input ports and forwards the data to its CSI-2 transmit ports. The MODE pin strapping determines the default device functional mode, which sets the following:

- CDR (FPD-Link IV or FPD-Link III)
- Clock Mode (synchronous or non-synchronous)
- RX Mode (CSI-2 or DVP formatted data)
- Back Channel (enabled or not enabled)
- CSI-2 Transmitter Speed (2.5Gbps or 800Mbps)

8.4.1 Compatibility

The device is a versatile deserializer that selects FPD-Link data streams from camera sources and transmits the received data over a MIPI CSI-2 interface. This deserializer is compatible with the DS90UB971-Q1, DS90UB981-Q1, and the serializers in the FPD-Link III ADAS family. [Table 8-14](#) shows all the compatible serializers. This deserializer includes both FPD-Link IV and FPD-Link III CDRs in each of its RX ports. The user can configure each RX port independently to use the FPD-Link IV CDR or the FPD-Link III CDR depending on the desired serializer and operating mode. The default mode is determined by the mode strapping. The user can select the CDR used in each RX port in CHANNEL_MODE (reg 0xE4). Consult the serializer datasheet for each part for CSI-2 input bandwidth capability based on the mode and the forward channel frequency selected.

Table 8-14. Serializer Compatibility

Serializer	DS90UB971-Q1	DS90UB981-Q1	DS90UB953-Q1	DS90UB953A-Q1	DS90UB951-Q1	DS90UB935-Q1	DS90UB933-Q1	DS90UB913A-Q1
Compatibility	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Follow the steps below setup a link between the DS90UB9702-Q1 and compatible serializer.

1. Select RX port to configure (Main: 0xB0, Main: 0x4C)
2. Run the given script below that corresponds to the mode being used
3. Enable the RX ports being used (Main: 0x0C)
4. Issue digital reset (Main: 0x01) once all ports are configured
5. Delay for 20ms

8.4.1.1 Compatibility with DS90UB971-Q1

The device can be paired with the DS90UB971-Q1 serializer using the FPD-Link IV CDR. In synchronous mode, the forward channel runs at 7.55Gbps, and the back channel runs at 47.1875Mbps. Synchronous mode supports CMLOUT to drive another deserializer. Follow the example below to configure FPD-Link IV CDR in synchronous mode. (Note the steps below configure RX0 only, but the 0x4C setting can be adjusted to target a different RX port or multiple).

```

WriteI2C(0x4C,0x01) # Select RX0 Registers
WriteI2C(0xB0,0x04) # Select RX0 Registers
WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
WriteI2C(0x0C,0x01) # Enable RX0
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)

```

```

WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

```

In non-synchronous mode, the forward channel runs at 7.55Gbps, and the back channel runs at 9.4375Mbps. The reference clocks provided to the deserializer and DS90UB971-Q1 need to be within ± 100 ppm of each other. The example code can be used to configure for FPD-Link IV CDR in non-synchronous mode. (Note the steps below configure RX0 only, but the 0x4C setting can be adjusted to target a different RX port or multiple).

```

WriteI2C(0x4C,0x01) # Select RX0 Registers
WriteI2C(0xB0,0x04) # Select RX0 Registers
WriteI2C(0xE4,0x01)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x42) & 0xFA
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
WriteI2C(0x0C,0x01)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

```

8.4.1.2 Compatibility with DS90UB981-Q1

The device can be paired with the DS90UB981-Q1 serializer using the FPD-Link IV CDR in non-synchronous mode. The back channel rate will be 9.4375Mbps and the forward channel rate will be 7.55Gbps. Follow the example below to configure FPD-Link IV CDR to be paired with a DS90UB981-Q1 serializer. (Note the steps below configure RX0 only, but the 0x4C setting can be adjusted to target a different RX port or multiple).

```

WriteI2C(0x4C,0x01) # Select RX0 Registers
WriteI2C(0xB0,0x04) # Select RX0 Registers
WriteI2C(0xE4,0x01)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x42) & 0xFA

```

```

WriteI2C(0x58, reg_0x58)
WriteI2C(0xB1, 0x04)
WriteI2C(0xB2, 0x00)
WriteI2C(0xB1, 0x1B)
WriteI2C(0xB2, 0x00)
WriteI2C(0xB1, 0x21)
WriteI2C(0xB2, 0x2F)
WriteI2C(0xB1, 0x25)
WriteI2C(0xB2, 0xC1)
WriteI2C(0x3C, 0x0F)
WriteI2C(0x0C, 0x01)
WriteI2C(0xB2, 0x41)
WriteI2C(0x3C, 0x1F)
WriteI2C(0xB1, 0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1, 0x27)
WriteI2C(0xB2, read_aeq_init)
WriteI2C(0xB1, 0x28)
WriteI2C(0xB2, read_aeq_init+1)
WriteI2C(0xB1, 0x2B)
WriteI2C(0xB2, 0x00)
WriteI2C(0xB1, 0x9E)
WriteI2C(0xB2, 0x00)
WriteI2C(0xB1, 0x90)
WriteI2C(0xB2, 0x40)
WriteI2C(0xB1, 0x2E)
WriteI2C(0xB2, 0x40)
WriteI2C(0xB1, 0xF0)
WriteI2C(0xB2, 0x00)
WriteI2C(0xB1, 0x71)
WriteI2C(0xB2, 0x00)

```

Refer to the DS90UB981-Q1 datasheet for more information on how to configure the DS90UB981-Q1 for ADAS mode.

8.4.1.3 Compatibility with DS90UB953-Q1, DS90UB953A-Q1 and DS90UB935-Q1

When paired with a DS90UB953-Q1, DS90UB953A-Q1 or DS90UB935-Q1, the deserializer can use either the FPD-Link IV or FPD-Link III CDR. The table below summarizes the major differences between the two CDRs. The user should select the type of CDR they wish to use based on their application.

Table 8-15. Pairing With DS90UB953/953A/935-Q1

Pairing With DS90UB953/953A/935-Q1		
	FPD-Link IV CDR	FPD-Link III CDR
Mode	Synchronous mode only	Synchronous and non-synchronous mode
Forward Channel Rate	3.775Gbps	3.775Gbps or 4.16Gbps configurable
Back Channel Rate	47.1875Mbps in sync mode	47.1875-52Mbps in sync mode (see below for configuration options)
CSI Bandwidth	Up to 755Mbps/lane	755Mbps-832Mbps based on configured back channel rate in synchronous mode. Up to 832Mbps in non-synchronous mode based on serializer forward channel rate (see serializer datasheet)
CMLOUT	Supports CMLOUT loop-thru	Doesn't Support CMLOUT loop-thru

The following code can be used to configure for FPD-Link IV CDR to be paired with the DS90UB953-Q1, DS90UB953A-Q1, or DS90UB935-Q1 in synchronous mode with a 47.1875Mbps back channel and a 3.775 Gbps forward channel. The DS90UB9702-Q1 can only be programmed for half-rate mode (Note the steps below configure RX0 only, but the 0x4C and 0xB0 settings can be adjusted to target a different RX port or multiple).

```

WriteI2C(0x4C, 0x01) # Select RX0 Registers
WriteI2C(0xB0, 0x04) # Select RX0 Registers
WriteI2C(0xE4, 0x00)
WriteI2C(0xB1, 0x01)
WriteI2C(0xB2, 0x80)

```

```

WriteI2C(0xB1,0x88)
WriteI2C(0xB2,0x01)
WriteI2C(0xC2,0x01) # Set desired ports into half rate mode
WriteI2C(0x0C,0x01)
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

```

The following code shows an example for setting up backwards compatibility with the DS90UB953-Q1, DS90UB953A-Q1, or DS90UB935-Q1 in synchronous mode using FPD-Link III CDR and 47.1875Mbps back channel which sets a 3.775Gbps forward channel rate from the serializer. (Note the steps below configure RX0 only, but the 0x4C and 0xB0 settings can be adjusted to target a different RX port or multiple.)

```

WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xE4,0x02)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0xA8)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x1B)
reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)
WriteI2C(0x0C,0x01)

```

When using the FPD-Link III CDR it is also possible to set the back channel rate to 50Mbps or 52Mbps which will set a forward channel rate of 4Gbps or 4.16Gbps respectively by placing additional configurations prior to issuing the digital reset in the script above. (Note 52Mbps back channel is not compatible with DS90UB971-Q1 and is common to all ports. If DS90UB971-Q1 is being used then the 47.1875Mbps back channel should be used.)

```

#Set back channel to 52Mbps
WriteI2C(0xB0,0x16)
WriteI2C(0xB1,0x8A)
WriteI2C(0xB2,0x10)
WriteI2C(0xB1,0x87)
WriteI2C(0xB2,0xA6)
WriteI2C(0xB1,0x83)
WriteI2C(0xB2,0x66)
WriteI2C(0xB1,0x84)
WriteI2C(0xB2,0x66)
WriteI2C(0xB1,0x85)
WriteI2C(0xB2,0x66)
OR
#Set back channel to 50Mbps
WriteI2C(0xB0,0x16)
WriteI2C(0xB1,0x8A)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x87)
WriteI2C(0xB2,0xA0)
WriteI2C(0xB1,0x83)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x84)

```

```
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x85)
WriteI2C(0xB2,0x00)
```

If a back channel rate has been adjusted to 50Mbps or 52Mbps and the user wishes to switch back to using the FPD-Link IV CDR, then the following code can be used to reset the back channel rate to 47.1875Mbps which is required to the FPD-Link IV CDR mode:

```
#Set back channel to 47.1875Mbps
WriteI2C(0xB0,0x16)
WriteI2C(0xB1,0x8A)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x87)
WriteI2C(0xB2,0x97)
WriteI2C(0xB1,0x83)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x84)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x85)
WriteI2C(0xB2,0x00)
```

If running in non-synchronous mode, the deserializer will also need to be configured to use the FPD-Link III CDR. In this mode, the DS90UB953-Q1, DS90UB953A-Q1, and DS90UB935-Q1 support operation with an external clock at the serializer or the AON clock inside the serializer. The forward channel rate runs at up to 4.16Gbps depending on serializer clock input, and the back channel runs at 9.4375Mbps. The following code configures the link to pair with the DS90UB953-Q1, DS90UB953A-Q1, and DS90UB935-Q1 in non-synchronous mode. (Note the steps below configure RX0 only, but the 0x4C and 0xB0 settings can be adjusted to target a different RX port or multiple).

```
WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xE4,0x02)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x42) & 0xFA
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0xA8)
WriteI2C(0xB2,0x80)

WriteI2C(0xB1,0x1B)
reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)

WriteI2C(0x0C,0x01) # Enable RX port 0
```

8.4.1.4 Compatibility with DS90UB951-Q1

The deserializer can be paired with DS90UB951-Q1 running at 4.85Gbps forward channel (up to 970Mbps/lane CSI-2 bandwidth) and 9.4375Mbps back channel using the FPD-Link III CDR. Pairing with DS90UB951-Q1 only supports non-synchronous mode. Follow the code below to configure the device for FPD-Link III non-synchronous mode. (Note the steps below configure RX0 only, but the 0x4C and 0xB0 settings can be adjusted to target a different RX port or multiple).

```
WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xE4,0x02)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x42) & 0xFA
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x01)
WriteI2C(0xB2,0xC0)
WriteI2C(0xB1,0xA2)
WriteI2C(0xB2,0x17)
WriteI2C(0xB1,0xA8)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x1B)
```

```

reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)
WriteI2C(0x0C,0x01)

```

8.4.1.5 Compatibility with DS90UB933-Q1 and DS90UB913A-Q1

The deserializer can be paired with DS90UB933-Q1 and DS90UB913A-Q1 using the FPD-Link III CDR in DVP mode. The user needs to select the desired RX mode (RAW10, RAW12 LF, and RAW12 HF) in CHANNEL_MODE (reg 0xE4). The forward channel frames are 28-bit long. In this mode, the forward channel operates at between 0.7Gbps and 1.866Gbps and back channel runs at 2.3594Mbps. The code below shows an example for how to configure for DVP operation with the DS90UB933-Q1 and DS90UB913A-Q1. (Note the steps below configure RX0 only, but the 0x4C and 0xB0 settings can be adjusted to target a different RX port or multiple).

```

WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xE4,0x04)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x40) & 0xF8
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0xA8)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x1B)
reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)
WriteI2C(0x0C,0x01)

```

8.4.1.6 Example 1

The script in this section is an example of linking a DS90UB971-Q1 serializer to each of the four RX ports in FPD-Link IV Sync mode.

```

WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x01
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)

WriteI2C( 0x4C, 0x12) # Select RX port 1
WriteI2C( 0xB0, 0x08) # Select RX port 1
WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)

```

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```

WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x02
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)

WriteI2C( 0x4C, 0x24) # Select RX port 2
WriteI2C( 0xB0, 0x0C) # Select RX port 2
WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x04
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)

WriteI2C( 0x4C, 0x38) # Select RX port 3
WriteI2C( 0xB0, 0x10) # Select RX port 3
WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x08
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)

WriteI2C(0x4C,0x01) # Select RX port 0
WriteI2C(0xB0,0x04) # Select RX port 0
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x4C,0x12) # Select RX port 1
WriteI2C(0xB0,0x08) # Select RX port 1

```

```

WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x4C,0x24) # Select RX port 2
WriteI2C(0xB0,0x0C) # Select RX port 2
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x4C,0x38) # Select RX port 3
WriteI2C(0xB0,0x10) # Select RX port 3
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x01,0x01) # Digital Soft Reset

```

8.4.1.7 Example 2

The script in this section is an example of linking the following serializers:

- RX0: DS90UB971-Q1 Sync Mode
- RX1: DS90UB953-Q1 FPD4CDR Sync Mode
- RX2: DS90UB953-Q1 FPD3CDR Sync Mode
- RX3: DS90UB933-Q1 DVP Mode

```

WriteI2C(0x4C, 0x01) # Select RX0 Registers
WriteI2C(0xB0, 0x04) # Select RX0 Registers

```

```

WriteI2C(0xE4,0x00)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0x04)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x1B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x21)
WriteI2C(0xB2,0x2F)
WriteI2C(0xB1,0x25)
WriteI2C(0xB2,0xC1)
WriteI2C(0x3C,0x0F)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x01
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB2,0x41)
WriteI2C(0x3C,0x1F)
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C( 0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x4C,0x12) # Select RX port 1
WriteI2C(0xB0,0x08) # Select RX port 1
WriteI2C(0xE4,0x00)
WriteI2C(0xB1,0x01)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x88)
WriteI2C(0xB2,0x01)
WriteI2C(0xC2,0x04)
reg_0x0C = board.ReadI2C(devAddr,0x0C)
reg_0x0C = reg_0x0C | 0x02
board.WriteI2C(devAddr, 0x0C, reg_0x0C)
WriteI2C(0xB1,0x2C)
read_aeq_init = ReadI2C(0xB2)
WriteI2C(0xB1,0x27)
WriteI2C(0xB2,read_aeq_init)
WriteI2C(0xB1,0x28)
WriteI2C(0xB2,read_aeq_init+1)
WriteI2C(0xB1,0x2B)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x9E)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x90)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0x2E)
WriteI2C(0xB2,0x40)
WriteI2C(0xB1,0xF0)
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x71)
WriteI2C(0xB2,0x00)

WriteI2C(0x4C,0x24) # Select RX port 2
WriteI2C(0xB0,0x0C) # Select RX port 2
WriteI2C(0xE4,0x02)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = reg_0x58 | 0x46
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0xA8)

```

```

WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x1B)
reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)

WriteI2C(0x4C,0x38)  # Select RX port 3
WriteI2C(0xB0,0x10)  # Select RX port 3
WriteI2C(0xE4,0x04)
reg_0x58 = ReadI2C(0x58)
reg_0x58 = (reg_0x58 | 0x40) & 0xF8
WriteI2C(0x58,reg_0x58)
WriteI2C(0xB1,0xA8)
WriteI2C(0xB2,0x80)
WriteI2C(0xB1,0x1B)
reg_0x1B = ReadI2C(0xB2)
reg_0x1B = reg_0x1B | 0x08
WriteI2C(0xB2,reg_0x1B)
WriteI2C(0xB1,0x0D)
WriteI2C(0xB2,0x7F)

WriteI2C(0x0C,0x0F) # Enable all RX ports
WriteI2C(0x01,0x01) # Perform digital soft reset

```

8.4.2 Clock Mode

The deserializer consists of two clock modes: synchronous and non-synchronous.

In synchronous mode, the deserializer provides a 47.1875Mbps back channel to the serializer. The serializer multiplies the back channel frequency up to the appropriate frequencies for the forward channel. The serializer does not need a separate reference clock input. This mode is supported when pairing with a DS90UB971-Q1, DS90UB953(A)-Q1, or DS90UB935-Q1.

In non-synchronous mode, the paired serializer does not use the back channel to derive the forward channel; instead, the serializer uses a local clock source or its internal clock to generate the forward channel. There are two different sub-modes in non-synchronous mode:

- non-DVP: operates at between 7.55Gbps and ~2Gbps forward channel rate and 9.4375Mbps back channel rate. This mode is used when paired with a serializer with CSI-2 interface, which includes DS90UB971-Q1, DS90UB951-Q1, DS90UB953(A)-Q1, and DS90UB935-Q1.
- DVP: operates at between 0.7Gbps and 1.866Gbps forward channel rate and 2.3594Mbps back channel rate. This mode is used when paired with a serializer with parallel interface, which includes DS90UB933-Q1 and DS90UB913A-Q1.

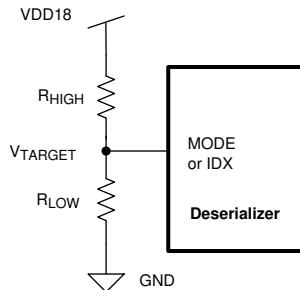
8.4.3 RX Mode

The deserializer supports two RX modes: CSI-2 and DVP. CSI-2 mode refers to pairing with a serializer with CSI-2 input, and DVP refers to pairing with a serializer with parallel input. In CSI-2 mode, the forward channel frame is 40-bit long; whereas in DVP mode, the forward channel frame is 28-bit long. DVP mode consists of the following sub-modes:

- RAW10: 10 bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Line rate = $(PCLK / 2) \times 28$. For example, PCLK = 100 MHz, line rate = $(100 \text{ MHz} / 2) \times 28 = 1.40 \text{ Gbps}$. Note: HS/HV is restricted to no more than one transition per 10 PCLK cycles. The back channel rate must be set to 2.3594 Mbps in this mode
- RAW12 LF: 12 bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit, low-frequency mode. Line rate = $PCLK \times 28$. For example, PCLK = 50 MHz, line rate = $50 \text{ MHz} \times 28 = 1.40 \text{ Gbps}$. Note: No HS/V/S restrictions (raw). The back channel rate must be set to 2.3594 Mbps in this mode.
- RAW12 HF: 12 bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 100 MHz (75 MHz for DS90UB913AQ1) in the 12-bit, high-frequency mode. Line rate = $PCLK \times (2/3) \times 28$. For example, PCLK = 100 MHz, line rate = $(100 \text{ MHz}) \times (2/3) \times 28 = 1.87 \text{ Gbps}$. Note: No HS/V/S restrictions (raw). NOTE: The back channel rate must be set to 2.3594 Mbps in this mode.

8.4.4 MODE Pin

A pull-up resistor and a pull-down resistor of suggested values should be used to set the voltage ratio of the MODE input (V_{MODE}) and V_{DD18} to set to different modes. All the parameters set by the MODE pin can be overwritten via registers.

**Figure 8-16. MODE Pin Connection Diagram****Table 8-16. Mode Configuration**

NO.	V _{MODE} VOLTAGE RANGE			SUGGESTED STRAP RESISTORS (1% TOL)		MODE NAME	BACK CHANNEL	CSI-2 TRANSMITTER RATE (Mbps)	RX MODE
	V _{MIN}	V _{TYP}	V _{MAX}	R _{HIGH} (kΩ)	R _{LOW} (kΩ)				
0	0	0	0.131 × VDD18	OPEN	10.0	FPD-Link IV Synchronous	On	2500	CSI-2
1	0.179 × VDD18	0.213 × VDD18	0.247 × VDD18	88.7	23.2	FPD-Link IV Non-Synchronous	On	2500	CSI-2
2	0.296 × VDD18	0.330 × VDD18	0.362 × VDD18	75.0	35.7	FPD-Link III Sync/Non-Synchronous	On	800	CSI-2
3	0.412 × VDD18	0.443 × VDD18	0.474 × VDD18	71.5	56.2	FPD-Link III Non-Synchronous DVP	On	800	RAW12 HF
4	0.525 × VDD18	0.559 × VDD18	0.592 × VDD18	78.7	97.6	FPD-Link IV Synchronous	Off	2500	CSI-2
5	0.642 × VDD18	0.673 × VDD18	0.704 × VDD18	39.2	78.7	FPD-Link IV Non-Synchronous	Off	2500	CSI-2
6	0.761 × VDD18	0.792 × VDD18	0.823 × VDD18	25.5	95.3	FPD-Link III Sync/Non-Synchronous	Off	800	CSI-2
7	0.876 × VDD18	VDD18	VDD18	10.0	OPEN	FPD-Link III Non-Synchronous DVP	Off	800	RAW12 HF

8.5 I²C Programming

8.5.1 Serial Control Bus

The deserializer implements two I²C compatible serial control buses. Both I²C ports support local device configuration and incorporate a bi-directional control channel (BCC) that allows communication with a remote serializers as well as remote I²C slave devices.

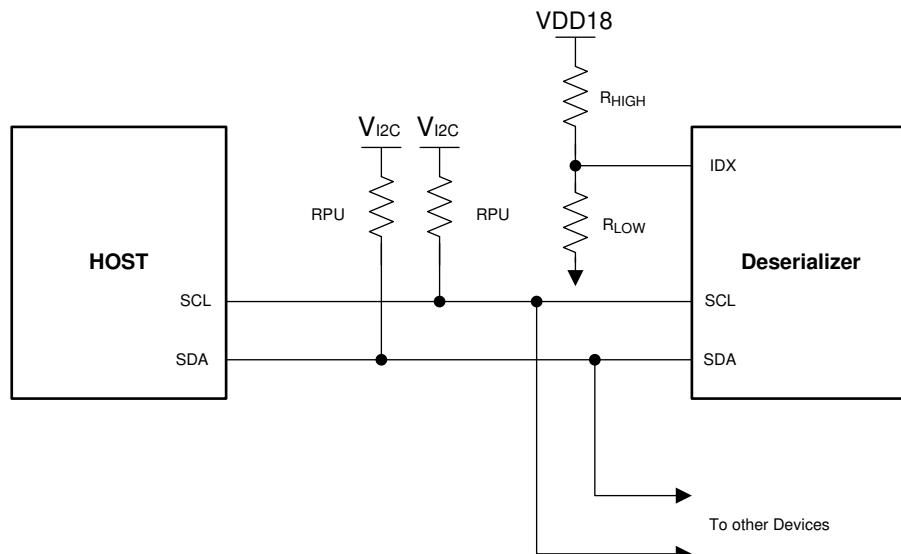


Figure 8-17. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to VDDIO. For most applications, TI recommends a 2.2 kΩ or 4.7 kΩ pullup resistor to VDDIO. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See [Figure 8-18](#).

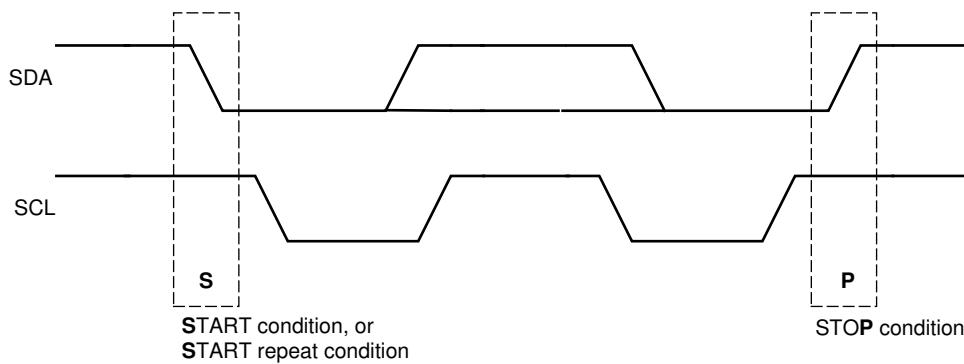


Figure 8-18. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match a device's slave address, it not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data

byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in [Figure 8-19](#) and a WRITE is shown in [Figure 8-20](#).

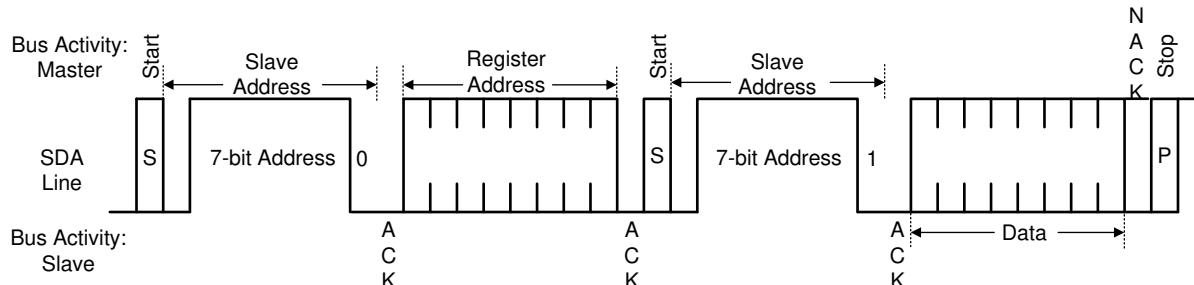


Figure 8-19. Serial Control Bus — READ

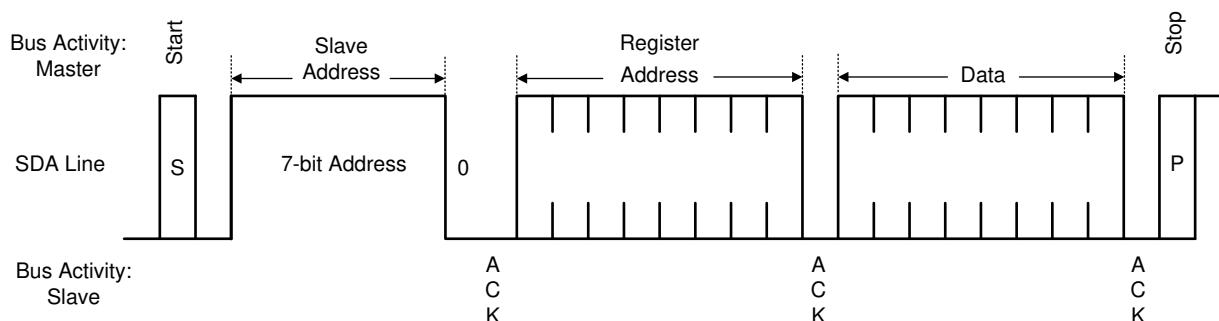


Figure 8-20. Serial Control Bus — WRITE

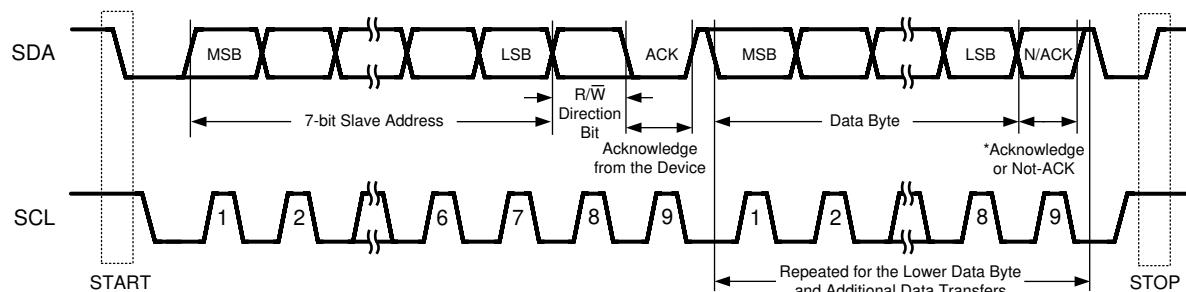


Figure 8-21. Basic Operation

The I2C Master located at the Deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to [I2C Communication Over FPD-Link with Bidirectional Control Channel](#) and [I2C over DS90UB913/4 FPD-Link with Bidirectional Control Channel](#).

8.5.2 IDX Pin

The device address is set via a resistor divider connected to the IDX pin. The IDX pin configures the control interface to one of 8 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDX input pin (V_{IDX}) and VDD18, each ratio corresponding to a specific device address, see [Figure 8-22](#).

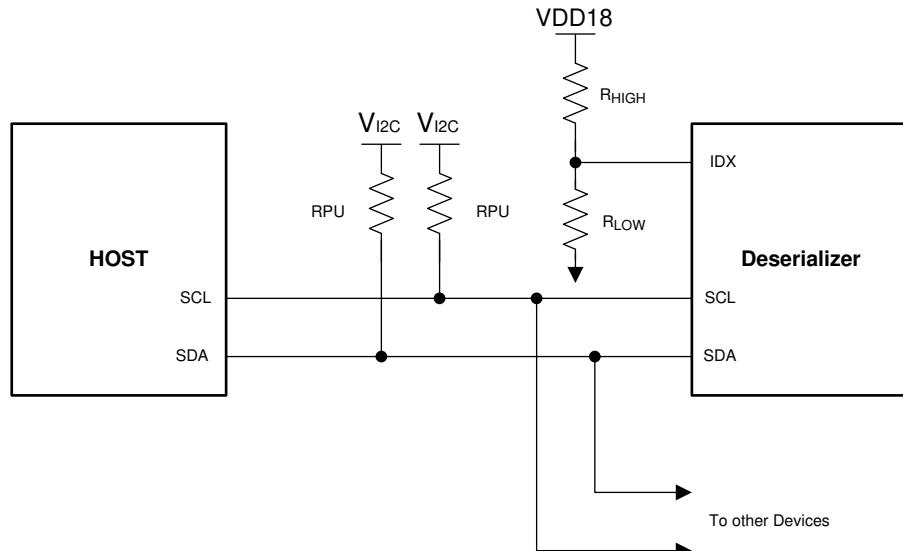


Figure 8-22. Serial Control Bus Connection

Table 8-17. IDX Configuration

NO .	V _{IDX} VOLTAGE RANGE			V _{IDX} TARGET VOLTAGE VDD18 = 1.80 V	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I ₂ C ADDRESS	
	V _{MIN}	V _{TYP}	V _{MAX}		R _{HIGH} (kΩ)	R _{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × V _(VDD18)	0	OPEN	10.0	0x30	0x60
1	0.179 × V _(VDD18)	0.213 × V _(VDD18)	0.247 × V _(VDD18)	0.374	88.7	23.2	0x32	0x64
2	0.296 × V _(VDD18)	0.330 × V _(VDD18)	0.362 × V _(VDD18)	0.582	75.0	35.7	0x34	0x68
3	0.412 × V _(VDD18)	0.443 × V _(VDD18)	0.474 × V _(VDD18)	0.792	71.5	56.2	0x36	0x6C
4	0.525 × V _(VDD18)	0.559 × V _(VDD18)	0.592 × V _(VDD18)	0.995	78.7	97.6	0x38	0x70
5	0.642 × V _(VDD18)	0.673 × V _(VDD18)	0.704 × V _(VDD18)	1.202	39.2	78.7	0x3A	0x74
6	0.761 × V _(VDD18)	0.792 × V _(VDD18)	0.823 × V _(VDD18)	1.420	25.5	95.3	0x3C	0x78
7	0.876 × V _(VDD18)	V _(VDD18)	V _(VDD18)	1.8	10.0	OPEN	0x3D	0x7A

8.6 Register Maps

The deserializer implements the following register blocks, accessible via I2C as well as the bi-directional control channel:

- Main Registers
- PATGEN and CSI-2 Registers
- FPD-Link IV RX Port Analog Registers (separate register block for each of the RX ports)
- PLL Control Registers
- CSI-2 Analog Registers (separate register block for each of the CSI-2 ports)
- DIE ID Registers
- SAR ADC Registers

Table 8-18. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP			
0x00-0x31	Digital Shared Registers	Shared			
0x33-0x3A	Digital CSI-2 Registers (paged, broadcast write allowed)	CSI-2 TX Port 0 R: 0x32[4]=0 W: 0x32[0]=1	CSI-2 TX Port 1 R: 0x32[4]=1 W: 0x32[1]=1		
0x3B-0x3F	Digital Shared Registers	Reserved			
0x40-0x45	Sensor Registers	Shared			
0x46-0x8F	Digital RX Port Registers (paged, broadcast write allowed)	FPD4 RX Port 0 R: 0x4C[5:4]=00 W: 0x4C[0]=1	FPD4 RX Port 1 R: 0x4C[5:4]=01 W: 0x4C[1]=1	FPD4 RX Port 2 R: 0x4C[5:4]=10 W: 0x4C[2]=1	FPD4 RX Port 3 R: 0x4C[5:4]=11 W: 0x4C[3]=1
0x90-0x9F	Digital CSI-2 Debug Registers	Shared			
0xA0-0xA7	VC-ID Mapping	FPD4 RX Port 0	FPD4 RX Port 1	FPD4 RX Port 2	FPD4 RX Port 3
0xA8-0xAF	eFuse Program Registers	Shared			
0xB0-0xB2	Indirect Access Registers	Shared			
0xB3-0xBF	Digital Share Debug Registers	Shared			
0xC0-0xCF	Digital Shared Registers	Shared			
0xD0-0xDF	Digital RX Port Debug/Interrupt Registers	FPD4 RX Port 0	FPD4 RX Port 1	FPD4 RX Port 2	FPD4 RX Port 3
0xE0-0xE6	Reserved	Reserved			
0xE7-0xEF	Digital Shared Registers	Shared			
0xF0-0xF7	FPD4 RX ID	Shared			
0xF8-0xFF	Port I2C Addressing	Shared			

LEGEND:

- RW = Read Write
- RW/SC = RW/SC = Read Write access/Self Clearing bit
- R = Read Only, Permanent value
- R/COR = Read Only, Clear On Read

8.6.1 Main Registers

MAIN Registers lists the memory-mapped registers for the Main registers. All register offset addresses not listed in **MAIN Registers** should be considered as reserved locations and the register contents should not be modified.

Table 8-19. MAIN Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG	GENERAL_CFG	Go
0x3	REV_MASK_ID	REV_MASK_ID	Go
0x4	DEVICE_STS	DEVICE_STS	Go

Table 8-19. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x5	PAR_ERR_THOLD1	PAR_ERR_THOLD1	Go
0x6	PAR_ERR_THOLD0	PAR_ERR_THOLD0	Go
0x7	BCC_Watchdog_Control	BCC_Watchdog_Control	Go
0x8	I2C_Control_1	I2C_Control_1	Go
0x9	I2C_Control_2	I2C_Control_2	Go
0xA	SCL_High_Time	SCL_High_Time	Go
0xB	SCL_Low_Time	SCL_Low_Time	Go
0xC	RX_PORT_CTL	RX_PORT_CTL	Go
0xD	IO_CTL	IO_CTL	Go
0xE	GPIO_PIN_STS	GPIO_PIN_STS	Go
0xF	GPIO_INPUT_CTL	GPIO_INPUT_CTL	Go
0x10	GPIO0_PIN_CTL	GPIO0_PIN_CTL	Go
0x11	GPIO1_PIN_CTL	GPIO1_PIN_CTL	Go
0x12	GPIO2_PIN_CTL	GPIO2_PIN_CTL	Go
0x13	GPIO3_PIN_CTL	GPIO3_PIN_CTL	Go
0x14	GPIO4_PIN_CTL	GPIO4_PIN_CTL	Go
0x15	GPIO5_PIN_CTL	GPIO5_PIN_CTL	Go
0x16	GPIO6_PIN_CTL	GPIO6_PIN_CTL	Go
0x17	GPIO7_PIN_CTL	GPIO7_PIN_CTL	Go
0x18	FS_CTL	FS_CTL	Go
0x19	FS_HIGH_TIME_1	FS_HIGH_TIME_1	Go
0x1A	FS_HIGH_TIME_0	FS_HIGH_TIME_0	Go
0x1B	FS_LOW_TIME_1	FS_LOW_TIME_1	Go
0x1C	FS_LOW_TIME_0	FS_LOW_TIME_0	Go
0x1D	MAX_FRM_HI	MAX_FRM_HI	Go
0x1E	MAX_FRM_LO	MAX_FRM_LO	Go
0x1F	CSI_PLL_CTL	CSI_PLL_CTL	Go
0x20	FWD_CTL1	FWD_CTL1	Go
0x21	FWD_CTL2	FWD_CTL2	Go
0x22	FWD_STS	FWD_STS	Go
0x23	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x24	INTERRUPT_STS	INTERRUPT_STS	Go
0x25	TS_CONFIG	TS_CONFIG	Go
0x26	TS_CONTROL	TS_CONTROL	Go
0x27	TS_LINE_HI	TS_LINE_HI	Go
0x28	TS_LINE_LO	TS_LINE_LO	Go
0x29	TS_STATUS	TS_STATUS	Go
0x2A	TIMESTAMP_P0_HI	TIMESTAMP_P0_HI	Go
0x2B	TIMESTAMP_P0_LO	TIMESTAMP_P0_LO	Go
0x2C	TIMESTAMP_P1_HI	TIMESTAMP_P1_HI	Go
0x2D	TIMESTAMP_P1_LO	TIMESTAMP_P1_LO	Go
0x2E	TIMESTAMP_P2_HI	TIMESTAMP_P2_HI	Go
0x2F	TIMESTAMP_P2_LO	TIMESTAMP_P2_LO	Go
0x30	TIMESTAMP_P3_HI	TIMESTAMP_P3_HI	Go
0x31	TIMESTAMP_P3_LO	TIMESTAMP_P3_LO	Go

Table 8-19. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x32	CSI_PORT_SEL	CSI_PORT_SEL	Go
0x33	CSI_CTL	CSI_CTL	Go
0x34	CSI_CTL2	CSI_CTL2	Go
0x35	CSI_STS	CSI_STS	Go
0x36	CSI_TX_ICR	CSI_TX_ICR	Go
0x37	CSI_TX_ISR	CSI_TX_ISR	Go
0x38	CSI_TEST_CTL	CSI_TEST_CTL	Go
0x39	CSI_TEST_PATT_HI	CSI_TEST_PATT_HI	Go
0x3A	CSI_TEST_PATT_LO	CSI_TEST_PATT_LO	Go
0x3B	CSI_EXCLUSIVE_FWD1	CSI_EXCLUSIVE_FWD1	Go
0x3C	CSI_EXCLUSIVE_FWD2	CSI_EXCLUSIVE_FWD2	Go
0x3D	REFCLK_FREQ	REFCLK_FREQ	Go
0x3E	BC_CTRL	BC_CTRL	Go
0x46	BCC_ERR_CTL	BCC_ERR_CTL	Go
0x47	BCC_STATUS	BCC_STATUS	Go
0x4B	RAW_EMBED_DTYPE	RAW_EMBED_DTYPE	Go
0x4C	FPD3_PORT_SEL	FPD3_PORT_SEL	Go
0x4D	RX_PORT_STS1	RX_PORT_STS1	Go
0x4E	RX_PORT_STS2	RX_PORT_STS2	Go
0x4F	RX_FREQ_HIGH	RX_FREQ_HIGH	Go
0x50	RX_FREQ_LOW	RX_FREQ_LOW	Go
0x51	SENSOR_STS_0	SENSOR_STS_0	Go
0x52	SENSOR_STS_1	SENSOR_STS_1	Go
0x53	SENSOR_STS_2	SENSOR_STS_2	Go
0x54	SENSOR_STS_3	SENSOR_STS_3	Go
0x55	RX_PAR_ERR_HI	RX_PAR_ERR_HI	Go
0x56	RX_PAR_ERR_LO	RX_PAR_ERR_LO	Go
0x57	BIST_ERR_COUNT	BIST_ERR_COUNT	Go
0x58	BCC_CONFIG	BCC_CONFIG	Go
0x59	DATAPATH_CTL1	DATAPATH_CTL1	Go
0x5B	SER_ID	SER_ID	Go
0x5C	SER_ALIAS_ID	SER_ALIAS_ID	Go
0x5D	SLAVE_ID_0	SLAVE_ID_0	Go
0x5E	SLAVE_ID_1	SLAVE_ID_1	Go
0x5F	SLAVE_ID_2	SLAVE_ID_2	Go
0x60	SLAVE_ID_3	SLAVE_ID_3	Go
0x61	SLAVE_ID_4	SLAVE_ID_4	Go
0x62	SLAVE_ID_5	SLAVE_ID_5	Go
0x63	SLAVE_ID_6	SLAVE_ID_6	Go
0x64	SLAVE_ID_7	SLAVE_ID_7	Go
0x65	SLAVE_ALIAS_0	SLAVE_ALIAS_0	Go
0x66	SLAVE_ALIAS_1	SLAVE_ALIAS_1	Go
0x67	SLAVE_ALIAS_2	SLAVE_ALIAS_2	Go
0x68	SLAVE_ALIAS_3	SLAVE_ALIAS_3	Go
0x69	SLAVE_ALIAS_4	SLAVE_ALIAS_4	Go

Table 8-19. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x6A	SLAVE_ALIAS_5	SLAVE_ALIAS_5	Go
0x6B	SLAVE_ALIAS_6	SLAVE_ALIAS_6	Go
0x6C	SLAVE_ALIAS_7	SLAVE_ALIAS_7	Go
0x6D	PORT_CONFIG	PORT_CONFIG	Go
0x6E	BC_GPIO_CTL0	BC_GPIO_CTL0	Go
0x6F	BC_GPIO_CTL1	BC_GPIO_CTL1	Go
0x70	RAW10_ID	RAW10_ID	Go
0x71	RAW12_ID	RAW12_ID	Go
0x73	LINE_COUNT_1	LINE_COUNT_1	Go
0x74	LINE_COUNT_0	LINE_COUNT_0	Go
0x75	LINE_LEN_1	LINE_LEN_1	Go
0x76	LINE_LEN_0	LINE_LEN_0	Go
0x77	FPD3_FREQ_DET_CTL	FPD3_FREQ_DET_CTL	Go
0x78	MAILBOX_1	MAILBOX_1	Go
0x79	MAILBOX_2	MAILBOX_2	Go
0x7A	CSI_RX_STS	CSI_RX_STS	Go
0x7B	CSI_ERR_COUNTER	CSI_ERR_COUNTER	Go
0x7C	PORT_CONFIG2	PORT_CONFIG2	Go
0x7D	PORT_PASS_CTL	PORT_PASS_CTL	Go
0x7E	SEN_INT_RISE_CTL	SEN_INT_RISE_CTL	Go
0x7F	SEN_INT_FALL_CTL	SEN_INT_FALL_CTL	Go
0x88	FFD_CTL	FFD_CTL	Go
0x89	GPIO9_PIN_CTL	GPIO9_PIN_CTL	Go
0x8A	GPIO10_PIN_CTL	GPIO10_PIN_CTL	Go
0x8B	GPIO_INPUT_CTL_2	GPIO_INPUT_CTL_2	Go
0x8C	REFCLK_DET_INT_CTL	REFCLK_DET_INT_CTL	Go
0x90	CSI0_FRAME_COUNT_HI	CSI0_FRAME_COUNT_HI	Go
0x91	CSI0_FRAME_COUNT_LO	CSI0_FRAME_COUNT_LO	Go
0x92	CSI0_FRAME_ERR_COUNT_HI	CSI0_FRAME_ERR_COUNT_HI	Go
0x93	CSI0_FRAME_ERR_COUNT_LO	CSI0_FRAME_ERR_COUNT_LO	Go
0x94	CSI0_LINE_COUNT_HI	CSI0_LINE_COUNT_HI	Go
0x95	CSI0_LINE_COUNT_LO	CSI0_LINE_COUNT_LO	Go
0x96	CSI0_LINE_ERR_COUNT_HI	CSI0_LINE_ERR_COUNT_HI	Go
0x97	CSI0_LINE_ERR_COUNT_LO	CSI0_LINE_ERR_COUNT_LO	Go
0x98	CSI1_FRAME_COUNT_HI	CSI1_FRAME_COUNT_HI	Go
0x99	CSI1_FRAME_COUNT_LO	CSI1_FRAME_COUNT_LO	Go
0x9A	CSI1_FRAME_ERR_COUNT_HI	CSI1_FRAME_ERR_COUNT_HI	Go
0x9B	CSI1_FRAME_ERR_COUNT_LO	CSI1_FRAME_ERR_COUNT_LO	Go
0x9C	CSI1_LINE_COUNT_HI	CSI1_LINE_COUNT_HI	Go
0x9D	CSI1_LINE_COUNT_LO	CSI1_LINE_COUNT_LO	Go
0x9E	CSI1_LINE_ERR_COUNT_HI	CSI1_LINE_ERR_COUNT_HI	Go
0x9F	CSI1_LINE_ERR_COUNT_LO	CSI1_LINE_ERR_COUNT_LO	Go
0xA0	VC_ID_MAP_0	VC_ID_MAP_0	Go
0xA1	VC_ID_MAP_1	VC_ID_MAP_1	Go
0xA2	VC_ID_MAP_2	VC_ID_MAP_2	Go

Table 8-19. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0xA3	VC_ID_MAP_3	VC_ID_MAP_3	Go
0xA4	VC_ID_MAP_4	VC_ID_MAP_4	Go
0xA5	VC_ID_MAP_5	VC_ID_MAP_5	Go
0xA6	VC_ID_MAP_6	VC_ID_MAP_6	Go
0xA7	VC_ID_MAP_7	VC_ID_MAP_7	Go
0xB0	IND_ACC_CTL	IND_ACC_CTL	Go
0xB1	IND_ACC_ADDR	IND_ACC_ADDR	Go
0xB2	IND_ACC_DATA	IND_ACC_DATA	Go
0xB3	BIST_CTL	BIST_CTL	Go
0xB8	MODE_CAD_STS	MODE_CAD_STS	Go
0xB9	LINK_ERROR_COUNT	LINK_ERROR_COUNT	Go
0xBA	DCA_CONTROL	DCA_CONTROL	Go
0xBB	CSI_PLL_CTL2	CSI_PLL_CTL2	Go
0xBC	FV_MIN_TIME	FV_MIN_TIME	Go
0xBE	GPIO_PD_CTL	GPIO_PD_CTL	Go
0xC2	IQ_DIV	IQ_DIV	Go
0xC7	CSI_PORT2_FIFO_CTRL	CSI_PORT2_FIFO_CTRL	Go
0xC9	CSI_PLL_DIV	CSI_PLL_DIV	Go
0xCA	LOCAL_DEV_ICR	LOCAL_DEV_ICR	Go
0xCB	LOCAL_DEV_ISR	LOCAL_DEV_ISR	Go
0xCF	EXCLUSIVE_FWD_STS	EXCLUSIVE_FWD_STS	Go
0xD0	PORT_DEBUG	PORT_DEBUG	Go
0xD5	CMLOUT_TEST_PAT_0	CMLOUT_TEST_PAT_0	Go
0xD6	CMLOUT_TEST_PAT_1	CMLOUT_TEST_PAT_1	Go
0xD8	PORT_ICR_HI	PORT_ICR_HI	Go
0xD9	PORT_ICR_LO	PORT_ICR_LO	Go
0xDA	PORT_ISR_HI	PORT_ISR_HI	Go
0xDB	PORT_ISR_LO	PORT_ISR_LO	Go
0xDC	FC_GPIO_STS	FC_GPIO_STS	Go
0xDD	FC_GPIO_ICR	FC_GPIO_ICR	Go
0xDE	SEN_INT_RISE_STS	SEN_INT_RISE_STS	Go
0xDF	SEN_INT_FALL_STS	SEN_INT_FALL_STS	Go
0xE0	CML_CTRL_1	CML_CTRL_1	Go
0xE1	CML_CTRL_2	CML_CTRL_2	Go
0xE2	BC_AND_CML_CTRL	BC_AND_CML_CTRL	Go
0xE4	CHANNEL_MODE	CHANNEL_MODE	Go
0xE9	SAR_ADC_DOUT	SAR_ADC_DOUT	Go
0xF0	FPD_RX_ID0	FPD_RX_ID0	Go
0xF1	FPD_RX_ID1	FPD_RX_ID1	Go
0xF2	FPD_RX_ID2	FPD_RX_ID2	Go
0xF3	FPD_RX_ID3	FPD_RX_ID3	Go
0xF4	FPD_RX_ID4	FPD_RX_ID4	Go
0xF5	FPD_RX_ID5	FPD_RX_ID5	Go
0xF6	FPD_RX_ID6	FPD_RX_ID6	Go
0xF8	I2C_RX0_ID	I2C_RX0_ID	Go

Table 8-19. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0xF9	I2C_RX1_ID	I2C_RX1_ID	Go
0xFA	I2C_RX2_ID	I2C_RX2_ID	Go
0xFB	I2C_RX3_ID	I2C_RX3_ID	Go
0xFC	FFD_ICR_HI	FFD_ICR_HI	Go
0xFD	FFD_ICR_LO	FFD_ICR_LO	Go
0xFE	FFD_ISR_HI	FFD_ISR_HI	Go
0xFF	FFD_ISR_LO	FFD_ISR_LO	Go

8.6.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Default = 0x00]I2C_DEVICE_ID is shown in [I2C_DEVICE_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-20. I2C_DEVICE_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	DEVICE_ID	R/W	0x0	7-bit I2C ID of Deserializer. Strap This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 1 of this register is 1, this field is read/write and can be used to assign any valid I2C ID. At power-up, this field is set based on the IDX pin strap value.
0	DES_ID	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

8.6.1.2 RESET_CTL Register (Address = 0x1) [Default = 0x00]RESET_CTL is shown in [RESET_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-21. RESET_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	GPIO_HOLD_B	R/W	0x0	GPIO hold control 0: GPIO hold active 1: GPIO hold released
4-3	RESERVED	R	0x0	Reserved
2	RESTART_AUTOLOAD	RH/W1S	0x0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software may check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
1	DIGITAL_RESET1	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

8.6.1.3 GENERAL_CFG Register (Address = 0x2) [Default = 0x1E]GENERAL_CFG is shown in [GENERAL_CFG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-22. GENERAL_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SPI_MODE_EN	R/W	0x0	SPI Mode enable (Override option for strap from GPIO1)
5	I2C_MASTER_EN	R/W	0x0	I2C Master Enable When this bit is 0, the local I2C master is disabled, when it is 1, the master is enabled
4	OUTPUT_EN_MODE	R/W	0x1	Output Enable Mode If set to 0, the CSI TX output port will be forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1, the CSI TX output port will continue in normal operation if no assigned RX ports have an active Receiver lock. CSI TX operation will remain under register control via the CSI_CTL register for each port. If no assigned RX ports have an active Receiver lock, this will result in the CSI Transmitter entering the LP-11 state.
3	OUTPUT_ENABLE	R/W	0x1	Output Enable Control (in conjunction with Output Sleep State Select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the CSI TX outputs will be forced into a high impedance state.
2	OUTPUT_SLEEP_STATE_SEL	R/W	0x1	OSS Select to control output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the CSI TX outputs will be forced into a HS-0 state.
1	RX_PARITY_CHECK_EN	R/W	0x1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
0	FORCE_REFCLK_DET	R/W	0x0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present

8.6.1.4 REV_MASK_ID Register (Address = 0x3) [Default = 0x40]REV_MASK_ID is shown in [REV_MASK_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-23. REV_MASK_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	REVISION_ID	R	0x4	Revision ID 0010: CS1.0 or CS2.0 0100: DS90UB9702-Q1
3-0	RESERVED	R	0x0	Reserved

8.6.1.5 DEVICE_STS Register (Address = 0x4) [Default = 0xD0]DEVICE_STS is shown in [DEVICE_STS Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-24. DEVICE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	CFG_CKSUM_STS	R	0x1	Config Checksum Passed This bit will be set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	0x1	Power-up initialization complete This bit will be set after Initialization is complete. Configuration from eFuse ROM has completed.
5	RX_PLL_LOCK	R	0x0	Reserved
4	REFCLK_VALID	R	0x1	REFCLK valid frequency This bit indicates when a valid frequency has been detected on the REFCLK pin. 0: invalid frequency detected 1: REFCLK frequency between 12MHz and 64MHz
3-2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.1.6 PAR_ERR_THOLD1 Register (Address = 0x5) [Default = 0x01]PAR_ERR_THOLD1 is shown in [PAR_ERR_THOLD1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-25. PAR_ERR_THOLD1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PAR_ERR_THOLD_HI	R/W	0x1	FPD3 Parity Error Threshold High byte This register provides the 8 most significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag will be set in the RX_PORT_STS1 register.

8.6.1.7 PAR_ERR_THOLD0 Register (Address = 0x6) [Default = 0x00]PAR_ERR_THOLD0 is shown in [PAR_ERR_THOLD0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-26. PAR_ERR_THOLD0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PAR_ERR_THOLD_LO	R/W	0x0	FPD3 Parity Error Threshold Low byte This register provides the 8 least significant bits of the Parity Error Threshold value. For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag will be set in the RX_PORT_STS1 register.

8.6.1.8 BCC_Watchdog_Control Register (Address = 0x7) [Default = 0xFE]BCC_Watchdog_Control is shown in [BCC_Watchdog_Control Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-27. BCC_Watchdog_Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	BCC_WATCHDOG_TIME_R	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WATCHDOG_TIME_R_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

8.6.1.9 I2C_Control_1 Register (Address = 0x8) [Default = 0x1C]I2C_Control_1 is shown in [I2C_Control_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-28. I2C_Control_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LOCAL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
6-4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3-0	I2C_FILTER_DEPTH	R/W	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

8.6.1.10 I2C_Control_2 Register (Address = 0x9) [Default = 0x12]I2C_Control_2 is shown in [I2C_Control_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-29. I2C_Control_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	SDA_Output_Setup	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3-2	SDA_Output_Delay	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEED_UP	R/W	0x1	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.

Table 8-29. I2C_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	I2C_BUS_TIMER_DISABLE	R/W	0x0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.

8.6.1.11 SCL_High_Time Register (Address = 0xA) [Default = 0x7A]SCL_High_Time is shown in [SCL_High_Time Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-30. SCL_High_Time Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SCL_HIGH_TIME	R/W	0x7A	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional oscillator clock periods. Min_delay= 39.996ns * (SCL_HIGH_TIME + 5)

8.6.1.12 SCL_Low_Time Register (Address = 0xB) [Default = 0x7A]SCL_Low_Time is shown in [SCL_Low_Time Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-31. SCL_Low_Time Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SCL_LOW_TIME	R/W	0x7A	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional clock periods. Min_delay= 39.996ns * (SCL_LOW_TIME+ 5)

8.6.1.13 RX_PORT_CTL Register (Address = 0xC) [Default = 0x00]RX_PORT_CTL is shown in [RX_PORT_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-32. RX_PORT_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	BCC3_MAP	R/W	0x0	Map Control Channel 3 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
6	BCC2_MAP	R/W	0x0	Map Control Channel 2 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1

Table 8-32. RX_PORT_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	BCC1_MAP	R/W	0x0	Map Control Channel 1 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
4	BCC0_MAP	R/W	0x0	Map Control Channel 0 to I2C Slave Port 0: I2C Slave Port 0 1: I2C Slave Port 1
3	PORT3_EN	R/W	0x0	Port 3 Receiver Enable 0: Disable Port 3 Receiver 1: Enable Port 3 Receiver
2	PORT2_EN	R/W	0x0	Port 2 Receiver Enable 0: Disable Port 2 Receiver 1: Enable Port 2 Receiver
1	PORT1_EN	R/W	0x0	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver
0	PORT0_EN	R/W	0x0	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver

8.6.1.14 IO_CTL Register (Address = 0xD) [Default = 0x09]IO_CTL is shown in [IO_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-33. IO_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	SEL3P3V	R/W	0x0	3.3V I/O Select on pins PDB,TESTEN, INTB,I2C 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
6	IO_SUPPLY_MODE_OV	R/W	0x0	Override I/O Supply Mode bit If set to 0, the detected voltage level will be used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields will be used.
5-4	IO_SUPPLY_MODE	R/W	0x0	I/O Supply Mode 00: 1.8V 01: Reserved 10: Reserved 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
3-0	IMP_CTRL	R/W	0x9	GPIO Output Impedance Control

8.6.1.15 GPIO_PIN_STS Register (Address = 0xE) [Default = 0x00]GPIO_PIN_STS is shown in [GPIO_PIN_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-34. GPIO_PIN_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on each of the 8 GPIO pins. Bit 7 reads GPIO7 and bit 0 reads GPIO0.

8.6.1.16 GPIO_INPUT_CTL Register (Address = 0xF) [Default = 0xEF]

GPIO_INPUT_CTL is shown in [GPIO_INPUT_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-35. GPIO_INPUT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0: Disabled 1: Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0: Disabled 1: Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	0x0	GPIO4 Input Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

8.6.1.17 GPIO0_PIN_CTL Register (Address = 0x10) [Default = 0x00]

GPIO0_PIN_CTL is shown in [GPIO0_PIN_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-36. GPIO0_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO0_OUT_SEL	R/W	0x0	<p>GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO0_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved</p>
4-2	GPIO0_OUT_SRC	R/W	0x0	<p>GPIO0 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1</p>
1	GPIO0_OUT_VAL	R/W	0x0	<p>GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO0_OUT_EN	R/W	0x0	<p>GPIO0 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.18 GPIO1_PIN_CTL Register (Address = 0x11) [Default = 0x00]GPIO1_PIN_CTL is shown in [GPIO1_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-37. GPIO1_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO1_OUT_SEL	R/W	0x0	<p>GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO1_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO1_OUT_SRC	R/W	0x0	<p>GPIO1 Output Source Select Selects output source for GPIO1 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO1_OUT_VAL	R/W	0x0	<p>GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO1_OUT_EN	R/W	0x0	<p>GPIO1 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.19 GPIO2_PIN_CTL Register (Address = 0x12) [Default = 0x00]GPIO2_PIN_CTL is shown in [GPIO2_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-38. GPIO2_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO2_OUT_SEL	R/W	0x0	<p>GPIO02 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO2_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO2_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO2_OUT_SRC	R/W	0x0	<p>GPIO2 Output Source Select Selects output source for GPIO2 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO2_OUT_VAL	R/W	0x0	<p>GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO2_OUT_EN	R/W	0x0	<p>GPIO2 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.20 GPIO3_PIN_CTL Register (Address = 0x13) [Default = 0x00]GPIO3_PIN_CTL is shown in [GPIO3_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-39. GPIO3_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO3_OUT_SEL	R/W	0x0	<p>GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO3_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO3_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO3_OUT_SRC	R/W	0x0	<p>GPIO3 Output Source Select Selects output source for GPIO3 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO3_OUT_VAL	R/W	0x0	<p>GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO3_OUT_EN	R/W	0x0	<p>GPIO3 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.21 GPIO4_PIN_CTL Register (Address = 0x14) [Default = 0x31]

GPIO4_PIN_CTL is shown in [GPIO4_PIN_CTL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-40. GPIO4_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO4_OUT_SEL	R/W	0x1	<p>GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO4_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO4_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO4_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO4_OUT_SRC	R/W	0x4	<p>GPIO4 Output Source Select Selects output source for GPIO4 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO4_OUT_VAL	R/W	0x0	<p>GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO4_OUT_EN	R/W	0x1	<p>GPIO4 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.22 GPIO5_PIN_CTL Register (Address = 0x15) [Default = 0x00]GPIO5_PIN_CTL is shown in [GPIO5_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-41. GPIO5_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO5_OUT_SEL	R/W	0x0	<p>GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO5_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO5_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO5_OUT_SRC	R/W	0x0	<p>GPIO5 Output Source Select Selects output source for GPIO5 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO5_OUT_VAL	R/W	0x0	<p>GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO5_OUT_EN	R/W	0x0	<p>GPIO5 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.23 GPIO6_PIN_CTL Register (Address = 0x16) [Default = 0x00]GPIO6_PIN_CTL is shown in [GPIO6_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-42. GPIO6_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO6_OUT_SEL	R/W	0x0	<p>GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 00x (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO6_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO6_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: Reserved <p>If GPIO6_OUT_SRC is set to 110 (the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Ports Synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO6_OUT_SRC	R/W	0x0	<p>GPIO6 Output Source Select Selects output source for GPIO6 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO6_OUT_VAL	R/W	0x0	<p>GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO6_OUT_EN	R/W	0x0	<p>GPIO6 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.24 GPIO7_PIN_CTL Register (Address = 0x17) [Default = 0x00]GPIO7_PIN_CTL is shown in [GPIO7_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-43. GPIO7_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO7_OUT_SEL	R/W	0x0	<p>GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 00x (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO7_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO7_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: Reserved <p>If GPIO7_OUT_SRC is set to 110 (the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Ports Synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO7_OUT_SRC	R/W	0x0	<p>GPIO7 Output Source Select Selects output source for GPIO7 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO7_OUT_VAL	R/W	0x0	<p>GPIO7 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO7_OUT_EN	R/W	0x0	<p>GPIO7 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.25 FS_CTL Register (Address = 0x18) [Default = 0x00]FS_CTL is shown in [FS_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-44. FS_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	FS_MODE	R/W	0x0	<p>FrameSync Mode</p> <p>0000: Internal Generated FrameSync, use Back-channel frame clock from port 0</p> <p>0001: Internal Generated FrameSync, use Back-channel frame clock from port 1</p> <p>0010: Internal Generated FrameSync, use Back-channel frame clock from port 2</p> <p>0011: Internal Generated FrameSync, use Back-channel frame clock from port 3</p> <p>01xx: Internal Generated FrameSync, use 25MHz clock</p> <p>1000: External FrameSync from GPIO0</p> <p>1001: External FrameSync from GPIO1</p> <p>1010: External FrameSync from GPIO2</p> <p>1011: External FrameSync from GPIO3</p> <p>1100: External FrameSync from GPIO4</p> <p>1101: External FrameSync from GPIO5</p> <p>1110: External FrameSync from GPIO6</p> <p>1111: External FrameSync from GPIO7</p>
3	FS_SINGLE	RH/W1S	0x0	<p>Generate Single FrameSync pulse</p> <p>When this bit is set, a single FrameSync pulse will be generated. The system should wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit should remain set to 0. This bit is self-clearing and will always return 0.</p>
2	FS_INIT_STATE	R/W	0x0	<p>FrameSync Initial State</p> <p>This register controls the initial state of the FrameSync signal.</p> <p>0: FrameSync initial state is 0</p> <p>1: FrameSync initial state is 1</p>
1	FS_GEN_MODE	R/W	0x0	<p>FrameSync Generation Mode</p> <p>This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator will use the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the High and Low periods for the generated FrameSync signal. FrameSync times are based on the settings of the FS_MODE field. In 50/50 mode, the FrameSync generator will use the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal.</p> <p>0: Hi/Lo</p> <p>1: 50/50</p>
0	FS_GEN_ENABLE	R/W	0x0	<p>FrameSync Generation Enable</p> <p>0: Disabled</p> <p>1: Enabled</p>

8.6.1.26 FS_HIGH_TIME_1 Register (Address = 0x19) [Default = 0x00]FS_HIGH_TIME_1 is shown in [FS_HIGH_TIME_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-45. FS_HIGH_TIME_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FRAMESYNC_HIGH_TIME_1	R/W	0x0	<p>FrameSync High Time bits 15:8</p> <p>The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.</p>

8.6.1.27 FS_HIGH_TIME_0 Register (Address = 0x1A) [Default = 0x00]

FS_HIGH_TIME_0 is shown in [FS_HIGH_TIME_0 Register Field Descriptions](#).

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Table 8-46. FS_HIGH_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FRAMESYNC_HIGH_TIME_0	R/W	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

8.6.1.28 FS_LOW_TIME_1 Register (Address = 0x1B) [Default = 0x00]

FS_LOW_TIME_1 is shown in [FS_LOW_TIME_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-47. FS_LOW_TIME_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FRAMESYNC_LOW_TIME_1	R/W	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

8.6.1.29 FS_LOW_TIME_0 Register (Address = 0x1C) [Default = 0x00]

FS_LOW_TIME_0 is shown in [FS_LOW_TIME_0 Register Field Descriptions](#).

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Table 8-48. FS_LOW_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FRAMESYNC_LOW_TIME_0	R/W	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

8.6.1.30 MAX_FRM_HI Register (Address = 0x1D) [Default = 0x00]

MAX_FRM_HI is shown in [MAX_FRM_HI Register Field Descriptions](#).

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Table 8-49. MAX_FRM_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	MAX_FRAME_HI	R/W	0x0	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver will create CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

8.6.1.31 MAX_FRM_LO Register (Address = 0x1E) [Default = 0x04]MAX_FRM_LO is shown in [MAX_FRM_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-50. MAX_FRM_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	MAX_FRAME_LO	R/W	0x4	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver will create CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

8.6.1.32 CSI_PLL_CTL Register (Address = 0x1F) [Default = 0x10]CSI_PLL_CTL is shown in [CSI_PLL_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-51. CSI_PLL_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	CSI_TX_SPEED[2]	R/W	0x1	CSI timing register select MSB 'Strap 2.5G: 1'b1 800M: '1'b0 See CSI_TX_SPEED[1:0] description At power-up, this field is set based on the MODE pin strap value.
3	RESERVED	R/W	0x0	Reserved
2	REF_CLK_MODE	R/W	0x0	Reference Clock mode The digital logic requires a 200 MHz reference clock generated from the CSI PLL. If this bit is set to 1, the reference clock will be 100 MHz. 0: clock is 200 MHz 1: clock is 100 MHz
1-0	CSI_TX_SPEED[1:0]	R/W	0x0	CSI timing register select: 'Strap 2.5G: 2'h0 800M: '2'h2 This register selects the operating rate and CSI timing parameters for the CSI Transmitter. In addition to setting this field, the CSI_PLL_DIV register should also be programmed for the correct divider selection. 0_00: 1.6 Gbps serial rate 0_01: 1.2 Gbps serial rate 0_10: 800 Mbps serial rate 0_11: 400 Mbps serial rate 1_xx: 2.5 Gbps serial rate At power-up, this field is set based on the MODE pin strap value.

8.6.1.33 FWD_CTL1 Register (Address = 0x20) [Default = 0xF0]FWD_CTL1 is shown in [FWD_CTL1 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-52. FWD_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FWD_PORT3_DIS	R/W	0x1	Disable forwarding of RX Port 3 0: Forwarding enabled 1: Forwarding disabled
6	FWD_PORT2_DIS	R/W	0x1	Disable forwarding of RX Port 2 0: Forwarding enabled 1: Forwarding disabled
5	FWD_PORT1_DIS	R/W	0x1	Disable forwarding of RX Port 1 0: Forwarding enabled 1: Forwarding disabled
4	FWD_PORT0_DIS	R/W	0x1	Disable forwarding of RX Port 0 0: Forwarding enabled 1: Forwarding disabled
3	RX3_MAP	R/W	0x0	Map RX Port 3 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
2	RX2_MAP	R/W	0x0	Map RX Port 2 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
1	RX1_MAP	R/W	0x0	Map RX Port 1 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
0	RX0_MAP	R/W	0x0	Map RX Port 0 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.

8.6.1.34 FWD_CTL2 Register (Address = 0x21) [Default = 0x03]

FWD_CTL2 is shown in [FWD_CTL2 Register Field Descriptions](#).

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Table 8-53. FWD_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FWD_SYNC_AS_AVAIL	R/W	0x0	Synchronized Forwarding As Available During Synchronized Forwarding, each forwarding engine will wait for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 will allow sending the next video line as it becomes available. For example if RX Ports 0 and 1 are being forwarded, port 0 video line will be forwarded when it becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation may reduce the likelihood of buffer overflow errors in some conditions. This bit will have no affect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. This bit applies to both CSI output ports

Table 8-53. FWD_CTL2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-4	CSI1_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 1 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
3-2	CSI0_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 0 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.
1	CSI1_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 1. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
0	CSI0_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 0. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.

8.6.1.35 FWD_STS Register (Address = 0x22) [Default = 0x00]FWD_STS is shown in [FWD_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-54. FWD_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	CSI_REPLICATE_CSI1	R/W	0x0	CSI Replicate Mode for CSI PORT 1 Setting this bit enables 2-lane Replication mode for CSI Port 1. When enabled, data on lanes 0/1 will be replicated to lanes 2/3 for CSI Port 1. In DPHY mode, the 2nd clock pin will also be enabled the port.
4	CSI_REPLICATE_CSI0	R/W	0x0	CSI Replicate Mode for CSI PORT 0 Setting this bit enables 2-lane Replication mode for CSI Port 0. When enabled, data on lanes 0/1 will be replicated to lanes 2/3 for CSI Port 0. In DPHY mode, the 2nd clock pin will also be enabled the port.
3	FWD_SYNC_FAIL1	RC	0x0	Forwarding synchronization failed for CSI output port 1 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.

Table 8-54. FWD_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	FWD_SYNC_FAIL0	RC	0x0	Forwarding synchronization failed for CSI output port 0 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
1	FWD_SYNC1	R	0x0	Forwarding synchronized for CSI output port 1 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized
0	FWD_SYNC0	R	0x0	Forwarding synchronized for CSI output port 0 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized

8.6.1.36 INTERRUPT_CTL Register (Address = 0x23) [Default = 0x00]INTERRUPT_CTL is shown in [INTERRUPT_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-55. INTERRUPT_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
6	IE_DEV	R/W	0x0	Local Device Interrupt. Enable interrupts for general device functions such as TEMP sensor, Voltage sensor, line fault, etc. See the LOCAL_DEV_ICR register for the functions that can generate the local device interrupts.
5	IE_CSI_TX1	R/W	0x0	CSI Transmit Port 1 Interrupt: Enable interrupt from CSI Transmitter Port 1.
4	IE_CSI_TX0	R/W	0x0	CSI Transmit Port 0 Interrupt: Enable interrupt from CSI Transmitter Port 0.
3	IE_RX3	R/W	0x0	RX Port 3 Interrupt: Enable interrupt from Receiver Port 3.
2	IE_RX2	R/W	0x0	RX Port 2 Interrupt: Enable interrupt from Receiver Port 2.
1	IE_RX1	R/W	0x0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
0	IE_RX0	R/W	0x0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.

8.6.1.37 INTERRUPT_STS Register (Address = 0x24) [Default = 0x00]INTERRUPT_STS is shown in [INTERRUPT_STS Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-56. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit will be set to 1.
6	IS_DEV	R	0x0	Local Device Interrupt: A general device interrupt has been generated. If this bit is set, the LOCAL_DEV_ISR register should be read to determine the source of the interrupt. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt.
5	IS_CSI_TX1	R	0x0	CSI Transmit Port 1 Interrupt: An interrupt has occurred for CSI Transmitter Port 1. This interrupt will be cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 1.
4	IS_CSI_TX0	R	0x0	CSI Transmit Port 0 Interrupt: An interrupt has occurred for CSI Transmitter Port 0. This interrupt will be cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 0.
3	IS_RX3	R	0x0	RX Port 3 Interrupt: An interrupt has occurred for Receive Port 3. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
2	IS_RX2	R	0x0	RX Port 2 Interrupt: An interrupt has occurred for Receive Port 2. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
1	IS_RX1	R	0x0	RX Port 1 Interrupt: An interrupt has occurred for Receive Port 1. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
0	IS_RX0	R	0x0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

8.6.1.38 TS_CONFIG Register (Address = 0x25) [Default = 0x00]TS_CONFIG is shown in [TS_CONFIG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-57. TS_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FS_POLARITY	R/W	0x0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
5-4	TS_RES_CTL	R/W	0x0	Timestamp Resolution Control 00: 40 ns 01: 80 ns 10: 160 ns 11: 1.0 us

Table 8-57. TS_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	TS_AS_AVAIL	R/W	0x0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
2	RESERVED	R	0x0	Reserved
1	TS_FREERUN	R/W	0x0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
0	TS_MODE	R/W	0x0	Timestamp Mode 0: Line start 1: Frame start

8.6.1.39 TS_CONTROL Register (Address = 0x26) [Default = 0x00]TS_CONTROL is shown in [TS_CONTROL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-58. TS_CONTROL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	TS_FREEZE	R/W	0x0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit will freeze timestamps and clear the TS_READY flag. The TS_FREEZE bit should be cleared after reading timestamps to resume operation.
3	TS_ENABLE3	R/W	0x0	Timestamp Enable RX Port 3 0: Disabled 1: Enabled
2	TS_ENABLE2	R/W	0x0	Timestamp Enable RX Port 2 0: Disabled 1: Enabled
1	TS_ENABLE1	R/W	0x0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
0	TS_ENABLE0	R/W	0x0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled

8.6.1.40 TS_LINE_HI Register (Address = 0x27) [Default = 0x00]TS_LINE_HI is shown in [TS_LINE_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-59. TS_LINE_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TS_LINE_HI	R/W	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

8.6.1.41 TS_LINE_LO Register (Address = 0x28) [Default = 0x00]TS_LINE_LO is shown in [TS_LINE_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-60. TS_LINE_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TS_LINE_LO	R/W	0x0	<p>Timestamp Line, lower 8 bits</p> <p>This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1.</p> <p>During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start</p>

8.6.1.42 TS_STATUS Register (Address = 0x29) [Default = 0x00]TS_STATUS is shown in [TS_STATUS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-61. TS_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	TS_READY	R	0x0	<p>Timestamp Ready</p> <p>This flag indicates when timestamps are ready to be read. This flag will be cleared when the TS_FREEZE bit is set.</p>
3	TS_VALID3	R	0x0	Timestamp Valid, RX Port 3
2	TS_VALID2	R	0x0	Timestamp Valid, RX Port 2
1	TS_VALID1	R	0x0	Timestamp Valid, RX Port 1
0	TS_VALID0	R	0x0	Timestamp Valid, RX Port 0

8.6.1.43 TIMESTAMP_P0_HI Register (Address = 0x2A) [Default = 0x00]TIMESTAMP_P0_HI is shown in [TIMESTAMP_P0_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-62. TIMESTAMP_P0_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0

8.6.1.44 TIMESTAMP_P0_LO Register (Address = 0x2B) [Default = 0x00]TIMESTAMP_P0_LO is shown in [TIMESTAMP_P0_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-63. TIMESTAMP_P0_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0

8.6.1.45 TIMESTAMP_P1_HI Register (Address = 0x2C) [Default = 0x00]TIMESTAMP_P1_HI is shown in [TIMESTAMP_P1_HI Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-64. TIMESTAMP_P1_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1

8.6.1.46 TIMESTAMP_P1_LO Register (Address = 0x2D) [Default = 0x00]TIMESTAMP_P1_LO is shown in [TIMESTAMP_P1_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-65. TIMESTAMP_P1_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1

8.6.1.47 TIMESTAMP_P2_HI Register (Address = 0x2E) [Default = 0x00]TIMESTAMP_P2_HI is shown in [TIMESTAMP_P2_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-66. TIMESTAMP_P2_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P2_HI	R	0x0	Timestamp, upper 8 bits, RX Port 2

8.6.1.48 TIMESTAMP_P2_LO Register (Address = 0x2F) [Default = 0x00]TIMESTAMP_P2_LO is shown in [TIMESTAMP_P2_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-67. TIMESTAMP_P2_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P2_LO	R	0x0	Timestamp, lower 8 bits, RX Port 2

8.6.1.49 TIMESTAMP_P3_HI Register (Address = 0x30) [Default = 0x00]TIMESTAMP_P3_HI is shown in [TIMESTAMP_P3_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-68. TIMESTAMP_P3_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P3_HI	R	0x0	Timestamp, upper 8 bits, RX Port 3

8.6.1.50 TIMESTAMP_P3_LO Register (Address = 0x31) [Default = 0x00]TIMESTAMP_P3_LO is shown in [TIMESTAMP_P3_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-69. TIMESTAMP_P3_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TIMESTAMP_P3_LO	R	0x0	Timestamp, lower 8 bits, RX Port 3

8.6.1.51 CSI_PORT_SEL Register (Address = 0x32) [Default = 0x00]CSI_PORT_SEL is shown in [CSI_PORT_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-70. CSI_PORT_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	TX_READ_PORT	R/W	0x0	Select TX port for register read This field selects one of the two TX port register blocks for readback. This applies to the subsequent registers prefixed CSI. 0: Port 0 registers 1: Port 1 registers
3-2	RESERVED	R	0x0	Reserved
1	TX_WRITE_PORT_1	R/W	0x0	Write Enable for TX port 1 registers This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled
0	TX_WRITE_PORT_0	R/W	0x0	Write Enable for TX port 0 registers This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled

8.6.1.52 CSI_CTL Register (Address = 0x33) [Default = 0x00]CSI_CTL is shown in [CSI_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-71. CSI_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	CSI_CAL_EN	R/W	0x0	Enable initial CSI Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI Transmitter will send the sequence at initialization, prior to sending any HS data. This bit should be set when operating at 1.6 Gbps CSI speed (as configured in the CSI_PLL register). 0: Disabled 1: Enabled
5-4	CSI_LANE_COUNT	R/W	0x0	CSI lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane
3-2	CSI_ULP	R/W	0x0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes
1	CSI_CONTS_CLOCK	R/W	0x0	Enable CSI continuous clock mode When enabled, the CSI Transmitter will enter continuous clock mode upon transmission of the first packet. 0: Disabled 1: Enabled

Table 8-71. CSI_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	CSI_ENABLE	R/W	0x0	Enable CSI output 0: Disabled 1: Enabled Forwarding should be disabled (via the FWD_CTL1 register) prior to enabling or disabling the CSI output.

8.6.1.53 CSI_CTL2 Register (Address = 0x34) [Default = 0x40]CSI_CTL2 is shown in [CSI_CTL2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-72. CSI_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CSI_CLK1_EN	R/W	0x0	Enable CSI_CLK1 output When this bit is set, the CSI_CLK1 will output the CSI clock signal. Note, the CSI_CLK1 output will also be enabled if the CSI_REPLICATE_CSI1 control is set in the FWD_STS register.
6	CSI_CLK0_EN	R/W	0x1	Enable CSI_CLK0 output When this bit is set, the CSI_CLK0 will output the CSI clock signal. Note, the CSI_CLK0 output will also be enabled if the CSI_REPLICATE_CSI0 control is set in the FWD_STS register.
5-4	CSI_CAL_LEN	R	0x0	These bits control the length of the periodic calibration sequence 00: 2 ¹⁰ bits 01: 2 ¹² bits 10: 2 ¹⁴ bits 11: 2 ¹⁵ bits
3	CSI_PASS_MODE	R/W	0x0	CSI PASS indication mode Determines whether the CSI Pass indication is for a single port or all enabled ports. 0: Assert PASS if at least one enabled Receive port is providing valid video data 1: Assert PASS only if ALL enabled Receive ports are providing valid video data
2	CSI_CAL_INV	R/W	0x0	CSI Calibration Inverted Data pattern During the CSI skew-calibration pattern, the CSI Transmitter will send a sequence of 01010101 data (first bit 0). Setting this bit to a 1 will invert the sequence to 10101010 data.
1	CSI_CAL_SINGLE	RH/W1S	0x0	Enable single periodic CSI Skew-Calibration sequence Setting this bit will send a single skew-calibration sequence from the CSI Transmitter. The skew-calibration sequence will be the 1010 bit sequence required for periodic calibration. The calibration sequence will be sent at the next idle period on the CSI interface. This bit is self-clearing and will reset to 0 after the calibration sequence is sent. Note: Adjust skew cal settings from CSI_CAL_LEN and CSI_CAL_INV with a separate register write prior to setting this bit
0	CSI_CAL_PERIODIC	R/W	0x0	Enable periodic CSI Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI Transmitter will send the periodic skew-calibration sequence following the sending of Frame End packets. Note: Adjust skew cal settings from CSI_CAL_LEN and CSI_CAL_INV with a separate register write prior to setting this bit 0: Disabled 1: Enabled

8.6.1.54 CSI_STS Register (Address = 0x35) [Default = 0x00]CSI_STS is shown in [CSI_STS Register Field Descriptions](#).

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Table 8-73. CSI_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	TX_PORT_NUM	R	0x0	TX Port Number This read-only field indicates the number of the currently selected TX read port.
3-2	RESERVED	R	0x0	Reserved
1	TX_PORT_SYNC	R	0x0	TX Port Synchronized This bit indicates the CSI Transmit Port is able to properly synchronize input data streams from multiple sources. This bit will be 0 if synchronization is disabled via the FWD_CTL2 register. 0: Input streams are not synchronized 1: Input streams are synchronized
0	PASS	R	0x0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In asynchronous operation, the TX_PORT_PASS indicates the CSI port is actively delivering valid video data. The status will be cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI TX output. Data may not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI transmit port.

8.6.1.55 CSI_TX_ICR Register (Address = 0x36) [Default = 0x00]

CSI_TX_ICR is shown in [CSI_TX_ICR Register Field Descriptions](#).

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Table 8-74. CSI_TX_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	IE_RX_PORT_INT	R/W	0x0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI Transmit Port.
3	IE_CSI_SYNC_ERROR	R/W	0x0	CSI Sync Error interrupt Enable Enable interrupt on CSI Synchronization enable.
2	IE_CSI_SYNC	R/W	0x0	CSI Synchronized interrupt Enable Enable interrupts on CSI Transmit Port assertion of CSI Synchronized Status.
1	IE_CSI_PASS_ERROR	R/W	0x0	CSI RX Pass Error interrupt Enable Enable interrupt on CSI Pass Error
0	IE_CSI_PASS	R/W	0x0	CSI Pass interrupt Enable Enable interrupt on CSI Transmit Port assertion of CSI Pass.

8.6.1.56 CSI_TX_ISR Register (Address = 0x37) [Default = 0x00]

CSI_TX_ISR is shown in [CSI_TX_ISR Register Field Descriptions](#).

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Table 8-75. CSI_TX_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	IS_RX_PORT_INT	R	0x0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI Transmit Port. A read of the associated port receive status registers will clear this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
3	IS_CSI_SYNC_ERROR	RC	0x0	CSI Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI Transmitter.
2	IS_CSI_SYNC	RC	0x0	CSI Synchronized interrupt CSI Transmit Port assertion of CSI Synchronized Status. Current status for CSI Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
1	IS_CSI_PASS_ERROR	RC	0x0	CSI RX Pass Error interrupt A deassertion of CSI Pass has been detected on one of the RX Ports being forwarded to the CSI Transmit Port
0	IS_CSI_PASS	RC	0x0	CSI Pass interrupt CSI Transmit Port assertion of CSI Pass detected. Current status for the CSI Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

8.6.1.57 CSI_TEST_CTL Register (Address = 0x38) [Default = 0x00]CSI_TEST_CTL is shown in [CSI_TEST_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-76. CSI_TEST_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CSI_BERT_HS	R/W	0x0	CSI BERT HS mode Setting this bit will force the CSI Transmitter into HS mode at all times. HS Drivers will be enabled. LP drivers will be disabled.
6-4	RESERVED	R/W	0x0	Reserved
3-0	CSI_TEST_MODE	R/W	0x0	CSI Test Mode Select 0000: Normal operation 0001: Outputs Tristate 0010: LP 0 Test mode 0011: LP 1 test mode 0100: LP Toggle Test 0101: HS 0 Test mode 0110: HS 1 Test mode 0111: HS Random Test 1000: HS Pattern Test (16-bits pattern from CSI_TEST_PATT_HI and CSI_TEST_PATT_LO register) 1001 - 1111: Reserved

8.6.1.58 CSI_TEST_PATT_HI Register (Address = 0x39) [Default = 0x00]CSI_TEST_PATT_HI is shown in [CSI_TEST_PATT_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-77. CSI_TEST_PATT_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_TEST_PATT	R/W	0x0	Bits 15:8 of fixed pattern for characterization test

8.6.1.59 CSI_TEST_PATT_LO Register (Address = 0x3A) [Default = 0x00]

CSI_TEST_PATT_LO is shown in [CSI_TEST_PATT_LO Register Field Descriptions](#).

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Table 8-78. CSI_TEST_PATT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CCI_TEST_PATT	R/W	0x0	Bits 7:0 of fixed pattern for characterization test

8.6.1.60 CSI_EXCLUSIVE_FWD1 Register (Address = 0x3B) [Default = 0xFF]

CSI_EXCLUSIVE_FWD1 is shown in [CSI_EXCLUSIVE_FWD1 Register Field Descriptions](#).

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Table 8-79. CSI_EXCLUSIVE_FWD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	CSI1_EXCLUSIVE_FWD	R/W	0xF	Exclusive Forward Mask for CSI Port 1 When EXCLUSIVE_FWD_EN is set to 1, this value determines which Receive Ports will be forwarded to CSI Transmit port 1. xxx1 enables forwarding from FPD Port0. xx1x enables forwarding from FPD Port1. x1xx enables forwarding from FPD Port2. 1xxx enables forwarding from FPD Port3.
3-0	CSI0_EXCLUSIVE_FWD	R/W	0xF	Exclusive Forward Mask for CSI Port 0 When EXCLUSIVE_FWD_EN is set to 1, this value determines which Receive Ports will be forwarded to CSI Transmit port 0. A value of 1 in the bit will enable forwarding. xxx1 enables forwarding from FPD Port0. xx1x enables forwarding from FPD Port1. x1xx enables forwarding from FPD Port2. 1xxx enables forwarding from FPD Port3.

8.6.1.61 CSI_EXCLUSIVE_FWD2 Register (Address = 0x3C) [Default = 0x3F]

CSI_EXCLUSIVE_FWD2 is shown in [CSI_EXCLUSIVE_FWD2 Register Field Descriptions](#).

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Table 8-80. CSI_EXCLUSIVE_FWD2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	EXCLUSIVE_FWD_EN	R/W	0x0	Exclusive Forwarding Enable Setting this bit to a 1 enables Exclusive Forwarding mode Note that FWD_CTL1[3:0] must be set to 0 for the registers in 0x3B to take effect
6	REPLICATE_CSI2_SEL	R/W	0x0	Replicate Selection for CSI-2 Transmit Port 2 When CSI-2 Transmit port 2 is enabled via the CSI_PORT2_ENABLE register control, this register enables which CSI Transmit port is replicated to CSI-2 Transmit Port 2. 0: Select CSI TX Port 0 for replication 1: Select CSI TX Port 1 for replication
5-4	FPD4_AUTO_RECOVER	R/W	0x3	FPD4 Auto Recover: 00= Disable 01= FPD4 auto recover mechanism 10= RESERVED 11= RESERVED
3	RESERVED	R/W	0x1	Reserved
2-0	RESERVED	R/W	0x7	Reserved

8.6.1.62 REFCLK_FREQ Register (Address = 0x3D) [Default = 0x19]REFCLK_FREQ is shown in [REFCLK_FREQ Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-81. REFCLK_FREQ Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	REFCLK_FREQ	R	0x19	REFCLK frequency measurement in MHz.

8.6.1.63 BC_CTRL Register (Address = 0x3E) [Default = 0x00]BC_CTRL is shown in [BC_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-82. BC_CTRL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FPD4_BCDATA_P3	R/W	0x0	Enable BC data with 8b10 encode
6	FPD4_BCDATA_P2	R/W	0x0	Enable BC data with 8b10 encode
5	FPD4_BCDATA_P1	R/W	0x0	Enable BC data with 8b10 encode
4	FPD4_BCDATA_P0	R/W	0x0	Enable BC data with 8b10 encode
3	GPIO_SEQ_EN_P3	R/W	0x0	Enable sending sequence number on GPIOs 1-3
2	GPIO_SEQ_EN_P2	R/W	0x0	Enable sending sequence number on GPIOs 1-3
1	GPIO_SEQ_EN_P1	R/W	0x0	Enable sending sequence number on GPIOs 1-3
0	GPIO_SEQ_EN_P0	R/W	0x0	Enable sending sequence number on GPIOs 1-3

8.6.1.64 BCC_ERR_CTL Register (Address = 0x46) [Default = 0x00]BCC_ERR_CTL is shown in [BCC_ERR_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-83. BCC_ERR_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Deserializer to generate an internal acknowledge to the beginning of a remote I2C slave read. This allows additional error detection at the Serializer. This bit should not be set when operating with Serializers that do not support Enhanced Error Checking. 0: Disable 1: Enable
6	BCC_EN_DATA_CHK	R/W	0x0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Serializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0: Disable returned data error detection 1: Enable returned data error detection

Table 8-83. BCC_ERR_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	BCC_EN_ENH_ERROR	R/W	0x0	Enable Enhanced Error checking in Bidirection Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0: Disable Enhanced Error checking 1: Enable Enhanced Error checking
4-3	FORCE_BCC_ERROR	R/W	0x0	BCC Force Error The BCC Force Error control causes an error to be forced on the BCC over the back channel. 00: No error 01: Force CRC Error on BCC frame= BCC_FRAME_SEL 10: Force CRC Error on normal frame following BCC frame= BCC_FRAME_SEL 11: FORCE Data Error on BCC frame= BCC_FRAME_SEL Setting this control generates a single error on the back channel signaling.
2-0	BCC_FRAME_SEL	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

8.6.1.65 BCC_STATUS Register (Address = 0x47) [Default = 0x00]BCC_STATUS is shown in [BCC_STATUS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-84. BCC_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	
5	BCC_SEQ_ERROR	RC	0x0	Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. If BCC_EN_ENH_ERR is 0 (disabled), this register is read-only copy of the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is cleared on read of this register.
4	BCC_MASTER_ERR	RC	0x0	BCC Master Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Master is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
3	BCC_MASTER_TO	RC	0x0	BCC Slave Timeout Error This bit will be set if the BCC Watchdog Timer expires while waiting for a response from the Serializer while the BCC I2C Master is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
2	BCC_SLAVE_ERR	RC	0x0	BCC Slave Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Slave is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

Table 8-84. BCC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	BCC_SLAVE_TO	RC	0x0	BCC Slave Timeout Error This bit will be set if the BCC Watchdog Timer expires while waiting for a response from the Serializer while the BCC I2C Slave is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
0	BCC_RESP_ERR	RC	0x0	BCC Response Error This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the I2C Slave is active, the Serializer should return data written (I2C address, offset, or data). When the I2C Slave is active, the Serializer should return data read. The BCC function checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

8.6.1.66 RAW_EMBED_DTYPE Register (Address = 0x4B) [Default = 0x12]RAW_EMBED_DTYPE is shown in [RAW_EMBED_DTYPE Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-85. RAW_EMBED_DTYPE Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	EMBED_DTYPE_EN	R/W	0x0	Embedded Data Type Enable When the receiver is programmed for Raw mode data, this register field allows setting the Data Type field for the first N lines to indicated embedded non-image data. 0: All long packets will be forwarded as RAW10 or RAW12 video data 1-3: Send first N long packets (1, 2, or 3) as Embedded data using the data type in the EMBED_DTYPE_ID field of this register. This control has no effect if the Receiver is programmed to receive CSI formatted data.
5-0	EMBED_DTYPE_ID	R/W	0x12	Embedded Data Type If sending embedded data is enabled via the EMBED_DTYPE_EN control in this register, the Data Type field for the first N lines of each frame will use this value rather than the value programmed in the RAW12_ID or RAW10_ID registers. The default setting matches the CSI-2 specification for Embedded 8-bit non Image Data.

8.6.1.67 FPD3_PORT_SEL Register (Address = 0x4C) [Default = 0x00]FPD3_PORT_SEL is shown in [FPD3_PORT_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-86. FPD3_PORT_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	PHYS_PORT_NUM	R	0x0	Physical port number This field provides the physical port connection when reading from a remote device via the Bidirectional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bidirectional Control Channel, the value returned is the port number of the Receive port connection.

Table 8-86. FPD3_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-4	RX_READ_PORT	R/W	0x0	Select RX port for register read This field selects one of the four RX port register blocks for readback. This applies to all paged FPD Receiver port registers. 00: Port 0 registers 01: Port 1 registers 10: Port 2 registers 11: Port 3 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bidirectional Control Channel, the default value is the port number of the Receive port connection.
3	RX_WRITE_PORT_3	R/W	0x0	Write Enable for RX port 3 registers This bit enables writes to RX port 3 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 3. 1 for RX Port 3
2	RX_WRITE_PORT_2	R/W	0x0	Write Enable for RX port 2 registers This bit enables writes to RX port 2 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 2. 1 for RX Port 2
1	RX_WRITE_PORT_1	R/W	0x0	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 1. 1 for RX Port 1
0	RX_WRITE_PORT_0	R/W	0x0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 0. 1 for Rx Port 0

8.6.1.68 RX_PORT_STS1 Register (Address = 0x4D) [Default = 0x00]RX_PORT_STS1 is shown in [RX_PORT_STS1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-87. RX_PORT_STS1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RX_PORT_NUM	R	0x0	RX Port Number This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	RC	0x0	Bidirectional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.

Table 8-87. RX_PORT_STS1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LOCK_STS_CHG	RC	0x0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.
3	BCC_SEQ_ERROR/ BCC_ERROR	RC	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: Bidirectional Control Channel Error Flag This flag indicates one or more errors have been detected during Bidirectional Control Channel communication with the Deserializer. The BCC_STATUS register contains further information on the type of error detected. This bit will be cleared upon read of the BCC_STATUS register.
2	PARITY_ERROR	R	0x0	FPD parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THRESH registers. 1: Number of FPD parity errors detected is greater than the threshold 0: Number of FPD parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
1	PORT_PASS	R	0x0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
0	LOCK_STS	R	0x0	FPD-Link receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

8.6.1.69 RX_PORT_STS2 Register (Address = 0x4E) [Default = 0x00]RX_PORT_STS2 is shown in [RX_PORT_STS2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-88. RX_PORT_STS2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_LEN_UNSTABLE	RC	0x0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
6	LINE_LEN_CHG	RC	0x0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.

Table 8-88. RX_PORT_STS2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	FPD_ENCODE_ERROR	RC	0x0	FPD Encoder error detected If set, this flag indicates an error in the FPD-Link encoding has been detected by the FPD-Link receiver. This bit is cleared on read. Note, to detect FPD Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.
4	BUFFER_ERROR	RC	0x0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
3	CSI_ERROR	R	0x0	CSI Receive error detected See the CSI_RX_STS register for details.
2	FPD_FREQ_STABLE	R	0x0	FPD Frequency measurement stable Indicates the FPD input clock frequency is stable. Setting of this flag is dependent on the stability control settings in the FREQ_DET_CTL register. This field is not applicable to FPD4 operation
1	NO_FPD_CLK	R	0x0	No FPD-Link input clock detected When set, this bit indicates that no FPD Clock has been detected. This bit will be set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register. This field is not applicable to FPD4 operation
0	LINE_CNT_CHG	RC	0x0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

8.6.1.70 RX_FREQ_HIGH Register (Address = 0x4F) [Default = 0x00]RX_FREQ_HIGH is shown in [RX_FREQ_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-89. RX_FREQ_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FREQ_CNT_HIGH	R	0x0	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD Receiver. This portion of the field is the integer value in MHz. Frequency measurements will scale with reference clock frequency. This field is not applicable to FPD4 operation

8.6.1.71 RX_FREQ_LOW Register (Address = 0x50) [Default = 0x00]RX_FREQ_LOW is shown in [RX_FREQ_LOW Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-90. RX_FREQ_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FREQ_CNT_LOW	R	0x0	Frequency Counter Low Byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD Receiver. This portion of the field is the fractional value in 1/256 MHz. Frequency measurements will scale with reference clock frequency. This field is not applicable to FPD4 operation

8.6.1.72 SENSOR_STS_0 Register (Address = 0x51) [Default = 0x00]SENSOR_STS_0 is shown in [SENSOR_STS_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-91. SENSOR_STS_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SENSOR_STS_0	R	0x0	Sensor Status Register 0 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

8.6.1.73 SENSOR_STS_1 Register (Address = 0x52) [Default = 0x00]SENSOR_STS_1 is shown in [SENSOR_STS_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-92. SENSOR_STS_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SENSOR_STS_1	R	0x0	Sensor Status Register 1 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

8.6.1.74 SENSOR_STS_2 Register (Address = 0x53) [Default = 0x00]SENSOR_STS_2 is shown in [SENSOR_STS_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-93. SENSOR_STS_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SENSOR_STS_2	R	0x0	Sensor Status Register 2 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

8.6.1.75 SENSOR_STS_3 Register (Address = 0x54) [Default = 0x00]SENSOR_STS_3 is shown in [SENSOR_STS_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-94. SENSOR_STS_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SENSOR_STS_3	R	0x0	Sensor Status Register 3 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

8.6.1.76 RX_PAR_ERR_HI Register (Address = 0x55) [Default = 0x00]RX_PAR_ERR_HI is shown in [RX_PAR_ERR_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-95. RX_PAR_ERR_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PAR_ERROR_BYTE_1	R	0x0	Number of FPD3 parity errors – 8 most significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register will be cleared upon reading the RX_PAR_ERR_LO register.

8.6.1.77 RX_PAR_ERR_LO Register (Address = 0x56) [Default = 0x00]RX_PAR_ERR_LO is shown in [RX_PAR_ERR_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-96. RX_PAR_ERR_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PAR_ERROR_BYTE_0	RC	0x0	Number of FPD3 parity errors – 8 least significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register will be cleared on read.

8.6.1.78 BIST_ERR_COUNT Register (Address = 0x57) [Default = 0x00]BIST_ERR_COUNT is shown in [BIST_ERR_COUNT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-97. BIST_ERR_COUNT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	BIST_ERROR_COUNT	R	0x0	Bist Error Count Returns BIST error count

8.6.1.79 BCC_CONFIG Register (Address = 0x58) [Default = 0x1E]BCC_CONFIG is shown in [BCC_CONFIG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-98. BCC_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	I2C_PASS_THROUGH_A_LL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled

Table 8-98. BCC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	AUTO_ACK_ALL	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	BC_ALWAYS_ON	R/W	0x1	Back channel enable Strap 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit may only be written via a local I2C master. At power-up, this field is set based on the MODE pin strap value.
3	BC_CRC_GEN_ENABLE	R/W	0x1	Back Channel CRC Generator Enable 0: Disable 1: Enable
2-0	BC_FREQ_SELECT	R/W	0x6	Back Channel Frequency Select Strap 000: 2.5 Mbps (default for DS90UB913 compatibility) 001: Reserved 010: 10 Mbps 011: Reserved 100: Reserved 101: 25 Mbps 110: 50 Mbps (default for DS90UB953 compatibility) 111: Reserved Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Deserializer should first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Serializer.

8.6.1.80 DATAPATH_CTL1 Register (Address = 0x59) [Default = 0x00]

DATAPATH_CTL1 is shown in [DATAPATH_CTL1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-99. DATAPATH_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	1: Disable loading of the DATAPATH_CTL registers from the forward channel, keeping locally written values intact 0: Allow forward channel loading of DATAPATH_CTL registers
6-2	RESERVED	R/W	0x0	Reserved
1-0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs This field is normally loaded from the remote serializer. It can be overwritten if the OVERRIDE_FC_CONFIG bit in this register is 1.

8.6.1.81 SER_ID Register (Address = 0x5B) [Default = 0x00]

SER_ID is shown in [SER_ID Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-100. SER_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	SER_ID	R/W	0x0	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.

8.6.1.82 SER_ALIAS_ID Register (Address = 0x5C) [Default = 0x00]SER_ALIAS_ID is shown in [SER_ALIAS_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-101. SER_ALIAS_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SER_ALIAS_ID	R/W	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
0	SER_AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.83 SLAVE_ID_0 Register (Address = 0x5D) [Default = 0x00]SLAVE_ID_0 is shown in [SLAVE_ID_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-102. SLAVE_ID_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID0	R/W	0x0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.84 SLAVE_ID_1 Register (Address = 0x5E) [Default = 0x00]SLAVE_ID_1 is shown in [SLAVE_ID_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-103. SLAVE_ID_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID1	R/W	0x0	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

Table 8-103. SLAVE_ID_1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RESERVED	R	0x0	Reserved.

8.6.1.85 SLAVE_ID_2 Register (Address = 0x5F) [Default = 0x00]SLAVE_ID_2 is shown in [SLAVE_ID_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-104. SLAVE_ID_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID2	R/W	0x0	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.86 SLAVE_ID_3 Register (Address = 0x60) [Default = 0x00]SLAVE_ID_3 is shown in [SLAVE_ID_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-105. SLAVE_ID_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID3	R/W	0x0	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.87 SLAVE_ID_4 Register (Address = 0x61) [Default = 0x00]SLAVE_ID_4 is shown in [SLAVE_ID_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-106. SLAVE_ID_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID4	R/W	0x0	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.88 SLAVE_ID_5 Register (Address = 0x62) [Default = 0x00]SLAVE_ID_5 is shown in [SLAVE_ID_5 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-107. SLAVE_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	SLAVE_ID5	R/W	0x0	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.89 SLAVE_ID_6 Register (Address = 0x63) [Default = 0x00]SLAVE_ID_6 is shown in [SLAVE_ID_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-108. SLAVE_ID_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID6	R/W	0x0	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.90 SLAVE_ID_7 Register (Address = 0x64) [Default = 0x00]SLAVE_ID_7 is shown in [SLAVE_ID_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-109. SLAVE_ID_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ID7	R/W	0x0	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

8.6.1.91 SLAVE_ALIAS_0 Register (Address = 0x65) [Default = 0x00]SLAVE_ALIAS_0 is shown in [SLAVE_ALIAS_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-110. SLAVE_ALIAS_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID0	R/W	0x0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.

Table 8-110. SLAVE_ALIAS_0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	SLAVE_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.92 SLAVE_ALIAS_1 Register (Address = 0x66) [Default = 0x00]SLAVE_ALIAS_1 is shown in [SLAVE_ALIAS_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-111. SLAVE_ALIAS_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID1	R/W	0x0	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.93 SLAVE_ALIAS_2 Register (Address = 0x67) [Default = 0x00]SLAVE_ALIAS_2 is shown in [SLAVE_ALIAS_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-112. SLAVE_ALIAS_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID2	R/W	0x0	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.94 SLAVE_ALIAS_3 Register (Address = 0x68) [Default = 0x00]SLAVE_ALIAS_3 is shown in [SLAVE_ALIAS_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-113. SLAVE_ALIAS_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID3	R/W	0x0	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.

Table 8-113. SLAVE_ALIAS_3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	SLAVE_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.95 SLAVE_ALIAS_4 Register (Address = 0x69) [Default = 0x00]SLAVE_ALIAS_4 is shown in [SLAVE_ALIAS_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-114. SLAVE_ALIAS_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID4	R/W	0x0	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.96 SLAVE_ALIAS_5 Register (Address = 0x6A) [Default = 0x00]SLAVE_ALIAS_5 is shown in [SLAVE_ALIAS_5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-115. SLAVE_ALIAS_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID5	R/W	0x0	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.97 SLAVE_ALIAS_6 Register (Address = 0x6B) [Default = 0x00]SLAVE_ALIAS_6 is shown in [SLAVE_ALIAS_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-116. SLAVE_ALIAS_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID6	R/W	0x0	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.

Table 8-116. SLAVE_ALIAS_6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	SLAVE_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.98 SLAVE_ALIAS_7 Register (Address = 0x6C) [Default = 0x00]SLAVE_ALIAS_7 is shown in [SLAVE_ALIAS_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-117. SLAVE_ALIAS_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	SLAVE_ALIAS_ID7	R/W	0x0	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	SLAVE_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Slave 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

8.6.1.99 PORT_CONFIG Register (Address = 0x6D) [Default = 0x78]PORT_CONFIG is shown in [PORT_CONFIG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-118. PORT_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CSI_WAIT_FS1	R/W	0x0	CSI Wait for FrameStart packet with count 1 The CSI Receiver will wait for a Frame Start packet with count of 1 before accepting other packets This bit has no effect in RAW FPD3 input modes.
6	CSI_WAIT_FS	R/W	0x1	CSI Wait for FrameStart packet CSI2 Receiver will wait for a Frame Start packet before accepting other packets This bit has no effect in RAW FPD3 input modes.
5	CSI_FWD_CKSUM	R/W	0x1	Forward CSI packets with checksum errors 0: Do not forward errored packets 1: Forward errored packets This bit has no effect in RAW FPD3 input modes.
4	CSI_FWD_ECC	R/W	0x1	Forward CSI packets with ECC errors 0: Do not forward errored packets 1: Forward errored packets
3	CSI_FWD_LEN	R/W	0x1	In FPD3 RAW Mode, Discard first video line if FV to LV setup time is not met. 0: Forward truncated 1st video line 1: Discard truncated 1st video line In FPD3 CSI Mode, Forward CSI packets with length errors 0: Do not forward errored packets 1: Forward errored packets
2-0	RESERVED	R	0x0	Reserved

8.6.1.100 BC_GPIO_CTL0 Register (Address = 0x6E) [Default = 0x88]BC_GPIO_CTL0 is shown in [BC_GPIO_CTL0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-119. BC_GPIO_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	BC_GPIO1_SEL	R/W	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3-0	BC_GPIO0_SEL	R/W	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO0_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

8.6.1.101 BC_GPIO_CTL1 Register (Address = 0x6F) [Default = 0x88]BC_GPIO_CTL1 is shown in [BC_GPIO_CTL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-120. BC_GPIO_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	BC_GPIO3_SEL	R/W	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO3_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3-0	BC_GPIO2_SEL	R/W	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO2_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

8.6.1.102 RAW10_ID Register (Address = 0x70) [Default = 0x2B]RAW10_ID is shown in [RAW10_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-121. RAW10_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RAW10_VC	R/W	0x0	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number
5-0	RAW10_ID	R/W	0x2B	RAW10 ID This field configures the CSI data type used in RAW10 mode. The default of 0x2B matches the CSI specification.

8.6.1.103 RAW12_ID Register (Address = 0x71) [Default = 0x2C]

RAW12_ID is shown in [RAW12_ID Register Field Descriptions](#).

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Table 8-122. RAW12_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RAW12_VC	R/W	0x0	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number
5-0	RAW12_ID	R/W	0x2C	RAW12 ID This field configures the CSI data type used in RAW12 mode. The default of 0x2C matches the CSI specification.

8.6.1.104 LINE_COUNT_1 Register (Address = 0x73) [Default = 0x00]

LINE_COUNT_1 is shown in [LINE_COUNT_1 Register Field Descriptions](#).

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Table 8-123. LINE_COUNT_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value will be frozen until read.

8.6.1.105 LINE_COUNT_0 Register (Address = 0x74) [Default = 0x00]

LINE_COUNT_0 is shown in [LINE_COUNT_0 Register Field Descriptions](#).

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Table 8-124. LINE_COUNT_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value will be frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO will be latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

8.6.1.106 LINE_LEN_1 Register (Address = 0x75) [Default = 0x00]

LINE_LEN_1 is shown in [LINE_LEN_1 Register Field Descriptions](#).

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Table 8-125. LINE_LEN_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_LEN_HI	R	0x0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value will be frozen until read.

8.6.1.107 LINE_LEN_0 Register (Address = 0x76) [Default = 0x00]LINE_LEN_0 is shown in [LINE_LEN_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-126. LINE_LEN_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_LEN_LO	R	0x0	Low byte of Line Length The Line Length reports the length of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value will be frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO will be latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

8.6.1.108 FPD3_FREQ_DET_CTL Register (Address = 0x77) [Default = 0xC5]FPD3_FREQ_DET_CTL is shown in [FPD3_FREQ_DET_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-127. FPD3_FREQ_DET_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	FREQ_HYST	R/W	0x3	FPD3 Frequency Detect Hysteresis: The Frequency detect hysteresis controls reporting of the FPD3 Clock frequency stability via the FREQ_STABLE status in the RX_PORT_STS2 register. The frequency is considered stable when the frequency remains within a range of +/- the FREQ_HYST value from the previous measurement. The FREQ_HYST setting is in MHz. This field is not applicable to FPD4 operation
5-4	FREQ_STABLE_THR	R/W	0x0	FPD3 Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00: 40us 01: 80us 10: 320us 11: 1.28ms This field is not applicable to FPD4 operation
3-0	FREQ_LO THR	R/W	0x5	FPD3 Frequency Low Threshold: Sets the low threshold for the Clock frequency detect circuit in MHz. If the input clock is below this threshold, the NO_FPD3_CLK status will be set to 1. This field is not applicable to FPD4 operation

8.6.1.109 MAILBOX_1 Register (Address = 0x78) [Default = 0x00]MAILBOX_1 is shown in [MAILBOX_1 Register Field Descriptions](#).

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Table 8-128. MAILBOX_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	MAILBOX_0	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

8.6.1.110 MAILBOX_2 Register (Address = 0x79) [Default = 0x01]

MAILBOX_2 is shown in [MAILBOX_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-129. MAILBOX_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	MAILBOX_1	R/W	0x1	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

8.6.1.111 CSI_RX_STS Register (Address = 0x7A) [Default = 0x00]

CSI_RX_STS is shown in [CSI_RX_STS Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-130. CSI_RX_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0x0	Reserved
3	LENGTH_ERR	RC	0x0	Packet Length Error detected for received CSI packet If set, this bit indicates a packet length error was detected on at least one CSI packet received from the camera. Packet length errors occur if the data length field in the packet header does not match the actual data length for the packet. 1: One or more Packet Length errors have been detected 0: No Packet Length errors have been detected This bit is cleared on read.
2	CKSUM_ERR	RC	0x0	Data Checksum Error detected for received CSI packet If set, this bit indicates a data checksum error was detected on at least one CSI packet received from the camera. Data checksum errors indicate an error was detected in the packet data portion of the CSI packet. 1: One or more Data Checksum errors have been detected 0: No Data Checksum errors have been detected This bit is cleared on read.
1	ECC2_ERR	RC	0x0	2-bit ECC Error detected for received CSI packet If set, this bit indicates a multi-bit ECC error was detected on at least one CSI packet received from the camera. Multi-bit errors are not corrected by the device. 1: One or more multi-bit ECC errors have been detected 0: No multi-bit ECC errors have been detected This bit is cleared on read.

Table 8-130. CSI_RX_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	ECC1_ERR	RC	0x0	1-bit ECC Error detected for received CSI packet If set, this bit indicates a single-bit ECC error was detected on at least one CSI packet received from the camera. Single-bit errors are corrected by the device. 1: One or more 1-bit ECC errors have been detected 0: No 1-bit ECC errors have been detected This bit is cleared on read.

8.6.1.112 CSI_ERR_COUNTER Register (Address = 0x7B) [Default = 0x00]CSI_ERR_COUNTER is shown in [CSI_ERR_COUNTER Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-131. CSI_ERR_COUNTER Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_ERR_CNT	RC	0x0	CSI Error Counter Register This register counts the number of CSI packets received with errors since the last read of the counter.

8.6.1.113 PORT_CONFIG2 Register (Address = 0x7C) [Default = 0x20]PORT_CONFIG2 is shown in [PORT_CONFIG2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-132. PORT_CONFIG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data will be processed as 8-bit data and packed accordingly for transmission over CSI. 00: Normal Raw10 Mode 01: Reserved 10: 8-bit processing using upper 8 bits 11: 8-bit processing using lower 8 bits
5	DISCARD_ON_PAR_ERR	R/W	0x1	Discard frames on Parity Error 0: Forward packets with parity errors 1: Truncate Frames if a parity error is detected
4	DISCARD_ON_LINE_SIZE	R/W	0x0	Discard frames on Line Size 0: Allow changes in Line Size within packets 1: Truncate Frames if a change in line size is detected
3	DISCARD_ON_FRAME_SIZE	R/W	0x0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0: Allow changes in Frame Size 1: Truncate Frames if a change in frame size is detected
2	RESERVED	R	0x0	Reserved
1	LV_POLARITY	R/W	0x0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1: LineValid is low for the duration of the video line 0: LineValid is high for the duration of the video line This bit is ignored if AUTO_POLARITY is set.

Table 8-132. PORT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	FV_POLARITY	R/W	0x0	<p>FrameValid Polarity</p> <p>This register indicates the expected polarity for the FrameValid indication received in Raw mode.</p> <p>1: FrameValid is low for the duration of the video frame</p> <p>0: FrameValid is high for the duration of the video frame</p> <p>This bit is ignored if AUTO_POLARITY is set.</p>

8.6.1.114 PORT_PASS_CTL Register (Address = 0x7D) [Default = 0x00]PORT_PASS_CTL is shown in [PORT_PASS_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-133. PORT_PASS_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PASS_DISCARD_EN	R/W	0x0	<p>Pass Discard Enable</p> <p>Discard packets if PASS is not indicated.</p> <p>0: Ignore PASS for forwarding packets</p> <p>1: Discard packets when PASS is not true</p>
6	PASS_CLEAR_CNT	R/W	0x0	<p>This bit controls the values read back from the LINE_COUNT_1, LINE_COUNT_0, LINE_LEN_1, and LINE_LEN_0 registers.</p> <p>0: Registers read back the counter values regardless of the state of the PASS flag</p> <p>1: Registers read back zero when the PASS flag is de-asserted and the count values when PASS is asserted</p>
5	PASS_LINE_CNT	R/W	0x0	<p>Pass Line Count Control</p> <p>This register controls whether the device will include line count in qualification of the Pass indication:</p> <p>0: Don't check line count</p> <p>1: Check line count</p> <p>When checking line count, Pass will be deasserted upon detection of a change in the number of video lines per frame. Pass will not be reasserted until the PASS_THRESHOLD setting is met.</p>
4	PASS_LINE_SIZE	R/W	0x0	<p>Pass Line Size Control</p> <p>This register controls whether the device will include line size in qualification of the Pass indication:</p> <p>0: Don't check line size</p> <p>1: Check line size</p> <p>When checking line size, Pass will be deasserted upon detection of a change in video line size. Pass will not be reasserted until the PASS_THRESHOLD setting is met.</p>
3	PASS_PARITY_ERR	R/W	0x0	<p>Parity Error Mode</p> <p>If this bit is set to 0, the port Pass indication will be deasserted for every parity error detected on the FPD3 Receive interface. If this bit is set to a 1, the port Pass indication will be cleared on a parity error and remain clear until the PASS_THRESHOLD is met.</p>
2	PASS_WDOG_DIS	R/W	0x0	<p>RX Port Pass Watchdog disable</p> <p>When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication will be deasserted. The watchdog timer will not have any effect if the PASS_THRESHOLD is set to 0.</p> <p>0: Enable watchdog timer for RX Pass</p> <p>1: Disable watchdog timer for RX Pass</p>
1-0	PASS_THRESHOLD	R/W	0x0	<p>Pass Threshold Register</p> <p>This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS will be asserted after Receiver Lock detect. If non-zero, PASS will be asserted following reception of the programmed number of valid frames.</p>

8.6.1.115 SEN_INT_RISE_CTL Register (Address = 0x7E) [Default = 0x00]SEN_INT_RISE_CTL is shown in [SEN_INT_RISE_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-134. SEN_INT_RISE_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SEN_INT_RISE_MASK	R/W	0x0	Sensor Interrupt Rise Mask This register provides the interrupt mask for detecting rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_RISE_STS register.

8.6.1.116 SEN_INT_FALL_CTL Register (Address = 0x7F) [Default = 0x00]SEN_INT_FALL_CTL is shown in [SEN_INT_FALL_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-135. SEN_INT_FALL_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SEN_INT_FALL_MASK	R/W	0x0	Sensor Interrupt Fall Mask This register provides the interrupt mask for detecting falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_FALL_STS register.

8.6.1.117 FFD_CTL Register (Address = 0x88) [Default = 0x01]FFD_CTL is shown in [FFD_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-136. FFD_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	RESERVED
5-4	PRWS_SELECT	R/W	0x0	00: Legacy 01: Mode1 10: Mode2 11: Mode3
3	FRAMEFREEZE_USE_CRC	R/W	0x0	0: check frame number to detect frame freeze; 1: check CRC for video lines to detect frame freeze.
2-0	FRAMEFREEZE_THRESHOLD	R/W	0x1	Frame Freeze Detection Threshold 3'h0: detect 2 frames are frozen; 3'h1: detect 4 frames are frozen; 3'h2: detect 8 frames are frozen; 3'h3: detect 16 frames are frozen; 3'h4: detect 32 frames are frozen; 3'h5: detect 64 frames are frozen; 3'h6: detect 128 frames are frozen; 3'h7: detect 256 frames are frozen.

8.6.1.118 GPIO9_PIN_CTL Register (Address = 0x89) [Default = 0x00]GPIO9_PIN_CTL is shown in [GPIO9_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-137. GPIO9_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO9_OUT_SEL	R/W	0x0	<p>GPIO9 Output Select Determines the output data for the selected source. If GPIO9_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal <p>If GPIO9_OUT_SRC is set to 100 (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> 000: Value in GPIO9_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk <p>If GPIO9_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply:</p> <ul style="list-style-type: none"> 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4-2	GPIO0_OUT_SRC	R/W	0x0	<p>GPIO9 Output Source Select Selects output source for GPIO0 data:</p> <ul style="list-style-type: none"> 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO9_OUT_VAL	R/W	0x0	<p>GPIO9 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO9_OUT_EN	R/W	0x0	<p>GPIO9 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.119 GPIO10_PIN_CTL Register (Address = 0x8A) [Default = 0x00]GPIO10_PIN_CTL is shown in [GPIO10_PIN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-138. GPIO10_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	GPIO10_OUT_SEL	R/W	0x0	<p>GPIO10 Output Select Determines the output data for the selected source. If GPIO10_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO10_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO10_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO10_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved</p>
4-2	GPIO10_OUT_SRC	R/W	0x0	<p>GPIO10 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1</p>
1	GPIO10_OUT_VAL	R/W	0x0	<p>GPIO10 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.</p>
0	GPIO10_OUT_EN	R/W	0x0	<p>GPIO10 Output Enable 0: Disabled 1: Enabled</p>

8.6.1.120 GPIO_INPUT_CTL_2 Register (Address = 0x8B) [Default = 0x04]GPIO_INPUT_CTL_2 is shown in [GPIO_INPUT_CTL_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-139. GPIO_INPUT_CTL_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved

Table 8-139. GPIO_INPUT_CTL_2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	INTB_PAD_EN	R/W	0x1	1: Enables INTB in Open Drain for GPIO3 pin 0: GPIO3 pin is controlled by GPIO3_PIN_CTL
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.1.121 REFCLK_DET_INT_CTL Register (Address = 0x8C) [Default = 0x00]REFCLK_DET_INT_CTL is shown in [REFCLK_DET_INT_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-140. REFCLK_DET_INT_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-3	RESERVED	R	0x0	
2	REFCLK_NOT_IMMEDIATE	R/W	0x0	REFCLK not detected immediate interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is NOT detected as indicated by the REFCLK_VALID register status equal to 0. This control allows constant interrupt generation as long as the event is true. As long as the REFCLK_VALID=0, this will cause an interrupt. While REFCLK_VALID=0, the only way to clear this interrupt condition is to clear this bit. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register
1	REFCLK_LOST_INT	R/W	0x0	REFCLK lost interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is NOT detected as indicated by the REFCLK_VALID register status changing from 1 to 0. This enable allows detecting the loss of REFCLK_VALID rather than the steady-state condition. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register
0	REFCLK_DET_INT	R/W	0x0	REFCLK detect interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is detected as indicated by the REFCLK_VALID register status. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register

8.6.1.122 CSI0_FRAME_COUNT_HI Register (Address = 0x90) [Default = 0x00]CSI0_FRAME_COUNT_HI is shown in [CSI0_FRAME_COUNT_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-141. CSI0_FRAME_COUNT_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI0_FRAME_COUNT_HI	RC	0x0	CSI Port 0, Frame Counter MSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_FRAME_COUNT. The LSBs of the counter are sampled into the CSI0_FRAME_COUNT_LO register and the counter is cleared.

8.6.1.123 CSI0_FRAME_COUNT_LO Register (Address = 0x91) [Default = 0x00]CSI0_FRAME_COUNT_LO is shown in [CSI0_FRAME_COUNT_LO Register Field Descriptions](#).

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Table 8-142. CSI0_FRAME_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI0_FRAME_COUNT_LO	R	0x0	CSI Port 0, Frame Counter LSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_FRAME_COUNT. The CSI0_FRAME_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.124 CSI0_FRAME_ERR_COUNT_HI Register (Address = 0x92) [Default = 0x00]

CSI0_FRAME_ERR_COUNT_HI is shown in [CSI0_FRAME_ERR_COUNT_HI Register Field Descriptions](#).

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Table 8-143. CSI0_FRAME_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI0_FRAME_ERR_CO NT_HI	RC	0x0	CSI Port 0, Frame Counter with Errors MSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_FRAME_ERR_COUNT. The LSBs of the counter are sampled into the CSI0_FRAME_ERR_COUNT_LO register and the counter is cleared.

8.6.1.125 CSI0_FRAME_ERR_COUNT_LO Register (Address = 0x93) [Default = 0x00]

CSI0_FRAME_ERR_COUNT_LO is shown in [CSI0_FRAME_ERR_COUNT_LO Register Field Descriptions](#).

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Table 8-144. CSI0_FRAME_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI0_FRAME_ERR_CO NT_LO	R	0x0	CSI Port 0, Frame Counter with Errors LSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_FRAME_ERR_COUNT. The CSI0_FRAME_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.126 CSI0_LINE_COUNT_HI Register (Address = 0x94) [Default = 0x00]

CSI0_LINE_COUNT_HI is shown in [CSI0_LINE_COUNT_HI Register Field Descriptions](#).

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Table 8-145. CSI0_LINE_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI0_LINE_COUNT_HI	RC	0x0	CSI Port 0, Line Counter MSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_LINE_COUNT. The LSBs of the counter are sampled into the CSI0_LINE_COUNT_LO register and the counter is cleared.

8.6.1.127 CSI0_LINE_COUNT_LO Register (Address = 0x95) [Default = 0x00]CSI0_LINE_COUNT_LO is shown in [CSI0_LINE_COUNT_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-146. CSI0_LINE_COUNT_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI0_LINE_COUNT_LO	R	0x0	CSI Port 0, Line Counter LSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_LINE_COUNT. The CSI0_LINE_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.128 CSI0_LINE_ERR_COUNT_HI Register (Address = 0x96) [Default = 0x00]CSI0_LINE_ERR_COUNT_HI is shown in [CSI0_LINE_ERR_COUNT_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-147. CSI0_LINE_ERR_COUNT_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI0_LINE_ERR_COUNT_HI	RC	0x0	CSI Port 0, Line Counter with Errors MSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_LINE_ERR_COUNT. The LSBs of the counter are sampled into the CSI0_LINE_ERR_COUNT_LO register and the counter is cleared.

8.6.1.129 CSI0_LINE_ERR_COUNT_LO Register (Address = 0x97) [Default = 0x00]CSI0_LINE_ERR_COUNT_LO is shown in [CSI0_LINE_ERR_COUNT_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-148. CSI0_LINE_ERR_COUNT_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI0_LINE_ERR_COUNT_LO	R	0x0	CSI Port 0, Line Counter with Errors LSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_LINE_ERR_COUNT. The CSI0_LINE_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.130 CSI1_FRAME_COUNT_HI Register (Address = 0x98) [Default = 0x00]CSI1_FRAME_COUNT_HI is shown in [CSI1_FRAME_COUNT_HI Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-149. CSI1_FRAME_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI1_FRAME_COUNT_HI	RC	0x0	CSI Port 1, Frame Counter MSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_FRAME_COUNT. The LSBs of the counter are sampled into the CSI1_FRAME_COUNT_LO register and the counter is cleared.

8.6.1.131 CSI1_FRAME_COUNT_LO Register (Address = 0x99) [Default = 0x00]CSI1_FRAME_COUNT_LO is shown in [CSI1_FRAME_COUNT_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-150. CSI1_FRAME_COUNT_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI1_FRAME_COUNT_LO	R	0x0	CSI Port 1, Frame Counter LSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_FRAME_COUNT. The CSI1_FRAME_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.132 CSI1_FRAME_ERR_COUNT_HI Register (Address = 0x9A) [Default = 0x00]CSI1_FRAME_ERR_COUNT_HI is shown in [CSI1_FRAME_ERR_COUNT_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-151. CSI1_FRAME_ERR_COUNT_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI1_FRAME_ERR_COUNT_HI	RC	0x0	CSI Port 1, Frame Counter with Errors MSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_FRAME_ERR_COUNT. The LSBs of the counter are sampled into the CSI1_FRAME_ERR_COUNT_LO register and the counter is cleared.

8.6.1.133 CSI1_FRAME_ERR_COUNT_LO Register (Address = 0x9B) [Default = 0x00]CSI1_FRAME_ERR_COUNT_LO is shown in [CSI1_FRAME_ERR_COUNT_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-152. CSI1_FRAME_ERR_COUNT_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI1_FRAME_ERR_COUNT_LO	R	0x0	CSI Port 1, Frame Counter with Errors LSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_FRAME_ERR_COUNT. The CSI1_FRAME_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.134 CSI1_LINE_COUNT_HI Register (Address = 0x9C) [Default = 0x00]

CSI1_LINE_COUNT_HI is shown in [CSI1_LINE_COUNT_HI Register Field Descriptions](#).

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Table 8-153. CSI1_LINE_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI1_LINE_COUNT_HI	RC	0x0	CSI Port 1, Line Counter MSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_LINE_COUNT. The LSBs of the counter are sampled into the CSI1_LINE_COUNT_LO register and the counter is cleared.

8.6.1.135 CSI1_LINE_COUNT_LO Register (Address = 0x9D) [Default = 0x00]

CSI1_LINE_COUNT_LO is shown in [CSI1_LINE_COUNT_LO Register Field Descriptions](#).

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Table 8-154. CSI1_LINE_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI1_LINE_COUNT_LO	R	0x0	CSI Port 1, Line Counter LSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_LINE_COUNT. The CSI1_LINE_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.136 CSI1_LINE_ERR_COUNT_HI Register (Address = 0x9E) [Default = 0x00]

CSI1_LINE_ERR_COUNT_HI is shown in [CSI1_LINE_ERR_COUNT_HI Register Field Descriptions](#).

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Table 8-155. CSI1_LINE_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI1_LINE_ERR_COUNT_HI	RC	0x0	CSI Port 1, Line Counter with Errors MSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_LINE_ERR_COUNT. The LSBs of the counter are sampled into the CSI1_LINE_ERR_COUNT_LO register and the counter is cleared.

8.6.1.137 CSI1_LINE_ERR_COUNT_LO Register (Address = 0x9F) [Default = 0x00]

CSI1_LINE_ERR_COUNT_LO is shown in [CSI1_LINE_ERR_COUNT_LO Register Field Descriptions](#).

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Table 8-156. CSI1_LINE_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI1_LINE_ERR_COUNT_LO	R	0x0	CSI Port 1, Line Counter with Errors LSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_LINE_ERR_COUNT. The CSI1_LINE_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

8.6.1.138 VC_ID_MAP_0 Register (Address = 0xA0) [Default = 0x10]VC_ID_MAP_0 is shown in [VC_ID_MAP_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-157. VC_ID_MAP_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_0	R/W	0x10	If, the input VC_ID (from 971 and 953) is 0, it can be remapped to CSI_VC_MAP_0[3:0] If, the input VC_ID (from 971) is 1, it can be remapped to CSI_VC_MAP_0[7:4]

8.6.1.139 VC_ID_MAP_1 Register (Address = 0xA1) [Default = 0x32]VC_ID_MAP_1 is shown in [VC_ID_MAP_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-158. VC_ID_MAP_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_1	R/W	0x32	If, the input VC_ID (from 971) is 2, it can be remapped to CSI_VC_MAP_1[3:0] If, the input VC_ID (from 971) is 3, it can be remapped to CSI_VC_MAP_1[7:4]

8.6.1.140 VC_ID_MAP_2 Register (Address = 0xA2) [Default = 0x54]VC_ID_MAP_2 is shown in [VC_ID_MAP_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-159. VC_ID_MAP_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_2	R/W	0x54	If, the input VC_ID (from 971) is 4, it can be remapped to CSI_VC_MAP_2[3:0] If, the input VC_ID from 971 is 5 (or from 953 is 1), it can be remapped to CSI_VC_MAP_2[7:4]

8.6.1.141 VC_ID_MAP_3 Register (Address = 0xA3) [Default = 0x76]VC_ID_MAP_3 is shown in [VC_ID_MAP_3 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-160. VC_ID_MAP_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_3	R/W	0x76	If, the input VC_ID (from 971) is 6, it can be remapped to CSI_VC_MAP_3[3:0] If, the input VC_ID (from 971) is 7, it can be remapped to CSI_VC_MAP_3[7:4]

8.6.1.142 VC_ID_MAP_4 Register (Address = 0xA4) [Default = 0x98]VC_ID_MAP_4 is shown in [VC_ID_MAP_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-161. VC_ID_MAP_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_4	R/W	0x98	If, the input VC_ID (from 971) is 8, it can be remapped to CSI_VC_MAP_4[3:0] If, the input VC_ID (from 971) is 9, it can be remapped to CSI_VC_MAP_4[7:4]

8.6.1.143 VC_ID_MAP_5 Register (Address = 0xA5) [Default = 0xBA]VC_ID_MAP_5 is shown in [VC_ID_MAP_5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-162. VC_ID_MAP_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_5	R/W	0xBA	If, the input VC_ID from 971 is 10 (or from 953 is 2), it can be remapped to CSI_VC_MAP_5[3:0] If, the input VC_ID (from 971) is 11, it can be remapped to CSI_VC_MAP_5[7:4]

8.6.1.144 VC_ID_MAP_6 Register (Address = 0xA6) [Default = 0xDC]VC_ID_MAP_6 is shown in [VC_ID_MAP_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-163. VC_ID_MAP_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_6	WR	0xDC	If, the input VC_ID (from 971) is 12, it can be remapped to CSI_VC_MAP_6[3:0] If, the input VC_ID (from 971) is 13, it can be remapped to CSI_VC_MAP_6[7:4]

8.6.1.145 VC_ID_MAP_7 Register (Address = 0xA7) [Default = 0xFE]VC_ID_MAP_7 is shown in [VC_ID_MAP_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-164. VC_ID_MAP_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CSI_VC_MAP_7	R/W	0xFE	If, the input VC_ID (from 971) is 14, it can be remapped to CSI_VC_MAP_7[3:0] If, the input VC_ID from 971 is 15 (or from 953 is 3), it can be remapped to CSI_VC_MAP_7[7:4]

8.6.1.146 IND_ACC_CTL Register (Address = 0xB0) [Default = 0x00]IND_ACC_CTL is shown in [IND_ACC_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-165. IND_ACC_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-2	IA_SEL	R/W	0x0	Indirect Access Register Select: Selects target for register access 0000: Pattern Generator Registers 0001: FPD RX Port 0 Registers 0010: FPD RX Port 1 Registers 0011: FPD RX Port 2 Registers 0100: FPD RX Port 3 Registers 0101: PLL Control Registers 0110: Simultaneous write to FPD RX Port 0-3 registers 0111: CSI-2 Analog Registers 1000: Read of Configuration Data (loaded from eFuse ROM) 1001: Read of DIE ID (loaded from eFuse ROM) 1010: SAR ADC Registers
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data. Note that this bit needs to be set (to 1) if we need to do COR on an indirect page

8.6.1.147 IND_ACC_ADDR Register (Address = 0xB1) [Default = 0x00]IND_ACC_ADDR is shown in [IND_ACC_ADDR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-166. IND_ACC_ADDR Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IA_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

8.6.1.148 IND_ACC_DATA Register (Address = 0xB2) [Default = 0x00]IND_ACC_DATA is shown in [IND_ACC_DATA Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-167. IND_ACC_DATA Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IA_DATA	R/W	0x0	Indirect Access Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected block register

8.6.1.149 BIST_CTL Register (Address = 0xB3) [Default = 0x08]

BIST_CTL is shown in [BIST_CTL Register Field Descriptions](#).

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Table 8-168. BIST_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00: No toggling 01: Alternating 1/0 toggling 1x: Toggle based on BIST data
5-4	RESERVED	R/W	0x0	Reserved
3	BIST_PIN_CONFIG	R/W	0x1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
2-1	BIST_CLOCK_SOURCE	R/W	0x0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. Note: When connected to a DS90UB913A, a setting of 0x3 may result in a clock frequency that is too slow for proper recovery.
0	BIST_EN	R/W	0x0	BIST Control 1: Enabled 0: Disabled

8.6.1.150 MODE_CAD_STS Register (Address = 0xB8) [Default = 0xF8]

MODE_CAD_STS is shown in [MODE_CAD_STS Register Field Descriptions](#).

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Table 8-169. MODE_CAD_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	CAD_DONE	R	0x1	CAD Done: If set, indicates the CAD decode has completed and latched into the CAD status bits.
6-4	CAD	R	0x7	CAD Decode 3-bit decode from CAD pin
3	MODE_DONE	R	0x1	MODE Done: If set, indicates the MODE decode has completed and latched into the MODE status bits.
2-0	MODE	R	0x0	MODE Decode 3-bit decode from MODE pin

8.6.1.151 LINK_ERROR_COUNT Register (Address = 0xB9) [Default = 0x13]

LINK_ERROR_COUNT is shown in [LINK_ERROR_COUNT Register Field Descriptions](#).

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Table 8-170. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	LINK_ERR_COUNT_EN	R/W	0x1	Enable serial link data integrity error count 1: Enable error count 0: DISABLE

Table 8-170. LINK_ERROR_COUNT Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-0	RESERVED	R/W	0x3	Reserved

8.6.1.152 DCA_CONTROL Register (Address = 0xBA) [Default = 0x83]DCA_CONTROL is shown in [DCA_CONTROL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-171. DCA_CONTROL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DISABLE_DCA_CRC	R/W	0x1	Disable DCA CRC Checking DCA CRC errors will be ignored. The DCA CRC protects the DCA sequence data that is delivered as part of the Forward Channel DCA sequence from the Serializer to the Deserializer. This register bit will have no effect if the Serializer is not sending a CRC as part of the Forward Channel DCA sequence.
6-5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x3	Reserved

8.6.1.153 CSI_PLL_CTL2 Register (Address = 0xBB) [Default = 0x74]CSI_PLL_CTL2 is shown in [CSI_PLL_CTL2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-172. CSI_PLL_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FWD_DIS_IMMEDIATE	R/W	0x0	Forwarding Disable Mode When disabling forwarding, default operation for Best Effort forwarding is to wait for video line boundary prior to disabling forwarding. In synchronous forwarding, default is to wait for the next frame boundary. When this bit is set, forwarding will be disabled immediately upon assertion of the FWD_PORTx_DIS controls in the FWD_CTL1 register.
6-4	RESERVED	R/W	0x7	Reserved
3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R/W	0x4	Reserved

8.6.1.154 FV_MIN_TIME Register (Address = 0xBC) [Default = 0x80]FV_MIN_TIME is shown in [FV_MIN_TIME Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-173. FV_MIN_TIME Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FRAME_VALID_MIN	R/W	0x80	Frame Valid Minimum Time This register controls the minimum time the FrameValid (FV) should be active before the Raw mode FPD3 receiver generates a FrameStart packet. Duration is in FPD3 clock periods.

8.6.1.155 GPIO_PD_CTL Register (Address = 0xBE) [Default = 0x00]GPIO_PD_CTL is shown in [GPIO_PD_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-174. GPIO_PD_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO7_PD_DIS	R/W	0x0	GPIO7 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
6	GPIO6_PD_DIS	R/W	0x0	GPIO6 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
5	GPIO5_PD_DIS	R/W	0x0	GPIO5 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
4	GPIO4_PD_DIS	R/W	0x0	GPIO4 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
3	RESERVED	R/W	0x0	
2	GPIO2_PD_DIS	R/W	0x0	GPIO2 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
1	GPIO1_PD_DIS	R/W	0x0	GPIO1 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
0	GPIO0_PD_DIS	R/W	0x0	GPIO0 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor

8.6.1.156 IQ_DIV Register (Address = 0xC2) [Default = 0x00]IQ_DIV is shown in [IQ_DIV Register Field Descriptions](#).

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Table 8-175. IQ_DIV Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	DIV_IQ_SEL_DIV_CH3	R/W	0x0	FPD Rate Divider Settings: 00: Divide by 1: 7.55G mode 01: Divide by 2: 3.775G mode 10: Divide by 4: 1.8875G mode 11: Divide by 2: 3.775G EOM mode (if CH3_ALT_DIV4_EN in page5 is set to 0) OR Divide by 4: 1.8875G EOM mode (if CH3_ALT_DIV4_EN in page5 is set to 1)
5-4	DIV_IQ_SEL_DIV_CH2	R/W	0x0	FPD Rate Divider Settings: 00: Divide by 1: 7.55G mode 01: Divide by 2: 3.775G mode 10: Divide by 4: 1.8875G mode 11: Divide by 2: 3.775G EOM mode (if CH2_ALT_DIV4_EN in page5 is set to 0) OR Divide by 4: 1.8875G EOM mode (if CH2_ALT_DIV4_EN in page5 is set to 1)
3-2	DIV_IQ_SEL_DIV_CH1	R/W	0x0	FPD Rate Divider Settings: 00: Divide by 1: 7.55G mode 01: Divide by 2: 3.775G mode 10: Divide by 4: 1.8875G mode 11: Divide by 2: 3.775G EOM mode (if CH1_ALT_DIV4_EN in page5 is set to 0) OR Divide by 4: 1.8875G EOM mode (if CH1_ALT_DIV4_EN in page5 is set to 1)
1-0	DIV_IQ_SEL_DIV_CH0	R/W	0x0	FPD Rate Divider Settings: 00: Divide by 1: 7.55G mode 01: Divide by 2: 3.775G mode 10: Divide by 4: 1.8875G mode 11: Divide by 2: 3.775G EOM mode (if CH0_ALT_DIV4_EN in page5 is set to 0) OR Divide by 4: 1.8875G EOM mode (if CH0_ALT_DIV4_EN in page5 is set to 1)

8.6.1.157 CSI_PORT2_FIFO_CTRL Register (Address = 0xC7) [Default = 0x00]

CSI_PORT2_FIFO_CTRL is shown in [CSI_PORT2_FIFO_CTRL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-176. CSI_PORT2_FIFO_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	CSI_PORT2_EN	R/W	0x0	CSI Transmit Port2 Enable Setting this bit enables the CSI-2 Transmit Port 2 for replication of either CSI Transmit Port 0 or 1 data. Selection of which CSI Transmit port is replicated is determined by the REPLICATE_CSI2_SEL register control. This bit should be set prior to enabling the selected CSI Transmit Port.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	CSI_FIFO_UNDERRUN		0x0	CSI Port 2 FIFO Underrun Flag If this bit is set, an underrun has been detected on the CSI Port 2 FIFO. This register will be cleared on read.
0	CSI_FIFO_OVERFLOW		0x0	CSI Port 2 FIFO Overflow Flag If this bit is set, an overflow has been detected on the CSI Port 2 FIFO. This register will be cleared on read.

8.6.1.158 CSI_PLL_DIV Register (Address = 0xC9) [Default = 0x32]

CSI_PLL_DIV is shown in [CSI_PLL_DIV Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-177. CSI_PLL_DIV Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R	0x0	
5-0	CSI_PLL_DIVIDER	R/W	0x32	<p>CSI PLL Divider control Strap 2.5G: 6'h32 800M: 6'h20</p> <p>This register sets the CSI PLL Divider control to configure the PLL for the desired speed of operation. This field controls the divider for the VCO operation. The CSI Transmit frequency is dependent on this setting plus the VCO Post Divider setting which is typically set automatically by the CSI_TX_SPEED register control. The VCO frequency is based on the following equation:</p> $\text{VCO freq} = (2^{\text{pll_fb_div}}) * 25 \text{ MHz} * \text{csi_pll_divider}$ <p>where pll_fb_div is register 0x92[7:6] on page 7</p> <p>The CSI Transmit frequency is equal to the VCO frequency divided by the VCO Post divider.</p> <p>For example, the 2.5GHz default setting of 50 will set the VCO to 2.5 GHz. The VCO Post divider setting of 1 sets the CSI Transmit frequency to 2.5G</p> <p>The 800 MHz default setting of 32 will set the VCO to 1.6 GHz.. The VCO Post divider setting of 2 sets the CSI Transmit frequency to 800 MHz.</p> <p>At power-up, this field is set based on the MODE pin strap value.</p>

8.6.1.159 LOCAL_DEV_ICR Register (Address = 0xCA) [Default = 0x00]

LOCAL_DEV_ICR is shown in [LOCAL_DEV_ICR Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-178. LOCAL_DEV_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	IE_CSI_PORT2_FIFO	R/W	0x0	<p>Interrupt on CSI Port2 FIFO Status</p> <p>When enabled, an interrupt will be generated on detection of an error on the CSI Port2 FIFO. CSI2 FIFO status is reported in the CSI_PORT2_FIFO_CTRL register.</p>
4	IE_EXC_FWD_STS	R/W	0x0	<p>Interrupt on Exclusive Fowarding Status</p> <p>When enabled, an interrupt will be generated on detection of a change in one of the Exclusive Fowarding Status conditions. Exclusive Forwarding status is reported in the EXCLUSIVE_FWD_STS register.</p>
3	IE_REFCLK_DET	R/W	0x0	<p>Interrupt on change in REFCLK Detect status</p> <p>When enabled, an interrupt will be generated on detection of a change in sensor the Reference clock status based on configuration in the REFCLK_DET_INT_CTL register. Reference clock status is reported in the REFCLK_VALID bit in the DEVICE_STS Register</p>
2	IE_TEMP_SENSOR	R/W	0x0	<p>Interrupt on Temp Sensor</p> <p>When enabled, an interrupt will be generated from the Temperature Sensor. Temp Sensor interrupts are controlled by registers 0x23 and 0x25 on Indirect page 10.</p>
1	IE_VOLT_SENSOR	R/W	0x0	<p>Interrupt on Voltage Sensor</p> <p>When enabled, an interrupt will be generated from the Voltage Sensor. Temp Sensor interrupts are controlled by registers 0x23-0x26 on Indirect page 10.</p>

Table 8-178. LOCAL_DEV_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	IE_LINE_FAULT	R/W	0x0	Interrupt on Line Fault When enabled, an interrupt will be generated from the Line Fault detection circuit. Line Fault interrupts are controlled by registers 0x27-0x28 on Indirect page 10.

8.6.1.160 LOCAL_DEV_ISR Register (Address = 0xCB) [Default = 0x00]LOCAL_DEV_ISR is shown in [LOCAL_DEV_ISR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-179. LOCAL_DEV_ISR Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5	IS_CSI_PORT2_FIFO		0x0	Interrupt on CSI PORT2 FIFO Status An error on the CSI Port2 FIFO has been detected. This interrupt indicates there might be errors on the datapath when replicating data to the CSI Port2 interface. CS2 FIFO status is reported in the CSI_PORT2_FIFO_CTRL register. This interrupt condition will be cleared by reading the CSI_PORT2_FIFO_CTRL register.
4	IS_EXC_FWD_STS		0x0	Interrupt on Exclusive Fowrading Status A change in one of the Exclusive Fowarding Status conditions has been detected. Exclusive Forwarding status is reported in the EXCLUSIVE_FWD_STS register. This interrupt condition will be cleared by reading the EXCLUSIVE_FWD_STS register.
3	IS_REFCLK_DET		0x0	Interrupt on change in REFCLK Detect status A change in sensor the Reference clock status has been detected. Reference clock status is reported in the REFCLK_VALID bit in the DEVICE_STS Register. This interrupt condition will be cleared by reading this register.
2	IS_TEMP_SENSOR	R	0x0	Interrupt on Temp Sensor When enabled, an interrupt will be generated from the Temperature Sensor. Temp Sensor interrupts are controlled by registers 0x23 and 0x25 on Indirect page 10.
1	IS_VOLT_SENSOR	R	0x0	Interrupt on Voltage Sensor When enabled, an interrupt will be generated from the Voltage Sensor. Temp Sensor interrupts are controlled by registers 0x23-0x26 on Indirect page 10.
0	IS_LINE_FAULT	R	0x0	Interrupt on Line Fault When enabled, an interrupt will be generated from the Line Fault detection circuit. Line Fault interrupts are controlled by registers 0x27-0x28 on Indirect page 10.

8.6.1.161 EXCLUSIVE_FWD_STS Register (Address = 0xCF) [Default = 0x00]EXCLUSIVE_FWD_STS is shown in [EXCLUSIVE_FWD_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-180. EXCLUSIVE_FWD_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0x0	RESERVED
1	EXC_FWD_FIFO_OVER_FLAG		0x0	Exclusive Forwarding FIFO Overrun Flag This register indicates a FIFO overrun condition has occurred on the Exclusive Forwarding datapath for CSI Port 1. This register is cleared on a read of this register.

Table 8-180. EXCLUSIVE_FWD_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	EXC_FWD_FIFO_UNDER_FLAG	R	0x0	Exclusive Forwarding FIFO Underrun Flag This register indicates a FIFO underrun condition has occurred on the Exclusive Forwarding datapath for CSI Port 1. This register is cleared on a read of this register.

8.6.1.162 PORT_DEBUG Register (Address = 0xD0) [Default = 0x00]PORT_DEBUG is shown in [PORT_DEBUG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-181. PORT_DEBUG Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	RESERVED
5	SER_BIST_ACT	R	0x0	Serializer BIST active This register indicates the Serializer is in BIST mode. If the Deserializer is not in BIST mode, this could indicate an error condition.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	FORCE_BC_ERRORS	R/W	0x0	This bit introduces continuous errors into Back channel frame.
0	FORCE_1_BC_ERROR	RH/W1S	0x0	This bit introduces one error into Back channel frame. Self clearing bit.

8.6.1.163 CMLOUT_TEST_PAT_0 Register (Address = 0xD5) [Default = 0x55]CMLOUT_TEST_PAT_0 is shown in [CMLOUT_TEST_PAT_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-182. CMLOUT_TEST_PAT_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CMLOUT_TEST_PAT_HI	R/W	0x55	CML Output Test Pattern Bits 15:8 of fixed pattern for characterization test Test pattern generation is enabled by setting the CMLOUT_PATGEN_EN control in the BC_AND_CML_CTRL register.

8.6.1.164 CMLOUT_TEST_PAT_1 Register (Address = 0xD6) [Default = 0x55]CMLOUT_TEST_PAT_1 is shown in [CMLOUT_TEST_PAT_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-183. CMLOUT_TEST_PAT_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	CMLOUT_TEST_PAT_LO	R/W	0x55	CML Output Test Pattern Bits 7:0 of fixed pattern for characterization test Test pattern generation is enabled by setting the CMLOUT_PATGEN_EN control in the BC_AND_CML_CTRL register.

8.6.1.165 PORT_ICR_HI Register (Address = 0xD8) [Default = 0x00]PORT_ICR_HI is shown in [PORT_ICR_HI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-184. PORT_ICR_HI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	IE_FC_GPIO	R/W	0x0	Interrupt on FC GPIO signals When enabled, an interrupt will be generated on detection of a change in one of the Forward Channel GPIO signals. Forward Channel GPIO status is reported in the FC_GPIO_STS register.
3	IE_FC_SEN_STS	R/W	0x0	Interrupt on change in Sensor Status When enabled, an interrupt will be generated on detection of a change in sensor status as reported in the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers.
2	IE_FPD_ENC_ERR	R/W	0x0	Interrupt on FPD-Link Receiver Encoding Error When enabled, an interrupt will be generated on detection of an encoding error on the FPD-Link interface for the receive port as reported in the FPD_ENC_ERROR bit in the RX_PORT_STS2 register
1	IE_BCC_SEQ_ERR/ IE_BCC_ERROR	R/W	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: Interrupt on BCC SEQ Sequence Error When enabled, an interrupt will be generated if a Sequence Error is detected for the Bidirectional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: Interrupt on BCC Error When enabled, an interrupt will be generated if a BCC Error is detected for the Bidirectional Control Channel receiver as reported in the BCC_ERROR bit in the RX_PORT_STS1 register.
0	IE_BCC_CRC_ERR	R/W	0x0	Interrupt on BCC CRC error detect When enabled, an interrupt will be generated if a CRC error is detected on a Bidirectional Control Channel frame received over the FPD-Link forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.

8.6.1.166 PORT_ICR_LO Register (Address = 0xD9) [Default = 0x00]PORT_ICR_LO is shown in [PORT_ICR_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-185. PORT_ICR_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_FRAME_FREEZE_DET	R/W	0x0	Interrupt on Frame Freeze Detection When enabled, and interrupt will be generated if a Frame Freeze condition is detected. Frame Freeze interrupt control/status is via the FFD_ICR_HI/LO and FFD_ISR_HI/LO registers.
6	IE_LINE_LEN_CHG	R/W	0x0	Interrupt on Video Line length When enabled, an interrupt will be generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
5	IE_LINE_CNT_CHG	R/W	0x0	Interrupt on Video Line count When enabled, an interrupt will be generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.

Table 8-185. PORT_ICR_LO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	IE_BUFFER_ERR	R/W	0x0	Interrupt on Receiver Buffer Error When enabled, an interrupt will be generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.
3	IE_CSI_RX_ERR	R/W	0x0	Interrupt on CSI Receiver Error When enabled, an interrupt will be generated on detection of an error by the CSI Receiver. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A).
2	IE_FPD_PAR_ERR	R/W	0x0	Interrupt on FPD-Link Receiver Parity Error When enabled, an interrupt will be generated on detection of parity errors on the FPD-Link interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
1	IE_PORT_PASS	R/W	0x0	Interrupt on change in Port PASS status When enabled, an interrupt will be generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
0	IE_LOCK_STS	R/W	0x0	Interrupt on change in Lock Status When enabled, an interrupt will be generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

8.6.1.167 PORT_ISR_HI Register (Address = 0xDA) [Default = 0x00]

PORT_ISR_HI is shown in [PORT_ISR_HI Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-186. PORT_ISR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4	IS_FC_GPIO	R	0x0	FC GPIO Interrupt Status A change in forward channel GPIO signal has been detected. Forward Channel GPIO status is reported in the FC_GPIO_STS register. This interrupt condition will be cleared by reading the FC_GPIO_STS register.
3	IS_FC_SEN_STS	R	0x0	Interrupt on change in Sensor Status A change in Sensor Status has been detected. Sensor Status is reported in the SENSOR_STS_X registers. This interrupt condition will be cleared by reading the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers.
2	IS_FPD_ENC_ERR	R	0x0	FPD-Link Receiver Encode Error Interrupt Status An encoding error on the FPD-Link interface for the receive port has been detected. Status is reported in the FPD_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.

Table 8-186. PORT_ISR_HI Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	IS_BCC_SEQ_ERR/ IS_BCC_ERROR	R	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bidirectional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: BCC Error Interrupt Status An error has been detected for the Bidirectional Control Channel forward channel receiver. Status is reported in the BCC_ERROR bit in the RX_PORT_STS1 register with detailed reporting in the BCC_STATUS register. This interrupt condition will be cleared by reading the BCC_STATUS register.
0	IS_BCC_CRC_ERR	R	0x0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bidirectional Control Channel frame received over the FPD-Link forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.

8.6.1.168 PORT_ISR_LO Register (Address = 0xDB) [Default = 0x00]PORT_ISR_LO is shown in [PORT_ISR_LO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-187. PORT_ISR_LO Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_FRAME_FREEZE_DET	R	0x0	Frame Freeze Detection Interrupt Status A Frame Freeze condition is detected. Status is reported via the FFD_ISR_HI/LO registers. This interrupt condition will be cleared by reading the FFD_ISR_HI/LO registers.
6	IS_LINE_LEN_CHG	R	0x0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
5	IS_LINE_CNT_CHG	R	0x0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
4	IS_BUFFER_ERR	R	0x0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
3	IS_CSI_RX_ERR	R	0x0	CSI Receiver Error Interrupt Status The CSI Receiver has detected an error. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A). This interrupt condition will be cleared by reading the CSI_RX_STS register.

Table 8-187. PORT_ISR_LO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	IS_FPD_PAR_ERR	R	0x0	FPD-Link Receiver Parity Error Interrupt Status A parity error on the FPD-Link interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.
1	IS_PORT_PASS	R	0x0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.
0	IS_LOCK_STS	R	0x0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.

8.6.1.169 FC_GPIO_STS Register (Address = 0xDC) [Default = 0x00]FC_GPIO_STS is shown in [FC_GPIO_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-188. FC_GPIO_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO3_INT_STS	RC	0x0	GPIO3 Interrupt Status This bit indicates an interrupt condition has been met for GPIO3. This bit is cleared on read.
6	GPIO2_INT_STS	RC	0x0	GPIO2 Interrupt Status This bit indicates an interrupt condition has been met for GPIO2. This bit is cleared on read.
5	GPIO1_INT_STS	RC	0x0	GPIO1 Interrupt Status This bit indicates an interrupt condition has been met for GPIO1. This bit is cleared on read.
4	GPIO0_INT_STS	RC	0x0	GPIO0 Interrupt Status This bit indicates an interrupt condition has been met for GPIO0. This bit is cleared on read.
3	FC_GPIO3_STS	R	0x0	Forward Channel GPIO3 Status This bit indicates the current value for forward channel GPIO3.
2	FC_GPIO2_STS	R	0x0	Forward Channel GPIO2 Status This bit indicates the current value for forward channel GPIO2.
1	FC_GPIO1_STS	R	0x0	Forward Channel GPIO1 Status This bit indicates the current value for forward channel GPIO1.
0	FC_GPIO0_STS	R	0x0	Forward Channel GPIO0 Status This bit indicates the current value for forward channel GPIO0.

8.6.1.170 FC_GPIO_ICR Register (Address = 0xDD) [Default = 0x00]FC_GPIO_ICR is shown in [FC_GPIO_ICR Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-189. FC_GPIO_ICR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO3_FALL_IE	R/W	0x0	GPIO3 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO3.

Table 8-189. FC_GPIO_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	GPIO3_RISE_IE	R/W	0x0	GPIO3 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO3.
5	GPIO2_FALL_IE	R/W	0x0	GPIO2 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO2.
4	GPIO2_RISE_IE	R/W	0x0	GPIO2 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO2.
3	GPIO1_FALL_IE	R/W	0x0	GPIO1 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO1.
2	GPIO1_RISE_IE	R/W	0x0	GPIO1 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO1.
1	GPIO0_FALL_IE	R/W	0x0	GPIO0 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO0.
0	GPIO0_RISE_IE	R/W	0x0	GPIO0 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO0.

8.6.1.171 SEN_INT_RISE_STS Register (Address = 0xDE) [Default = 0x00]SEN_INT_RISE_STS is shown in [SEN_INT_RISE_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-190. SEN_INT_RISE_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SEN_INT_RISE	RC	0x0	Sensor Interrupt Rise Status This register provides the interrupt status for rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_RISE_MASK register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

8.6.1.172 SEN_INT_FALL_STS Register (Address = 0xDF) [Default = 0x00]SEN_INT_FALL_STS is shown in [SEN_INT_FALL_STS Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-191. SEN_INT_FALL_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SEN_INT_FALL	RC	0x0	Sensor Interrupt Fall Status This register provides the interrupt status for falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_FALL_MASK register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

8.6.1.173 CML_CTRL_1 Register (Address = 0xE0) [Default = 0x3F]CML_CTRL_1 is shown in [CML_CTRL_1 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-192. CML_CTRL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CMLTX_SER_EN	R/W	0x0	CML Transmit Serializer Enable This register enables the CML transmit serializer in analog.
6	CMLTX_EN	R/W	0x0	CML Transmit Driver Enable This control enables the CML Transmit driver in analog. It is also used to enable the CML Transmit datapath FIFO.
5	RESERVED	R/W	0x1	Reserved
4-3	CMLR1_EN	R/W	0x3	CML Swing Control setting swing(V) 11 1.10 MAX SWING 10 0.96 01 0.82 00 0.68 MIN SWING
2-1	RESERVED	R/W	0x3	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.1.174 CML_CTRL_2 Register (Address = 0xE1) [Default = 0x3F]CML_CTRL_2 is shown in [CML_CTRL_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-193. CML_CTRL_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CMLTX_CLK_GATE	R/W	0x0	set to 1 to enable CML retime mode
6	CLR_FIFO_ERRORS	R/W	0x0	Setting this register to 1 will clear the CML Transmit FIFO Error flags, CML_FIFO_OVERFLOW and CML_FIFO_UNDERFLOW. This register should be set back to 0 to re-arm the error flags.
5-0	RESERVED	R/W	0x3F	Reserved

8.6.1.175 BC_AND_CML_CTRL Register (Address = 0xE2) [Default = 0x00]BC_AND_CML_CTRL is shown in [BC_AND_CML_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-194. BC_AND_CML_CTRL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	CMLDIV_EN	R/W	0x0	CML Divider Settings: 00: Divide by 1: 7.55G mode 01: Divide by 2: 3.775G mode 10: Divide by 4: 1.8875G mode 11: RESERVED
5	CML_FIFO_OVERFLOW	R	0x0	CML FIFO Overflow Flag This flag indicates the CML FIFO has detected an Overflow condition. This flag will be latched until cleared by the CLR_FIFO_ERRORS bit in the CML_CTRL_2 register.
4	CML_FIFO_UNDERRUN	R	0x0	CML FIFO Overflow Flag This flag indicates the CML FIFO has detected an Overflow condition. This flag will be latched until cleared by the CLR_FIFO_ERRORS bit in the CML_CTRL_2 register.
3	RESERVED	R/W	0x0	Reserved
2	CMLOUT_PATGEN_EN	R/W	0x0	CML Output Test Pattern Enable Setting this bit to 1 enables the CML Output test pattern. Data for the test pattern is controlled via the CMLOUT_TEST_PAT_HI/LO registers.
1	RESERVED	R/W	0x0	Reserved

Table 8-194. BC_AND_CML_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RESERVED	R/W	0x0	Reserved

8.6.1.176 CHANNEL_MODE Register (Address = 0xE4) [Default = 0x00]CHANNEL_MODE is shown in [CHANNEL_MODE Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-195. CHANNEL_MODE Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R	0x0	Reserved
4-3	RESERVED	R/W	0x0	Reserved
2-0	REG_FPD_FUNC_MODE	R/W	0x0	FPD interface Mode Selection: Strap 0,1,2,4 000: FPD4 Sync Mode 001: FPD4 Non-sync Mode 010: FPD3 CSI Sync/Non-sync Mode 011: Reserved 100: FPD3 DVP RAW12 HF 101: FPD3 DVP RAW10 110: FPD3 DVP RAW12 LF 111: Reserved At power-up, this field is set based on the MODE pin strap value.

8.6.1.177 SAR_ADC_DOUT Register (Address = 0xE9) [Default = 0x00]SAR_ADC_DOUT is shown in [SAR_ADC_DOUT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-196. SAR_ADC_DOUT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SAR_ADC_DOUT_LV	R	0x0	ADC output - Configurable for Line-Fault, or temp-sensor

8.6.1.178 FPD_RX_ID0 Register (Address = 0xF0) [Default = 0x5F]FPD_RX_ID0 is shown in [FPD_RX_ID0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-197. FPD_RX_ID0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID0	R	0x5F	FPD_RX_ID0: First byte ID code: ' _ '

8.6.1.179 FPD_RX_ID1 Register (Address = 0xF1) [Default = 0x55]FPD_RX_ID1 is shown in [FPD_RX_ID1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-198. FPD_RX_ID1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID1	R	0x55	FPD_RX_ID1: 2nd byte of ID code: 'U'

8.6.1.180 FPD_RX_ID2 Register (Address = 0xF2) [Default = 0x42]

FPD_RX_ID2 is shown in [FPD_RX_ID2 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-199. FPD_RX_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID2	R	0x42	FPD_RX_ID2: 3rd byte of ID code: 'B'

8.6.1.181 FPD_RX_ID3 Register (Address = 0xF3) [Default = 0x39]

FPD_RX_ID3 is shown in [FPD_RX_ID3 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-200. FPD_RX_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID3	R	0x39	FPD_RX_ID3: 4th byte of ID code: '9'

8.6.1.182 FPD_RX_ID4 Register (Address = 0xF4) [Default = 0x37]

FPD_RX_ID4 is shown in [FPD_RX_ID4 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-201. FPD_RX_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID4	R	0x37	FPD_RX_ID4: 4th byte of ID code: '7'

8.6.1.183 FPD_RX_ID5 Register (Address = 0xF5) [Default = 0x30]

FPD_RX_ID5 is shown in [FPD_RX_ID5 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-202. FPD_RX_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID5	R	0x30	FPD_RX_ID5: 5th byte of ID code: '0'

8.6.1.184 FPD_RX_ID6 Register (Address = 0xF6) [Default = 0x32]

FPD_RX_ID6 is shown in [FPD_RX_ID6 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-203. FPD_RX_ID6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	FPD_RX_ID6	R	0x32	FPD_RX_ID6: 5th byte of ID code: '2'

8.6.1.185 I2C_RX0_ID Register (Address = 0xF8) [Default = 0x00]

I2C_RX0_ID is shown in [I2C_RX0_ID Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-204. I2C_RX0_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	RX_PORT0_ID	R/W	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
0	RESERVED	R	0x0	Reserved

8.6.1.186 I2C_RX1_ID Register (Address = 0xF9) [Default = 0x00]I2C_RX1_ID is shown in [I2C_RX1_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-205. I2C_RX1_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	RX_PORT1_ID	R/W	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
0	RESERVED	R	0x0	Reserved

8.6.1.187 I2C_RX2_ID Register (Address = 0xFA) [Default = 0x00]I2C_RX2_ID is shown in [I2C_RX2_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-206. I2C_RX2_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	RX_PORT2_ID	R/W	0x0	7-bit Receive Port 2 I2C ID Configures the decoder for detecting transactions designated for Receiver port 2 registers. This provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. A value of 0 in this field disables the Port2 decoder.
0	RESERVED	R	0x0	Reserved

8.6.1.188 I2C_RX3_ID Register (Address = 0xFB) [Default = 0x00]I2C_RX3_ID is shown in [I2C_RX3_ID Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-207. I2C_RX3_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7-1	RX_PORT3_ID	R/W	0x0	7-bit Receive Port 3 I2C ID Configures the decoder for detecting transactions designated for Receiver port 3 registers. This provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. A value of 0 in this field disables the Port3 decoder.
0	RESERVED	R	0x0	Reserved

8.6.1.189 FFD_ICR_HI Register (Address = 0xFC) [Default = 0x00]

FFD_ICR_HI is shown in [FFD_ICR_HI Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-208. FFD_ICR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IE_FFD_ICR_HI	R/W	0x0	Frame Freeze Detection Interrupt Control for virtual channel [7:0]

8.6.1.190 FFD_ICR_LO Register (Address = 0xFD) [Default = 0x00]

FFD_ICR_LO is shown in [FFD_ICR_LO Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-209. FFD_ICR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IE_FFD_ICR_LO	R/W	0x0	Frame Freeze Detection Interrupt Control for virtual channel [15:8]

8.6.1.191 FFD_ISR_HI Register (Address = 0xFE) [Default = 0x00]

FFD_ISR_HI is shown in [FFD_ISR_HI Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-210. FFD_ISR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IS_FFD_ISR_HI	RC	0x0	Frame Freeze Detection Interrupt Status In DVP mode, only bit[0] is valid. In CSI mode, bit[7:0] are for virtual channel [7:0].

8.6.1.192 FFD_ISR_LO Register (Address = 0xFF) [Default = 0x00]

FFD_ISR_LO is shown in [FFD_ISR_LO Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-211. FFD_ISR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IS_FFD_ISR_LO	RC	0x0	Frame Freeze Detection Interrupt Status In DVP mode, every bit is 0. In CSI mode, bit[7:0] are for virtual channel [15:8].

8.6.2 PATGEN_and_CSI-2_Trim Registers

[PATGEN_AND_CSI-2_TRIM Registers](#) lists the memory-mapped registers for the PATGEN_and_CSI-2_Trim registers. All register offset addresses not listed in [PATGEN_AND_CSI-2_TRIM Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-212. PATGEN_AND_CSI-2_TRIM Registers

Address	Acronym	Register Name	Section
0x1	PGEN_CTL	PGEN_CTL	Go
0x2	PGEN_CFG	PGEN_CFG	Go
0x3	PGEN_CSI_DI	PGEN_CSI_DI	Go
0x4	PGEN_LINE_SIZE1	PGEN_LINE_SIZE1	Go
0x5	PGEN_LINE_SIZE0	PGEN_LINE_SIZE0	Go

Table 8-212. PATGEN_AND_CSI-2_TRIM Registers (continued)

Address	Acronym	Register Name	Section
0x6	PGEN_BAR_SIZE1	PGEN_BAR_SIZE1	Go
0x7	PGEN_BAR_SIZE0	PGEN_BAR_SIZE0	Go
0x8	PGEN_ACT_LPF1	PGEN_ACT_LPF1	Go
0x9	PGEN_ACT_LPF0	PGEN_ACT_LPF0	Go
0xA	PGEN_TOT_LPF1	PGEN_TOT_LPF1	Go
0xB	PGEN_TOT_LPF0	PGEN_TOT_LPF0	Go
0xC	PGEN_LINE_PD1	PGEN_LINE_PD1	Go
0xD	PGEN_LINE_PD0	PGEN_LINE_PD0	Go
0xE	PGEN_VBP	PGEN_VBP	Go
0xF	PGEN_VFP	PGEN_VFP	Go
0x10	PGEN_COLOR0	PGEN_COLOR0	Go
0x11	PGEN_COLOR1	PGEN_COLOR1	Go
0x12	PGEN_COLOR2	PGEN_COLOR2	Go
0x13	PGEN_COLOR3	PGEN_COLOR3	Go
0x14	PGEN_COLOR4	PGEN_COLOR4	Go
0x15	PGEN_COLOR5	PGEN_COLOR5	Go
0x16	PGEN_COLOR6	PGEN_COLOR6	Go
0x17	PGEN_COLOR7	PGEN_COLOR7	Go
0x18	PGEN_COLOR8	PGEN_COLOR8	Go
0x19	PGEN_COLOR9	PGEN_COLOR9	Go
0x1A	PGEN_COLOR10	PGEN_COLOR10	Go
0x1B	PGEN_COLOR11	PGEN_COLOR11	Go
0x1C	PGEN_COLOR12	PGEN_COLOR12	Go
0x1D	PGEN_COLOR13	PGEN_COLOR13	Go
0x1E	PGEN_COLOR14	PGEN_COLOR14	Go
0x1F	PGEN_COLOR15	PGEN_COLOR15	Go
0x21	CSI1_PGEN_CTL	CSI1_PGEN_CTL	Go
0x22	CSI1_PGEN_CFG	CSI1_PGEN_CFG	Go
0x23	CSI1_PGEN_CSI_DI	CSI1_PGEN_CSI_DI	Go
0x24	CSI1_PGEN_LINE_SIZE1	CSI1_PGEN_LINE_SIZE1	Go
0x25	CSI1_PGEN_LINE_SIZE0	CSI1_PGEN_LINE_SIZE0	Go
0x26	CSI1_PGEN_BAR_SIZE1	CSI1_PGEN_BAR_SIZE1	Go
0x27	CSI1_PGEN_BAR_SIZE0	CSI1_PGEN_BAR_SIZE0	Go
0x28	CSI1_PGEN_ACT_LPF1	CSI1_PGEN_ACT_LPF1	Go
0x29	CSI1_PGEN_ACT_LPF0	CSI1_PGEN_ACT_LPF0	Go
0x2A	CSI1_PGEN_TOT_LPF1	CSI1_PGEN_TOT_LPF1	Go
0x2B	CSI1_PGEN_TOT_LPF0	CSI1_PGEN_TOT_LPF0	Go
0x2C	CSI1_PGEN_LINE_PD1	CSI1_PGEN_LINE_PD1	Go
0x2D	CSI1_PGEN_LINE_PD0	CSI1_PGEN_LINE_PD0	Go
0x2E	CSI1_PGEN_VBP	CSI1_PGEN_VBP	Go
0x2F	CSI1_PGEN_VFP	CSI1_PGEN_VFP	Go
0x30	CSI1_PGEN_COLOR0	CSI1_PGEN_COLOR0	Go
0x31	CSI1_PGEN_COLOR1	CSI1_PGEN_COLOR1	Go
0x32	CSI1_PGEN_COLOR2	CSI1_PGEN_COLOR2	Go
0x33	CSI1_PGEN_COLOR3	CSI1_PGEN_COLOR3	Go

Table 8-212. PATGEN_AND_CSI-2_TRIM Registers (continued)

Address	Acronym	Register Name	Section
0x34	CSI1_PGEN_COLOR4	CSI1_PGEN_COLOR4	Go
0x35	CSI1_PGEN_COLOR5	CSI1_PGEN_COLOR5	Go
0x36	CSI1_PGEN_COLOR6	CSI1_PGEN_COLOR6	Go
0x37	CSI1_PGEN_COLOR7	CSI1_PGEN_COLOR7	Go
0x38	CSI1_PGEN_COLOR8	CSI1_PGEN_COLOR8	Go
0x39	CSI1_PGEN_COLOR9	CSI1_PGEN_COLOR9	Go
0x3A	CSI1_PGEN_COLOR10	CSI1_PGEN_COLOR10	Go
0x3B	CSI1_PGEN_COLOR11	CSI1_PGEN_COLOR11	Go
0x3C	CSI1_PGEN_COLOR12	CSI1_PGEN_COLOR12	Go
0x3D	CSI1_PGEN_COLOR13	CSI1_PGEN_COLOR13	Go
0x3E	CSI1_PGEN_COLOR14	CSI1_PGEN_COLOR14	Go
0x3F	CSI1_PGEN_COLOR15	CSI1_PGEN_COLOR15	Go
0x40	CSI0_TCK_PREP	CSI0_TCK_PREP	Go
0x41	CSI0_TCK_ZERO	CSI0_TCK_ZERO	Go
0x42	CSI0_TCK_TRAIL	CSI0_TCK_TRAIL	Go
0x43	CSI0_TCK_POST	CSI0_TCK_POST	Go
0x44	CSI0_THS_PREP	CSI0_THS_PREP	Go
0x45	CSI0_THS_ZERO	CSI0_THS_ZERO	Go
0x46	CSI0_THS_TRAIL	CSI0_THS_TRAIL	Go
0x47	CSI0_THS_EXIT	CSI0_THS_EXIT	Go
0x48	CSI0_TPLX	CSI0_TPLX	Go
0x49	CSI0_TRIM_TCK_PREP	CSI0_TRIM_TCK_PREP	Go
0x4A	CSI0_TRIM_TCK_ZERO	CSI0_TRIM_TCK_ZERO	Go
0x4B	CSI0_TRIM_TCK_TRAIL	CSI0_TRIM_TCK_TRAIL	Go
0x4C	CSI0_TRIM_TCK_POST	CSI0_TRIM_TCK_POST	Go
0x4D	CSI0_TRIM_THS_PREP	CSI0_TRIM_THS_PREP	Go
0x4E	CSI0_TRIM_THS_ZERO	CSI0_TRIM_THS_ZERO	Go
0x4F	CSI0_TRIM_THS_TRAIL	CSI0_TRIM_THS_TRAIL	Go
0x50	CSI0_TRIM_THS_EXIT	CSI0_TRIM_THS_EXIT	Go
0x51	CSI0_TRIM_TPLX	CSI0_TRIM_TPLX	Go
0x67	CSI1_TCK_ZERO	CSI1_TCK_ZERO	Go
0x68	CSI1_TCK_TRAIL	CSI1_TCK_TRAIL	Go
0x69	CSI1_TCK_POST	CSI1_TCK_POST	Go
0x6A	CSI1_THS_PREP	CSI1_THS_PREP	Go
0x6B	CSI1_THS_ZERO	CSI1_THS_ZERO	Go
0x6C	CSI1_THS_TRAIL	CSI1_THS_TRAIL	Go
0x6D	CSI1_THS_EXIT	CSI1_THS_EXIT	Go
0x6E	CSI1_TPLX	CSI1_TPLX	Go
0x6F	CSI1_TRIM_TCK_PREP	CSI1_TRIM_TCK_PREP	Go
0x70	CSI1_TRIM_TCK_ZERO	CSI1_TRIM_TCK_ZERO	Go
0x71	CSI1_TRIM_TCK_TRAIL	CSI1_TRIM_TCK_TRAIL	Go
0x72	CSI1_TRIM_TCK_POST	CSI1_TRIM_TCK_POST	Go
0x73	CSI1_TRIM_THS_PREP	CSI1_TRIM_THS_PREP	Go
0x74	CSI1_TRIM_THS_ZERO	CSI1_TRIM_THS_ZERO	Go
0x75	CSI1_TRIM_THS_TRAIL	CSI1_TRIM_THS_TRAIL	Go

Table 8-212. PATGEN_AND_CSI-2_TRIM Registers (continued)

Address	Acronym	Register Name	Section
0x76	CSI1_TRIM_THS_EXIT	CSI1_TRIM_THS_EXIT	Go
0x77	CSI1_TRIM_TPLX	CSI1_TRIM_TPLX	Go

8.6.2.1 PGEN_CTL Register (Address = 0x1) [Default = 0x00]PGEN_CTL is shown in [PGEN_CTL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-213. PGEN_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	PGEN_CSI_VC_MSB	R/W	0x0	CSI Virtual Channel Identifier MSBs This field controls the Most Significant two bits of the Virtual Channel Identifier field in the CSI packet header.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-1	RESERVED	R/W	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

8.6.2.2 PGEN_CFG Register (Address = 0x2) [Default = 0x33]PGEN_CFG is shown in [PGEN_CFG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-214. PGEN_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved
5-4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3-0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

8.6.2.3 PGEN_CSI_DI Register (Address = 0x3) [Default = 0x24]PGEN_CSI_DI is shown in [PGEN_CSI_DI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-215. PGEN_CSI_DI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier

Table 8-215. PGEN_CSI_DI Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

8.6.2.4 PGEN_LINE_SIZE1 Register (Address = 0x4) [Default = 0x07]PGEN_LINE_SIZE1 is shown in [PGEN_LINE_SIZE1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-216. PGEN_LINE_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

8.6.2.5 PGEN_LINE_SIZE0 Register (Address = 0x5) [Default = 0x80]PGEN_LINE_SIZE0 is shown in [PGEN_LINE_SIZE0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-217. PGEN_LINE_SIZE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

8.6.2.6 PGEN_BAR_SIZE1 Register (Address = 0x6) [Default = 0x00]PGEN_BAR_SIZE1 is shown in [PGEN_BAR_SIZE1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-218. PGEN_BAR_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

8.6.2.7 PGEN_BAR_SIZE0 Register (Address = 0x7) [Default = 0xF0]PGEN_BAR_SIZE0 is shown in [PGEN_BAR_SIZE0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-219. PGEN_BAR_SIZE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

8.6.2.8 PGEN_ACT_LPF1 Register (Address = 0x8) [Default = 0x01]

PGEN_ACT_LPF1 is shown in [PGEN_ACT_LPF1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-220. PGEN_ACT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

8.6.2.9 PGEN_ACT_LPF0 Register (Address = 0x9) [Default = 0xE0]

PGEN_ACT_LPF0 is shown in [PGEN_ACT_LPF0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-221. PGEN_ACT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

8.6.2.10 PGEN_TOT_LPF1 Register (Address = 0xA) [Default = 0x02]

PGEN_TOT_LPF1 is shown in [PGEN_TOT_LPF1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-222. PGEN_TOT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

8.6.2.11 PGEN_TOT_LPF0 Register (Address = 0xB) [Default = 0x0D]

PGEN_TOT_LPF0 is shown in [PGEN_TOT_LPF0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-223. PGEN_TOT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

8.6.2.12 PGEN_LINE_PD1 Register (Address = 0xC) [Default = 0x0C]

PGEN_LINE_PD1 is shown in [PGEN_LINE_PD1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-224. PGEN_LINE_PD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[15:8]	R/W	0xC	<p>Line Period</p> <p>Most significant byte of the line period.</p> <p>In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds.</p> <p>In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds.</p> <p>In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.</p>

8.6.2.13 PGEN_LINE_PD0 Register (Address = 0xD) [Default = 0x67]PGEN_LINE_PD0 is shown in [PGEN_LINE_PD0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-225. PGEN_LINE_PD0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[7:0]	R/W	0x67	<p>Line Period</p> <p>Least significant byte of the line period.</p> <p>In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds.</p> <p>In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds.</p> <p>In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.</p>

8.6.2.14 PGEN_VBP Register (Address = 0xE) [Default = 0x21]PGEN_VBP is shown in [PGEN_VBP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-226. PGEN_VBP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_VBP	R/W	0x21	<p>Vertical Back Porch</p> <p>This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.</p>

8.6.2.15 PGEN_VFP Register (Address = 0xF) [Default = 0x0A]PGEN_VFP is shown in [PGEN_VFP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-227. PGEN_VFP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_VFP	R/W	0xA	<p>Vertical Front Porch</p> <p>This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.</p>

8.6.2.16 PGEN_COLOR0 Register (Address = 0x10) [Default = 0xAA]PGEN_COLOR0 is shown in [PGEN_COLOR0 Register Field Descriptions](#).

[Return to the Summary Table.](#)

Table 8-228. PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

8.6.2.17 PGEN_COLOR1 Register (Address = 0x11) [Default = 0x33]

PGEN_COLOR1 is shown in [PGEN_COLOR1 Register Field Descriptions](#).

[Return to the Summary Table.](#)

Table 8-229. PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

8.6.2.18 PGEN_COLOR2 Register (Address = 0x12) [Default = 0xF0]

PGEN_COLOR2 is shown in [PGEN_COLOR2 Register Field Descriptions](#).

[Return to the Summary Table.](#)

Table 8-230. PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

8.6.2.19 PGEN_COLOR3 Register (Address = 0x13) [Default = 0x7F]

PGEN_COLOR3 is shown in [PGEN_COLOR3 Register Field Descriptions](#).

[Return to the Summary Table.](#)

Table 8-231. PGEN_COLOR3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

8.6.2.20 PGEN_COLOR4 Register (Address = 0x14) [Default = 0x55]

PGEN_COLOR4 is shown in [PGEN_COLOR4 Register Field Descriptions](#).

[Return to the Summary Table.](#)

Table 8-232. PGEN_COLOR4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

8.6.2.21 PGEN_COLOR5 Register (Address = 0x15) [Default = 0xCC]PGEN_COLOR5 is shown in [PGEN_COLOR5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-233. PGEN_COLOR5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

8.6.2.22 PGEN_COLOR6 Register (Address = 0x16) [Default = 0x0F]PGEN_COLOR6 is shown in [PGEN_COLOR6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-234. PGEN_COLOR6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

8.6.2.23 PGEN_COLOR7 Register (Address = 0x17) [Default = 0x80]PGEN_COLOR7 is shown in [PGEN_COLOR7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-235. PGEN_COLOR7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

8.6.2.24 PGEN_COLOR8 Register (Address = 0x18) [Default = 0x00]PGEN_COLOR8 is shown in [PGEN_COLOR8 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-236. PGEN_COLOR8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

8.6.2.25 PGEN_COLOR9 Register (Address = 0x19) [Default = 0x00]PGEN_COLOR9 is shown in [PGEN_COLOR9 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-237. PGEN_COLOR9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

8.6.2.26 PGEN_COLOR10 Register (Address = 0x1A) [Default = 0x00]PGEN_COLOR10 is shown in [PGEN_COLOR10 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-238. PGEN_COLOR10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

8.6.2.27 PGEN_COLOR11 Register (Address = 0x1B) [Default = 0x00]PGEN_COLOR11 is shown in [PGEN_COLOR11 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-239. PGEN_COLOR11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

8.6.2.28 PGEN_COLOR12 Register (Address = 0x1C) [Default = 0x00]PGEN_COLOR12 is shown in [PGEN_COLOR12 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-240. PGEN_COLOR12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

8.6.2.29 PGEN_COLOR13 Register (Address = 0x1D) [Default = 0x00]PGEN_COLOR13 is shown in [PGEN_COLOR13 Register Field Descriptions](#).

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Table 8-241. PGEN_COLOR13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

8.6.2.30 PGEN_COLOR14 Register (Address = 0x1E) [Default = 0x00]

PGEN_COLOR14 is shown in [PGEN_COLOR14 Register Field Descriptions](#).

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Table 8-242. PGEN_COLOR14 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

8.6.2.31 PGEN_COLOR15 Register (Address = 0x1F) [Default = 0x00]

PGEN_COLOR15 is shown in [PGEN_COLOR15 Register Field Descriptions](#).

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Table 8-243. PGEN_COLOR15 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern. THIS IS NOT CURRENTLY USED

8.6.2.32 CSI1_PGEN_CTL Register (Address = 0x21) [Default = 0x00]

CSI1_PGEN_CTL is shown in [CSI1_PGEN_CTL Register Field Descriptions](#).

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Table 8-244. CSI1_PGEN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	PGEN_CSI_VC_MSB	R/W	0x0	CSI Virtual Channel Identifier MSBs This field controls the Most Significant two bits of the Virtual Channel Identifier field in the CSI packet header.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R/W	0x0	Reserved
1	PGEN_SIMUL_CTL	R/W	0x0	CSI1 Simultaneous control Enable Setting this bit to 1 will enable simultaneous control of both CSI0 and CSI1 pattern generators. Register writes in the range of 0x00 to 0x1F will write to the equivalent registers in CSI1 (i.e. 0x20 to 0x3F). 1: Enable Simultaneous control 0: Disable Simultaneous control
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

8.6.2.33 CSI1_PGEN_CFG Register (Address = 0x22) [Default = 0x33]CSI1_PGEN_CFG is shown in [CSI1_PGEN_CFG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-245. CSI1_PGEN_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved
5-4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3-0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

8.6.2.34 CSI1_PGEN_CSI_DI Register (Address = 0x23) [Default = 0x24]CSI1_PGEN_CSI_DI is shown in [CSI1_PGEN_CSI_DI Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-246. CSI1_PGEN_CSI_DI Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5-0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

8.6.2.35 CSI1_PGEN_LINE_SIZE1 Register (Address = 0x24) [Default = 0x07]CSI1_PGEN_LINE_SIZE1 is shown in [CSI1_PGEN_LINE_SIZE1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-247. CSI1_PGEN_LINE_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

8.6.2.36 CSI1_PGEN_LINE_SIZE0 Register (Address = 0x25) [Default = 0x80]CSI1_PGEN_LINE_SIZE0 is shown in [CSI1_PGEN_LINE_SIZE0 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-248. CSI1_PGEN_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

8.6.2.37 CSI1_PGEN_BAR_SIZE1 Register (Address = 0x26) [Default = 0x00]CSI1_PGEN_BAR_SIZE1 is shown in [CSI1_PGEN_BAR_SIZE1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-249. CSI1_PGEN_BAR_SIZE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

8.6.2.38 CSI1_PGEN_BAR_SIZE0 Register (Address = 0x27) [Default = 0xF0]CSI1_PGEN_BAR_SIZE0 is shown in [CSI1_PGEN_BAR_SIZE0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-250. CSI1_PGEN_BAR_SIZE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

8.6.2.39 CSI1_PGEN_ACT_LPF1 Register (Address = 0x28) [Default = 0x01]CSI1_PGEN_ACT_LPF1 is shown in [CSI1_PGEN_ACT_LPF1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-251. CSI1_PGEN_ACT_LPF1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

8.6.2.40 CSI1_PGEN_ACT_LPF0 Register (Address = 0x29) [Default = 0xE0]CSI1_PGEN_ACT_LPF0 is shown in [CSI1_PGEN_ACT_LPF0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-252. CSI1_PGEN_ACT_LPF0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

8.6.2.41 CSI1_PGEN_TOT_LPF1 Register (Address = 0x2A) [Default = 0x02]CSI1_PGEN_TOT_LPF1 is shown in [CSI1_PGEN_TOT_LPF1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-253. CSI1_PGEN_TOT_LPF1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

8.6.2.42 CSI1_PGEN_TOT_LPF0 Register (Address = 0x2B) [Default = 0x0D]CSI1_PGEN_TOT_LPF0 is shown in [CSI1_PGEN_TOT_LPF0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-254. CSI1_PGEN_TOT_LPF0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

8.6.2.43 CSI1_PGEN_LINE_PD1 Register (Address = 0x2C) [Default = 0x0C]CSI1_PGEN_LINE_PD1 is shown in [CSI1_PGEN_LINE_PD1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-255. CSI1_PGEN_LINE_PD1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

8.6.2.44 CSI1_PGEN_LINE_PD0 Register (Address = 0x2D) [Default = 0x67]CSI1_PGEN_LINE_PD0 is shown in [CSI1_PGEN_LINE_PD0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-256. CSI1_PGEN_LINE_PD0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

8.6.2.45 CSI1_PGEN_VBP Register (Address = 0x2E) [Default = 0x21]

CSI1_PGEN_VBP is shown in [CSI1_PGEN_VBP Register Field Descriptions](#).

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Table 8-257. CSI1_PGEN_VBP Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

8.6.2.46 CSI1_PGEN_VFP Register (Address = 0x2F) [Default = 0x0A]

CSI1_PGEN_VFP is shown in [CSI1_PGEN_VFP Register Field Descriptions](#).

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Table 8-258. CSI1_PGEN_VFP Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

8.6.2.47 CSI1_PGEN_COLOR0 Register (Address = 0x30) [Default = 0xAA]

CSI1_PGEN_COLOR0 is shown in [CSI1_PGEN_COLOR0 Register Field Descriptions](#).

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Table 8-259. CSI1_PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

8.6.2.48 CSI1_PGEN_COLOR1 Register (Address = 0x31) [Default = 0x33]

CSI1_PGEN_COLOR1 is shown in [CSI1_PGEN_COLOR1 Register Field Descriptions](#).

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Table 8-260. CSI1_PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

8.6.2.49 CSI1_PGEN_COLOR2 Register (Address = 0x32) [Default = 0xF0]

CSI1_PGEN_COLOR2 is shown in [CSI1_PGEN_COLOR2 Register Field Descriptions](#).

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Table 8-261. CSI1_PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

8.6.2.50 CSI1_PGEN_COLOR3 Register (Address = 0x33) [Default = 0x7F]CSI1_PGEN_COLOR3 is shown in [CSI1_PGEN_COLOR3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-262. CSI1_PGEN_COLOR3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

8.6.2.51 CSI1_PGEN_COLOR4 Register (Address = 0x34) [Default = 0x55]CSI1_PGEN_COLOR4 is shown in [CSI1_PGEN_COLOR4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-263. CSI1_PGEN_COLOR4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

8.6.2.52 CSI1_PGEN_COLOR5 Register (Address = 0x35) [Default = 0xCC]CSI1_PGEN_COLOR5 is shown in [CSI1_PGEN_COLOR5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-264. CSI1_PGEN_COLOR5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

8.6.2.53 CSI1_PGEN_COLOR6 Register (Address = 0x36) [Default = 0x0F]CSI1_PGEN_COLOR6 is shown in [CSI1_PGEN_COLOR6 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-265. CSI1_PGEN_COLOR6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

8.6.2.54 CSI1_PGEN_COLOR7 Register (Address = 0x37) [Default = 0x80]CSI1_PGEN_COLOR7 is shown in [CSI1_PGEN_COLOR7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-266. CSI1_PGEN_COLOR7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

8.6.2.55 CSI1_PGEN_COLOR8 Register (Address = 0x38) [Default = 0x00]CSI1_PGEN_COLOR8 is shown in [CSI1_PGEN_COLOR8 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-267. CSI1_PGEN_COLOR8 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

8.6.2.56 CSI1_PGEN_COLOR9 Register (Address = 0x39) [Default = 0x00]CSI1_PGEN_COLOR9 is shown in [CSI1_PGEN_COLOR9 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-268. CSI1_PGEN_COLOR9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

8.6.2.57 CSI1_PGEN_COLOR10 Register (Address = 0x3A) [Default = 0x00]CSI1_PGEN_COLOR10 is shown in [CSI1_PGEN_COLOR10 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-269. CSI1_PGEN_COLOR10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

8.6.2.58 CSI1_PGEN_COLOR11 Register (Address = 0x3B) [Default = 0x00]CSI1_PGEN_COLOR11 is shown in [CSI1_PGEN_COLOR11 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-270. CSI1_PGEN_COLOR11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

8.6.2.59 CSI1_PGEN_COLOR12 Register (Address = 0x3C) [Default = 0x00]CSI1_PGEN_COLOR12 is shown in [CSI1_PGEN_COLOR12 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-271. CSI1_PGEN_COLOR12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

8.6.2.60 CSI1_PGEN_COLOR13 Register (Address = 0x3D) [Default = 0x00]CSI1_PGEN_COLOR13 is shown in [CSI1_PGEN_COLOR13 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-272. CSI1_PGEN_COLOR13 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

8.6.2.61 CSI1_PGEN_COLOR14 Register (Address = 0x3E) [Default = 0x00]CSI1_PGEN_COLOR14 is shown in [CSI1_PGEN_COLOR14 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-273. CSI1_PGEN_COLOR14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

8.6.2.62 CSI1_PGEN_COLOR15 Register (Address = 0x3F) [Default = 0x00]CSI1_PGEN_COLOR15 is shown in [CSI1_PGEN_COLOR15 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-274. CSI1_PGEN_COLOR15 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern. THIS IS NOT CURRENTLY USED

8.6.2.63 CSI0_TCK_PREP Register (Address = 0x40) [Default = 0x00]CSI0_TCK_PREP is shown in [CSI0_TCK_PREP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-275. CSI0_TCK_PREP Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter - DPHY Only 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6-0	MR_TCK_PREP	R/W	0x0	Tck-prep value - DPHY Only If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.64 CSI0_TCK_ZERO Register (Address = 0x41) [Default = 0x00]CSI0_TCK_ZERO is shown in [CSI0_TCK_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-276. CSI0_TCK_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter - DPHY Only 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6-0	MR_TCK_ZERO	R/W	0x0	Tck-zero value - DPHY Only If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.65 CSI0_TCK_TRAIL Register (Address = 0x42) [Default = 0x00]CSI0_TCK_TRAIL is shown in [CSI0_TCK_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-277. CSI0_TCK_TRAIL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter - DPHY Only 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6-0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value - DPHY Only If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.66 CSI0_TCK_POST Register (Address = 0x43) [Default = 0x00]CSI0_TCK_POST is shown in [CSI0_TCK_POST Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-278. CSI0_TCK_POST Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter - DPHY Only 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6-0	MR_TCK_POST	R/W	0x0	Tck-post value - DPHY Only If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.67 CSI0_THS_PREP Register (Address = 0x44) [Default = 0x00]

CSI0_THS_PREP is shown in [CSI0_THS_PREP Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-279. CSI0_THS_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6-0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write. THS_PREPARE ~= MR_THS_PREP / (D-PHY_RATE / 8)

8.6.2.68 CSI0_THS_ZERO Register (Address = 0x45) [Default = 0x00]

CSI0_THS_ZERO is shown in [CSI0_THS_ZERO Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-280. CSI0_THS_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6-0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.69 CSI0_THS_TRAIL Register (Address = 0x46) [Default = 0x00]

CSI0_THS_TRAIL is shown in [CSI0_THS_TRAIL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-281. CSI0_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register

Table 8-281. CSI0_THS_TRAIL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6-0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.70 CSI0_THS_EXIT Register (Address = 0x47) [Default = 0x00]CSI0_THS_EXIT is shown in [CSI0_THS_EXIT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-282. CSI0_THS_EXIT Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6-0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.71 CSI0_TPLX Register (Address = 0x48) [Default = 0x00]CSI0_TPLX is shown in [CSI0_TPLX Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-283. CSI0_TPLX Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6-0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write. TLPX ~ = MR_TPLX / (D-PHY_RATE / 8)

8.6.2.72 CSI0_TRIM_TCK_PREP Register (Address = 0x49) [Default = 0x00]CSI0_TRIM_TCK_PREP is shown in [CSI0_TRIM_TCK_PREP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-284. CSI0_TRIM_TCK_PREP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_PREP_50M	R/W	0x0	Tck-prep timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_PREP_100M	R/W	0x0	Tck-prep timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1

Table 8-284. CSI0_TRIM_TCK_PREP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1-0	TRIM_TCK_PREP_200M	R/W	0x0	Tck-prep timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.73 CSI0_TRIM_TCK_ZERO Register (Address = 0x4A) [Default = 0x00]CSI0_TRIM_TCK_ZERO is shown in [CSI0_TRIM_TCK_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-285. CSI0_TRIM_TCK_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_ZERO_50M	R/W	0x0	Tck-zero timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_ZERO_100M	R/W	0x0	Tck-zero timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_ZERO_200M	R/W	0x0	Tck-zero timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.74 CSI0_TRIM_TCK_TRAIL Register (Address = 0x4B) [Default = 0x00]CSI0_TRIM_TCK_TRAIL is shown in [CSI0_TRIM_TCK_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-286. CSI0_TRIM_TCK_TRAIL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_TRAIL_50M	R/W	0x0	Tck-trail timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_TRAIL_100M	R/W	0x0	Tck-trail timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_TRAIL_200M	R/W	0x0	Tck-trail timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.75 CSI0_TRIM_TCK_POST Register (Address = 0x4C) [Default = 0x00]CSI0_TRIM_TCK_POST is shown in [CSI0_TRIM_TCK_POST Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-287. CSI0_TRIM_TCK_POST Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_POST_50M	R/W	0x0	Tck-post timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_POST_100M	R/W	0x0	Tck-post timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_POST_200M	R/W	0x0	Tck-post timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.76 CSI0_TRIM_THS_PREP Register (Address = 0x4D) [Default = 0x00]CSI0_TRIM_THS_PREP is shown in [CSI0_TRIM_THS_PREP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-288. CSI0_TRIM_THS_PREP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_PREP_50M	R/W	0x0	ths-prep timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_PREP_100M	R/W	0x0	ths-prep timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_PREP_200M	R/W	0x0	ths-prep timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.77 CSI0_TRIM_THS_ZERO Register (Address = 0x4E) [Default = 0x00]CSI0_TRIM_THS_ZERO is shown in [CSI0_TRIM_THS_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-289. CSI0_TRIM_THS_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved

Table 8-289. CSI0_TRIM_THS_ZERO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-4	TRIM_THS_ZERO_50M	R/W	0x0	ths-zero timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_ZERO_100M	R/W	0x0	ths-zero timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_ZERO_200M	R/W	0x0	ths-zero timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.78 CSI0_TRIM_THS_TRAIL Register (Address = 0x4F) [Default = 0x00]CSI0_TRIM_THS_TRAIL is shown in [CSI0_TRIM_THS_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-290. CSI0_TRIM_THS_TRAIL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_TRAIL_50M	R/W	0x0	ths-trail timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_TRAIL_100M	R/W	0x0	ths-trail timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_TRAIL_200M	R/W	0x0	ths-trail timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.79 CSI0_TRIM_THS_EXIT Register (Address = 0x50) [Default = 0x00]CSI0_TRIM_THS_EXIT is shown in [CSI0_TRIM_THS_EXIT Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-291. CSI0_TRIM_THS_EXIT Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_EXIT_50M	R/W	0x0	ths-exit timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1

Table 8-291. CSI0_TRIM_THS_EXIT Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-2	TRIM_THS_EXIT_100M	R/W	0x0	ths-exit timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_EXIT_200M	R/W	0x0	ths-exit timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.80 CSI0_TRIM_TPLX Register (Address = 0x51) [Default = 0x00]CSI0_TRIM_TPLX is shown in [CSI0_TRIM_TPLX Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-292. CSI0_TRIM_TPLX Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TPLX_50M	R/W	0x0	tplx timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TPLX_100M	R/W	0x0	tplx timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TPLX_200M	R/W	0x0	tplx timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.81 CSI1_TCK_ZERO Register (Address = 0x67) [Default = 0x00]CSI1_TCK_ZERO is shown in [CSI1_TCK_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-293. CSI1_TCK_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6-0	MR_TCK_ZERO	R/W	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.82 CSI1_TCK_TRAIL Register (Address = 0x68) [Default = 0x00]CSI1_TCK_TRAIL is shown in [CSI1_TCK_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-294. CSI1_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6-0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.83 CSI1_TCK_POST Register (Address = 0x69) [Default = 0x00]CSI1_TCK_POST is shown in [CSI1_TCK_POST Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-295. CSI1_TCK_POST Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6-0	MR_TCK_POST	R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.84 CSI1_THS_PREP Register (Address = 0x6A) [Default = 0x00]CSI1_THS_PREP is shown in [CSI1_THS_PREP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-296. CSI1_THS_PREP Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6-0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write. THS_PREPARE ~= MR_THS_PREP / (D-PHY_RATE / 8)

8.6.2.85 CSI1_THS_ZERO Register (Address = 0x6B) [Default = 0x00]CSI1_THS_ZERO is shown in [CSI1_THS_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-297. CSI1_THS_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6-0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.86 CSI1_THS_TRAIL Register (Address = 0x6C) [Default = 0x00]

CSI1_THS_TRAIL is shown in [CSI1_THS_TRAIL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-298. CSI1_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6-0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.87 CSI1_THS_EXIT Register (Address = 0x6D) [Default = 0x00]

CSI1_THS_EXIT is shown in [CSI1_THS_EXIT Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-299. CSI1_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6-0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8.6.2.88 CSI1_TPLX Register (Address = 0x6E) [Default = 0x00]

CSI1_TPLX is shown in [CSI1_TPLX Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-300. CSI1_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6-0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write. $TPLX \approx MR_TPLX / (D-PHY_RATE / 8)$

8.6.2.89 CSI1_TRIM_TCK_PREP Register (Address = 0x6F) [Default = 0x00]

CSI1_TRIM_TCK_PREP is shown in [CSI1_TRIM_TCK_PREP Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-301. CSI1_TRIM_TCK_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved

Table 8-301. CSI1_TRIM_TCK_PREP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-4	TRIM_TCK_PREP_50M	R/W	0x0	Tck-prep timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_PREP_100M	R/W	0x0	Tck-prep timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_PREP_200M	R/W	0x0	Tck-prep timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.90 CSI1_TRIM_TCK_ZERO Register (Address = 0x70) [Default = 0x00]CSI1_TRIM_TCK_ZERO is shown in [CSI1_TRIM_TCK_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-302. CSI1_TRIM_TCK_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_ZERO_50M	R/W	0x0	Tck-zero timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_ZERO_100M	R/W	0x0	Tck-zero timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_ZERO_200M	R/W	0x0	Tck-zero timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.91 CSI1_TRIM_TCK_TRAIL Register (Address = 0x71) [Default = 0x00]CSI1_TRIM_TCK_TRAIL is shown in [CSI1_TRIM_TCK_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-303. CSI1_TRIM_TCK_TRAIL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_TRAIL_50M	R/W	0x0	Tck-trail timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1

Table 8-303. CSI1_TRIM_TCK_TRAIL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-2	TRIM_TCK_TRAIL_100M	R/W	0x0	Tck-trail timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_TRAIL_200M	R/W	0x0	Tck-trail timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.92 CSI1_TRIM_TCK_POST Register (Address = 0x72) [Default = 0x00]CSI1_TRIM_TCK_POST is shown in [CSI1_TRIM_TCK_POST Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-304. CSI1_TRIM_TCK_POST Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TCK_POST_50M	R/W	0x0	Tck-post timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TCK_POST_100M	R/W	0x0	Tck-post timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TCK_POST_200M	R/W	0x0	Tck-post timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.93 CSI1_TRIM_THS_PREP Register (Address = 0x73) [Default = 0x00]CSI1_TRIM_THS_PREP is shown in [CSI1_TRIM_THS_PREP Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-305. CSI1_TRIM_THS_PREP Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_PREP_50M	R/W	0x0	ths-prep timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_PREP_100M	R/W	0x0	ths-prep timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1

Table 8-305. CSI1_TRIM_THS_PREP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1-0	TRIM_THS_PREP_200M	R/W	0x0	ths-prep timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.94 CSI1_TRIM_THS_ZERO Register (Address = 0x74) [Default = 0x00]CSI1_TRIM_THS_ZERO is shown in [CSI1_TRIM_THS_ZERO Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-306. CSI1_TRIM_THS_ZERO Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_ZERO_50M	R/W	0x0	ths-zero timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_ZERO_100M	R/W	0x0	ths-zero timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_ZERO_200M	R/W	0x0	ths-zero timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.95 CSI1_TRIM_THS_TRAIL Register (Address = 0x75) [Default = 0x00]CSI1_TRIM_THS_TRAIL is shown in [CSI1_TRIM_THS_TRAIL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-307. CSI1_TRIM_THS_TRAIL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_TRAIL_50M	R/W	0x0	ths-trail timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_TRAIL_100M	R/W	0x0	ths-trail timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_TRAIL_200M	R/W	0x0	ths-trail timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.96 CSI1_TRIM_THS_EXIT Register (Address = 0x76) [Default = 0x00]

CSI1_TRIM_THS_EXIT is shown in [CSI1_TRIM_THS_EXIT Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-308. CSI1_TRIM_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_THS_EXIT_50M	R/W	0x0	ths-exit timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_THS_EXIT_100M	R/W	0x0	ths-exit timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_THS_EXIT_200M	R/W	0x0	ths-exit timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.2.97 CSI1_TRIM_TPLX Register (Address = 0x77) [Default = 0x00]

CSI1_TRIM_TPLX is shown in [CSI1_TRIM_TPLX Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-309. CSI1_TRIM_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5-4	TRIM_TPLX_50M	R/W	0x0	tplx timing trim for 50 MHz mode 00: +0 01: +1 10: +2 11: -1
3-2	TRIM_TPLX_100M	R/W	0x0	tplx timing trim for 100 MHz mode 00: +0 01: +1 10: +2 11: -1
1-0	TRIM_TPLX_200M	R/W	0x0	tplx timing trim for 200 MHz mode 00: +0 01: +1 10: +2 11: -1

8.6.3 FPD_RX_Port_Analog Registers

[FPD_RX_PORT_ANALOG Registers](#) lists the memory-mapped registers for the FPD_RX_Port_Analog registers. All register offset addresses not listed in [FPD_RX_PORT_ANALOG Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-310. FPD_RX_PORT_ANALOG Registers

Address	Acronym	Register Name	Section
0x0	REG_RX_0	REG_RX_0	Go
0x1	REG_RX_1	REG_RX_1	Go

Table 8-310. FPD_RX_PORT_ANALOG Registers (continued)

Address	Acronym	Register Name	Section
0x2	REG_RX_2	REG_RX_2	Go
0x3	REG_RX_3	REG_RX_3	Go
0x4	REG_RX_4	REG_RX_4	Go
0x1B	REG_RX_1B	REG_RX_1B	Go
0x21	SYSTEM_INIT_REG0	SYSTEM_INIT_REG0	Go
0x25	SYSTEM_INIT_REG1	SYSTEM_INIT_REG1	Go
0x27	AEQ_ALP_SEL6	AEQ_ALP_SEL6	Go
0x28	AEQ_ALP_SEL7	AEQ_ALP_SEL7	Go
0x2B	AEQ_ALP_SEL10	AEQ_ALP_SEL10	Go
0x2C	AEQ_ALP_SEL11	AEQ_ALP_SEL11	Go
0x2E	EQ_ADAPT_CTRL	EQ_ADAPT_CTRL	Go
0x84	EQ_CTRL_SEL_12	EQ_CTRL_SEL_12	Go
0x88	EQ_CTRL_SEL_16	EQ_CTRL_SEL_16	Go
0x89	EQ_CTRL_SEL_17	EQ_CTRL_SEL_17	Go
0x8A	EQ_CTRL_SEL_18	EQ_CTRL_SEL_18	Go
0x8B	EQ_CTRL_SEL_19	EQ_CTRL_SEL_19	Go
0x8D	EQ_CTRL_SEL_21	EQ_CTRL_SEL_21	Go
0x8E	EQ_CTRL_SEL_22	EQ_CTRL_SEL_22	Go
0x90	EQ_CTRL_SEL_24	EQ_CTRL_SEL_24	Go
0x91	EQ_CTRL_SEL_25	EQ_CTRL_SEL_25	Go
0x92	EQ_CTRL_SEL_26	EQ_CTRL_SEL_26	Go
0x93	EQ_CTRL_SEL_27	EQ_CTRL_SEL_27	Go
0x9E	EQ_CTRL_SEL_38	EQ_CTRL_SEL_38	Go
0xA0	FPD3_CDR_CTRL_SEL_0	FPD3_CDR_CTRL_SEL_0	Go
0xA1	FPD3_CDR_CTRL_SEL_1	FPD3_CDR_CTRL_SEL_1	Go
0xA4	FPD3_CDR_CTRL_SEL_4	FPD3_CDR_CTRL_SEL_4	Go
0xA6	FPD3_CDR_CTRL_SEL_6	FPD3_CDR_CTRL_SEL_6	Go
0xA7	FPD3_AEQ_CTRL_SEL_0	FPD3_AEQ_CTRL_SEL_0	Go
0xA8	FPD3_AEQ_CTRL_SEL_1	FPD3_AEQ_CTRL_SEL_1	Go
0xA9	FPD3_AEQ_CTRL_SEL_2	FPD3_AEQ_CTRL_SEL_2	Go
0xAA	FPD3_AEQ_CTRL_SEL_3	FPD3_AEQ_CTRL_SEL_3	Go
0xAB	FPD3_AEQ_CTRL_SEL_4	FPD3_AEQ_CTRL_SEL_4	Go
0xAE	FPD3_AEQ_CTRL_SEL_7	FPD3_AEQ_CTRL_SEL_7	Go
0xC1	FPD4_CTRL_SEL_17	FPD4_CTRL_SEL_17	Go
0xE0	EQ_CTRL_SEL_40	EQ_CTRL_SEL_40	Go
0xF0	EQ_OVERRIDE_CTRL	EQ_OVERRIDE_CTRL	Go

8.6.3.1 REG_RX_0 Register (Address = 0x0) [Default = 0xC0]REG_RX_0 is shown in [REG_RX_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-311. REG_RX_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved

Table 8-311. REG_RX_0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	FPD_RX_SEL_HF	R	0x1	Reads back the status of the equalizer mode. 1: equalizer in high frequency (HF) mode 0: equalizer in low frequency (LF) mode If REG_FPD_FUNC_MODE is set to 0 or 1, HF mode will be selected and this field will return a 1. Otherwise, HF mode will be disabled and this field will return 0. This field may be overwritten by using the FPD_RX_SEL_HF_OV and FPD_RX_SEL_HF_VAL controls in REG_RX_1.
5-3	RESERVED	R	0x0	Reserved
2-0	RESERVED	R	0x0	

8.6.3.2 REG_RX_1 Register (Address = 0x1) [Default = 0x00]REG_RX_1 is shown in [REG_RX_1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-312. REG_RX_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FPD_RX_SEL_HF_OV	R/W	0x0	RX_SEL_HF Override If this bit is set to 1, the FPD_RX_SEL_HF control will be set to the value in FPD_RX_SEL_HF_VAL. If set to 0, the FPD_RX_SEL_HF will be based on the REG_FPD_FUNC_MODE controls.
6	FPD_RX_SEL_HF_VAL	R/W	0x0	RX_SEL_HF Override Value If RX_SEL_HF_OV is set to a 1, the FPD_RX_SEL_HF control will be set to the value in this field.
5-3	RESERVED	R	0x0	Reserved
2-0	RESERVED	R	0x0	Reserved

8.6.3.3 REG_RX_2 Register (Address = 0x2) [Default = 0x00]REG_RX_2 is shown in [REG_RX_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-313. REG_RX_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	FPD_RX_GAIN1_TUNE	R	0x0	Receiver VGA - 1 gain tune
3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R	0x0	Reserved

8.6.3.4 REG_RX_3 Register (Address = 0x3) [Default = 0x00]REG_RX_3 is shown in [REG_RX_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-314. REG_RX_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	FPD_RX_GAIN2_TUNE	R	0x0	Receiver VGA - 2 gain tune
3-0	RESERVED	R/W	0x0	Reserved

8.6.3.5 REG_RX_4 Register (Address = 0x4) [Default = 0x00]REG_RX_4 is shown in [REG_RX_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-315. REG_RX_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	FPD_BC_DRIVER_NM_R	R/W	0x0	Back channel driver impedance control: write 0 when interacting with DS90UB971-Q1 Do not change value otherwise
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.3.6 REG_RX_1B Register (Address = 0x1B) [Default = 0x00]REG_RX_1B is shown in [REG_RX_1B Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-316. REG_RX_1B Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6-4	FPD_BC_DRV_PM_R	R/W	0x0	Back channel driver impedance control: write 0 when interacting with DS90UB971-Q1 Do not change value otherwise
3	FPD_BC_CMR_RES_INC	R/W	0x0	Back channel driver impedance control: 0: when interacting with DS90UB971-Q1 1: when interacting with DS90UB953-Q1/DS90UB933-Q1/ DS90UB913A-Q1
2-1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.3.7 SYSTEM_INIT_REG0 Register (Address = 0x21) [Default = 0x2D]SYSTEM_INIT_REG0 is shown in [SYSTEM_INIT_REG0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-317. SYSTEM_INIT_REG0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	REG_PAR_CNTR_THRE_SH	R/W	0x1	AEQ parity counter threshold
4-3	REG_BER_TIMER_THRE_SH	R/W	0x1	BER timer threshold (0s, 1minute, 2minutes, 4minutes)
2-1	LOCK_TIME_CTRL	R/W	0x2	FPD4 LOCK time control 0: 50us 1:100us 2:200us 3:400us
0	RESERVED	R/W	0x1	Reserved

8.6.3.8 SYSTEM_INIT_REG1 Register (Address = 0x25) [Default = 0x42]SYSTEM_INIT_REG1 is shown in [SYSTEM_INIT_REG1 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-318. SYSTEM_INIT_REG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SYS_CONFIG_RST	RH/W1S	0x0	System config reset
6-0	SYS_EQ_CONFIG	R/W	0x42	System EQ config setting

8.6.3.9 AEQ_ALP_SEL6 Register (Address = 0x27) [Default = 0x00]AEQ_ALP_SEL6 is shown in [AEQ_ALP_SEL6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-319. AEQ_ALP_SEL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	REG_START_EQ	R/W	0x0	Sets the starting/minimum setting for the AEQ in FPD4 CDR Mode.

8.6.3.10 AEQ_ALP_SEL7 Register (Address = 0x28) [Default = 0x23]AEQ_ALP_SEL7 is shown in [AEQ_ALP_SEL7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-320. AEQ_ALP_SEL7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	REG_END_EQ	R/W	0x23	Sets the ending/maximum setting for the AEQ in FPD4 CDR Mode.

8.6.3.11 AEQ_ALP_SEL10 Register (Address = 0x2B) [Default = 0x02]AEQ_ALP_SEL10 is shown in [AEQ_ALP_SEL10 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-321. AEQ_ALP_SEL10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	REG_EQ_OFFSET	R/W	0x2	Sets the offset for the AEQ after the initial AEQ search is done. This register is in 2's compliment format.

8.6.3.12 AEQ_ALP_SEL11 Register (Address = 0x2C) [Default = 0x00]AEQ_ALP_SEL11 is shown in [AEQ_ALP_SEL11 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-322. AEQ_ALP_SEL11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	EQ_BOOST	R	0x0	Reads back the adapted AEQ setting in FPD4 CDR Mode

8.6.3.13 EQ_ADAPT_CTRL Register (Address = 0x2E) [Default = 0x00]EQ_ADAPT_CTRL is shown in [EQ_ADAPT_CTRL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-323. EQ_ADAPT_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	EQ_ADAPT_EN	R/W	0x0	0 - VGA sweep/ Adaptation is disabled 1 - VGA sweep / Adaptation is enabled
5-0	RESERVED	R	0x0	Reserved

8.6.3.14 EQ_CTRL_SEL_12 Register (Address = 0x84) [Default = 0x00]EQ_CTRL_SEL_12 is shown in [EQ_CTRL_SEL_12 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-324. EQ_CTRL_SEL_12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	EQ_ADAPT1_OV_EN	R/W	0x0	Override enable for EQ
5-0	EQ_ADAPT1_OV	R/W	0x0	Override value for EQ_ADAPT1. Used when EQ_ADAPT1_OV_EN=1

8.6.3.15 EQ_CTRL_SEL_16 Register (Address = 0x88) [Default = 0x03]EQ_CTRL_SEL_16 is shown in [EQ_CTRL_SEL_16 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-325. EQ_CTRL_SEL_16 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R/W	0x0	Reserved
1-0	RATE_SEL	R/W	0x3	FPD CDR Settings: 00: RESERVED 01: Used with the divide by 2 setting: 3.775G mode AND divide by 4 setting: 1.8875G mode 10: RESERVED 11: Used with the divide by 1 setting: 7.55G mode

8.6.3.16 EQ_CTRL_SEL_17 Register (Address = 0x89) [Default = 0x00]EQ_CTRL_SEL_17 is shown in [EQ_CTRL_SEL_17 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-326. EQ_CTRL_SEL_17 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	REF_ADAPT_OV_EN	R/W	0x0	Override enable for REF_ADAPT0_OV and REF_ADAPT1_OV
6-0	REF_ADAPT0_OV	R/W	0x0	Override value for EQ REF_ADAPT0

8.6.3.17 EQ_CTRL_SEL_18 Register (Address = 0x8A) [Default = 0x00]EQ_CTRL_SEL_18 is shown in [EQ_CTRL_SEL_18 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-327. EQ_CTRL_SEL_18 Register Field Descriptions

Bit	Field	Type	Default	Description
7	TAKE_CH_SNAPSHOT	R/W	0x0	Write a 1 to this bit to take a channel (eq and cdr) snapshot, self clearing
6-0	REF_ADAPT1_OV	R/W	0x0	Override value for EQ REF_ADAPT1

8.6.3.18 EQ_CTRL_SEL_19 Register (Address = 0x8B) [Default = 0x30]EQ_CTRL_SEL_19 is shown in [EQ_CTRL_SEL_19 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-328. EQ_CTRL_SEL_19 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5-4	RESERVED	R/W	0x3	Reserved
3	RX_MARGIN_START	R/W	0x0	Start RX margin operation, self-clearing
2-1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.3.19 EQ_CTRL_SEL_21 Register (Address = 0x8D) [Default = 0x00]EQ_CTRL_SEL_21 is shown in [EQ_CTRL_SEL_21 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-329. EQ_CTRL_SEL_21 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EQ_SNAPSHOT[15:8]	R	0x0	EQ snapshot, upper byte

8.6.3.20 EQ_CTRL_SEL_22 Register (Address = 0x8E) [Default = 0x00]EQ_CTRL_SEL_22 is shown in [EQ_CTRL_SEL_22 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-330. EQ_CTRL_SEL_22 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EQ_SNAPSHOT[7:0]	R	0x0	EQ snapshot, lower byte

8.6.3.21 EQ_CTRL_SEL_24 Register (Address = 0x90) [Default = 0x00]EQ_CTRL_SEL_24 is shown in [EQ_CTRL_SEL_24 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-331. EQ_CTRL_SEL_24 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FPD4_AEQ_MODE	R/W	0x0	FPD4 AEQ Control: 0: Disable 1: Enable

Table 8-331. EQ_CTRL_SEL_24 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5-0	RX_MARGIN_ERROR_C NT[29:24]	R	0x0	Error counter for eye-opening-monitor diagnosis (bits[29:24])

8.6.3.22 EQ_CTRL_SEL_25 Register (Address = 0x91) [Default = 0x00]EQ_CTRL_SEL_25 is shown in [EQ_CTRL_SEL_25 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-332. EQ_CTRL_SEL_25 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	RX_MARGIN_ERROR_C NT[23:16]	R	0x0	Error counter for eye-opening-monitor diagnosis (bits[23:16])

8.6.3.23 EQ_CTRL_SEL_26 Register (Address = 0x92) [Default = 0x00]EQ_CTRL_SEL_26 is shown in [EQ_CTRL_SEL_26 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-333. EQ_CTRL_SEL_26 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	RX_MARGIN_ERROR_C NT[15:8]	R	0x0	Error counter for eye-opening-monitor diagnosis (bits[15:8])

8.6.3.24 EQ_CTRL_SEL_27 Register (Address = 0x93) [Default = 0x00]EQ_CTRL_SEL_27 is shown in [EQ_CTRL_SEL_27 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-334. EQ_CTRL_SEL_27 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	RX_MARGIN_ERROR_C NT[7:0]	R	0x0	Error counter for eye-opening-monitor diagnosis (bits[7:0])

8.6.3.25 EQ_CTRL_SEL_38 Register (Address = 0x9E) [Default = 0x20]EQ_CTRL_SEL_38 is shown in [EQ_CTRL_SEL_38 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-335. EQ_CTRL_SEL_38 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	FPD4_AEQ_TAP2_CTRL	R/W	0x1	FPD4 AEQ TAP2 Control: 1: Disable 0: Enable
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.3.26 FPD3_CDR_CTRL_SEL_0 Register (Address = 0xA0) [Default = 0x00]

FPD3_CDR_CTRL_SEL_0 is shown in [FPD3_CDR_CTRL_SEL_0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-336. FPD3_CDR_CTRL_SEL_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	FPD3_CDR_SEL_HS_40 BIT	R/W	0x0	FPD3 CDR 40-bit HS mode operation. 'Strap 1'b0 or 1'b1 If this bit is set to 1, the CDR will operate in 40-bit HS mode. This register control will be automatically set as follows when the REG_FPD_FUNC_MODE control is set to one of the FPD3 modes of operation: 010: FPD3 CSI Mode: 1 100: FPD3 DVP RAW12 HF: 0 101: FPD3 DVP RAW10: 0 110: FPD3 DVP RAW12 LF: 0 The value can be changed after the FPD mode has been set. At power-up, this value is set based on the MODE pin setting. If FPD3 CSI Mode is strapped, the value will be 1, otherwise the strapped value will be 0.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.3.27 FPD3_CDR_CTRL_SEL_1 Register (Address = 0xA1) [Default = 0x00]

FPD3_CDR_CTRL_SEL_1 is shown in [FPD3_CDR_CTRL_SEL_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-337. FPD3_CDR_CTRL_SEL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	FPD3_CDR_EN_DIV4	R/W	0x0	FPD3 CDR Divide-by-4 Enable If this bit is set to 1, the CDR divide-by-4 will be enabled. Otherwise, the circuit will divide-by-2. This register control will be automatically set as follows when the REG_FPD_FUNC_MODE control is set to one of the FPD3 modes of operation: 010: FPD3 CSI Mode: 0 100: FPD3 DVP RAW12 HF: 0 101: FPD3 DVP RAW10: 1 110: FPD3 DVP RAW12 LF: 1 The value can be changed after the FPD mode has been set.
5-0	RESERVED	R/W	0x0	Reserved

8.6.3.28 FPD3_CDR_CTRL_SEL_4 Register (Address = 0xA4) [Default = 0x84]

FPD3_CDR_CTRL_SEL_4 is shown in [FPD3_CDR_CTRL_SEL_4 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-338. FPD3_CDR_CTRL_SEL_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD3_CDR_LF_MODE	R/W	0x1	FPD3 CDR LF Mode control 'Strap 1'b0 or 1'b1 This register control will be automatically set as follows when the REG_FPD_FUNC_MODE control is set to one of the FPD3 modes of operation: 010: FPD3 CSI Mode: 0 100: FPD3 DVP RAW12 HF: 1 101: FPD3 DVP RAW10: 1 110: FPD3 DVP RAW12 LF: 1 The value can be changed after the FPD mode has been set. At power-up, this value is set based on the MODE pin setting. If FPD3 CSI Mode is strapped, the value will be 0, otherwise the strapped value will be 1.
6-5	RESERVED	R/W	0x0	Reserved
4-0	RESERVED	R/W	0x4	Reserved

8.6.3.29 FPD3_CDR_CTRL_SEL_6 Register (Address = 0xA6) [Default = 0x00]FPD3_CDR_CTRL_SEL_6 is shown in [FPD3_CDR_CTRL_SEL_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-339. FPD3_CDR_CTRL_SEL_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	0x0	Reserved
5	FPD_RX_LOOP_THRU_EN	R/W	0x0	1: enable loopthrough connectivity from EQ output to CMLOUT driver. Used in CMLOUT monitoring mode 0: disable
4	CMLRAW_EN	R/W	0x0	mux control for CMLOUT driver 0: selects retimed, synchronous data 1: selects EQ output data
3-2	RESERVED	R/W	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

8.6.3.30 FPD3_AEQ_CTRL_SEL_0 Register (Address = 0xA7) [Default = 0x94]FPD3_AEQ_CTRL_SEL_0 is shown in [FPD3_AEQ_CTRL_SEL_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-340. FPD3_AEQ_CTRL_SEL_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-5	RESERVED	R/W	0x4	Reserved
4	RESERVED	R/W	0x1	Reserved
3	AEQ_RESTART	RH/W1S	0x0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption will be restarted.
2	RESERVED	R/W	0x1	Reserved
1-0	RESERVED	R/W	0x0	Reserved

8.6.3.31 FPD3_AEQ_CTRL_SEL_1 Register (Address = 0xA8) [Default = 0x00]FPD3_AEQ_CTRL_SEL_1 is shown in [FPD3_AEQ_CTRL_SEL_1 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-341. FPD3_AEQ_CTRL_SEL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5-0	EQ_SELECT_FPD3	R	0x0	Reads back the adapted EQ setting in FPD3 CDR Mode Value doesn't include the AEQ offset from REG_EQ_OFFSET

8.6.3.32 FPD3_AEQ_CTRL_SEL_2 Register (Address = 0xA9) [Default = 0x23]FPD3_AEQ_CTRL_SEL_2 is shown in [FPD3_AEQ_CTRL_SEL_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-342. FPD3_AEQ_CTRL_SEL_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5-0	AEQ_MAX	R/W	0x23	Adaptive Equalizer Maximum value in FPD3 CDR Mode This register sets the maximum value for the Adaptive EQ algorithm.

8.6.3.33 FPD3_AEQ_CTRL_SEL_3 Register (Address = 0xAA) [Default = 0x00]FPD3_AEQ_CTRL_SEL_3 is shown in [FPD3_AEQ_CTRL_SEL_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-343. FPD3_AEQ_CTRL_SEL_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	AEQ_MIN	R/W	0x0	When AEQ floor is enabled by the SET_AEQ_FLOOR register bit, the starting/minimum setting is given by this register in FPD3 CDR Mode.

8.6.3.34 FPD3_AEQ_CTRL_SEL_4 Register (Address = 0xAB) [Default = 0x77]FPD3_AEQ_CTRL_SEL_4 is shown in [FPD3_AEQ_CTRL_SEL_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-344. FPD3_AEQ_CTRL_SEL_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	SFILTER_MAX	R/W	0x7	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-14 with 7 being the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. If AEQ_SFIL_ORDER is set in the AEQ_CTL register, the SFILTER_MAX value should not be set lower than 0x7
3-0	SFILTER_MIN	R/W	0x7	SFILTER Minimum setting This field controls the minimum SFILTER setting. Allowed values are 0-14, where 7 is the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. If AEQ_SFIL_ORDER is set in the AEQ_CTL register, the SFILTER_MIN value should not be set higher than 0x6

8.6.3.35 FPD3_AEQ_CTRL_SEL_7 Register (Address = 0xAE) [Default = 0x01]

FPD3_AEQ_CTRL_SEL_7 is shown in [FPD3_AEQ_CTRL_SEL_7 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-345. FPD3_AEQ_CTRL_SEL_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	AEQ_ERR_THRESH	R/W	0x1	AEQ Error Threshold (in FPD3 CDR Mode) This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.

8.6.3.36 FPD4_CTRL_SEL_17 Register (Address = 0xC1) [Default = 0x00]

FPD4_CTRL_SEL_17 is shown in [FPD4_CTRL_SEL_17 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-346. FPD4_CTRL_SEL_17 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R	0x0	Reserved
5-0	I_PHASE_ADJ	R/W	0x0	Used for phase adjustment during eye opening monitor diagnosis

8.6.3.37 EQ_CTRL_SEL_40 Register (Address = 0xE0) [Default = 0x00]

EQ_CTRL_SEL_40 is shown in [EQ_CTRL_SEL_40 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-347. EQ_CTRL_SEL_40 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EQ_TUNE_OV_EN	R/W	0x0	EQ Override Control 1: override EQ settings to the value of EQ_TUNE_OV 0: disable override
5-0	EQ_TUNE_OV	R/W	0x0	EQ setting when EQ_TUNE_OV_EN is set.

8.6.3.38 EQ_OVERRIDE_CTRL Register (Address = 0xF0) [Default = 0x40]

EQ_OVERRIDE_CTRL is shown in [EQ_OVERRIDE_CTRL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-348. EQ_OVERRIDE_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EQ_OVERRIDE_EN	R/W	0x1	VGA gain tune override enable
5	RESERVED	R/W	0x0	Reserved
4-0	RESERVED	R/W	0x0	Reserved

8.6.4 PLL_Ctrl Registers

[PLL_CTRL Registers](#) lists the memory-mapped registers for the PLL_Ctrl registers. All register offset addresses not listed in [PLL_CTRL Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-349. PLL_CTRL Registers

Address	Acronym	Register Name	Section
0x83	FPD_ANA_CTRL_SEL_83	FPD_ANA_CTRL_SEL_83	Go
0x84	FPD_ANA_CTRL_SEL_84	FPD_ANA_CTRL_SEL_84	Go
0x85	FPD_ANA_CTRL_SEL_85	FPD_ANA_CTRL_SEL_85	Go
0x87	FPD_ANA_CTRL_SEL_87	FPD_ANA_CTRL_SEL_87	Go
0x8A	FPD_ANA_CTRL_SEL_8A	FPD_ANA_CTRL_SEL_8A	Go
0xC0	FPD_REG_0	FPD_REG_0	Go
0xC2	FPD_REG_2	FPD_REG_2	Go
0xC4	FPD_REG_4	FPD_REG_4	Go
0xC6	FPD_REG_6	FPD_REG_6	Go

8.6.4.1 FPD_ANA_CTRL_SEL_83 Register (Address = 0x83) [Default = 0x00]FPD_ANA_CTRL_SEL_83 is shown in [FPD_ANA_CTRL_SEL_83 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-350. FPD_ANA_CTRL_SEL_83 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PLL_FPD_RX_NUM_MAS H[23:16]	R/W	0x0	RX PLL MASH Divider Setting (bit[23:16]): For 8.32 GHz, set to 0x66 For 7.55 GHz, set to 0x00

8.6.4.2 FPD_ANA_CTRL_SEL_84 Register (Address = 0x84) [Default = 0x00]FPD_ANA_CTRL_SEL_84 is shown in [FPD_ANA_CTRL_SEL_84 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-351. FPD_ANA_CTRL_SEL_84 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PLL_FPD_RX_NUM_MAS H[15:8]	R/W	0x0	RX PLL MASH Divider Setting (bit[15:8]): For 8.32 GHz, set to 0x66 For 7.55 GHz, set to 0x00

8.6.4.3 FPD_ANA_CTRL_SEL_85 Register (Address = 0x85) [Default = 0x00]FPD_ANA_CTRL_SEL_85 is shown in [FPD_ANA_CTRL_SEL_85 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-352. FPD_ANA_CTRL_SEL_85 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PLL_FPD_RX_NUM_MAS H[7:0]	R/W	0x0	RX PLL MASH Divider Setting (bit[7:0]): For 8.32 GHz, set to 0x66 For 7.55 GHz, set to 0x00

8.6.4.4 FPD_ANA_CTRL_SEL_87 Register (Address = 0x87) [Default = 0x97]FPD_ANA_CTRL_SEL_87 is shown in [FPD_ANA_CTRL_SEL_87 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-353. FPD_ANA_CTRL_SEL_87 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PLL_FPD_RX_NCOUN[7:0]	R/W	0x97	RX PLL Divider Setting For 8.32 GHz, set to 0xA6 For 7.55 GHz, set to 0x97

8.6.4.5 FPD_ANA_CTRL_SEL_8A Register (Address = 0x8A) [Default = 0x00]FPD_ANA_CTRL_SEL_8A is shown in [FPD_ANA_CTRL_SEL_8A Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-354. FPD_ANA_CTRL_SEL_8A Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6-4	PLL_FPD_RX_MASH_OR_DER	R/W	0x0	RX PLL MASH Divider Order For 8.32 GHz, set to 3'h1 For 7.55 GHz, set to 3'h0
3-0	RESERVED	R/W	0x0	Reserved

8.6.4.6 FPD_REG_0 Register (Address = 0xC0) [Default = 0x00]FPD_REG_0 is shown in [FPD_REG_0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-355. FPD_REG_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CH0_ALT_DIV4_EN	R/W	0x0	Divide by 4 for eye opening monitor mode 1: when DIV_IQ_SEL_DIV_CH0 set to 0x3, this bit enables divide by 4 operation 0: disable divider
6-5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.4.7 FPD_REG_2 Register (Address = 0xC2) [Default = 0x00]FPD_REG_2 is shown in [FPD_REG_2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-356. FPD_REG_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CH1_ALT_DIV4_EN	R/W	0x0	Divide by 4 for eye opening monitor mode 1: when DIV_IQ_SEL_DIV_CH1 set to 0x3, this bit enables divide by 4 operation 0: disable divider
6-5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.4.8 FPD_REG_4 Register (Address = 0xC4) [Default = 0x00]FPD_REG_4 is shown in [FPD_REG_4 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-357. FPD_REG_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CH2_ALT_DIV4_EN	R/W	0x0	Divide by 4 for eye opening monitor mode 1: when DIV_IQ_SEL_DIV_CH2 set to 0x3, this bit enables divide by 4 operation 0: disable divider
6-5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.4.9 FPD_REG_6 Register (Address = 0xC6) [Default = 0x00]

FPD_REG_6 is shown in [FPD_REG_6 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-358. FPD_REG_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CH3_ALT_DIV4_EN	R/W	0x0	Divide by 4 for eye opening monitor mode 1: when DIV_IQ_SEL_DIV_CH3 set to 0x3, this bit enables divide by 4 operation 0: disable divider
6-5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-0	RESERVED	R/W	0x0	Reserved

8.6.5 CSI2 Registers

[CSI2 Registers](#) lists the memory-mapped registers for the CSI2 registers. All register offset addresses not listed in [CSI2 Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-359. CSI2 Registers

Address	Acronym	Register Name	Section
0x92	CSIPLL_REG_1	CSIPLL_REG_1	Go

8.6.5.1 CSIPLL_REG_1 Register (Address = 0x92) [Default = 0x50]

CSIPLL_REG_1 is shown in [CSIPLL_REG_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-360. CSIPLL_REG_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	PLL_FB_DIV	R/W	0x1	Sets CSI PLL frequency per the equation: CSI PLL frequency= $(2^{\text{PLL_FB_DIV}}) * 25 \text{ MHz} * \text{CSI_PLL_DIVIDER} / (2^{\text{PLL_OUT_DIV}})$
5-4	PLL_OUT_DIV	R/W	0x1	Sets CSI PLL frequency per the equation: CSI PLL frequency= $(2^{\text{PLL_FB_DIV}}) * 25 \text{ MHz} * \text{CSI_PLL_DIVIDER} / (2^{\text{PLL_OUT_DIV}})$
3-0	RESERVED	R/W	0x0	Reserved

8.6.6 DIE_ID Registers

[DIE_ID Registers](#) lists the memory-mapped registers for the DIE_ID registers. All register offset addresses not listed in [DIE_ID Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-361. DIE_ID Registers

Address	Acronym	Register Name	Section
0x0	UNIQUE_ID_0	UNIQUE_ID_0	Go
0x1	UNIQUE_ID_1	UNIQUE_ID_1	Go
0x2	UNIQUE_ID_2	UNIQUE_ID_2	Go
0x3	UNIQUE_ID_3	UNIQUE_ID_3	Go
0x4	UNIQUE_ID_4	UNIQUE_ID_4	Go
0x5	UNIQUE_ID_5	UNIQUE_ID_5	Go
0x6	UNIQUE_ID_6	UNIQUE_ID_6	Go
0x7	UNIQUE_ID_7	UNIQUE_ID_7	Go
0x8	UNIQUE_ID_8	UNIQUE_ID_8	Go
0x9	UNIQUE_ID_9	UNIQUE_ID_9	Go
0x10	UNIQUE_ID_10	UNIQUE_ID_10	Go
0x11	UNIQUE_ID_11	UNIQUE_ID_11	Go
0x12	UNIQUE_ID_12	UNIQUE_ID_12	Go
0x13	UNIQUE_ID_13	UNIQUE_ID_13	Go
0x14	UNIQUE_ID_14	UNIQUE_ID_14	Go
0x15	UNIQUE_ID_15	UNIQUE_ID_15	Go

8.6.6.1 UNIQUE_ID_0 Register (Address = 0x0) [Default = 0x00]

UNIQUE_ID_0 is shown in [UNIQUE_ID_0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-362. UNIQUE_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_0	R	0x0	Unique DIE ID byte 0

8.6.6.2 UNIQUE_ID_1 Register (Address = 0x1) [Default = 0x00]

UNIQUE_ID_1 is shown in [UNIQUE_ID_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-363. UNIQUE_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_1	R	0x0	Unique DIE ID byte 1

8.6.6.3 UNIQUE_ID_2 Register (Address = 0x2) [Default = 0x00]

UNIQUE_ID_2 is shown in [UNIQUE_ID_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-364. UNIQUE_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_2	R	0x0	Unique DIE ID byte 2

8.6.6.4 UNIQUE_ID_3 Register (Address = 0x3) [Default = 0x00]UNIQUE_ID_3 is shown in [UNIQUE_ID_3 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-365. UNIQUE_ID_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_3	R	0x0	Unique DIE ID byte 3

8.6.6.5 UNIQUE_ID_4 Register (Address = 0x4) [Default = 0x00]UNIQUE_ID_4 is shown in [UNIQUE_ID_4 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-366. UNIQUE_ID_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_4	R	0x0	Unique DIE ID byte 4

8.6.6.6 UNIQUE_ID_5 Register (Address = 0x5) [Default = 0x00]UNIQUE_ID_5 is shown in [UNIQUE_ID_5 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-367. UNIQUE_ID_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_5	R	0x0	Unique DIE ID byte 5

8.6.6.7 UNIQUE_ID_6 Register (Address = 0x6) [Default = 0x00]UNIQUE_ID_6 is shown in [UNIQUE_ID_6 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-368. UNIQUE_ID_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_6	R	0x0	Unique DIE ID byte 6

8.6.6.8 UNIQUE_ID_7 Register (Address = 0x7) [Default = 0x00]UNIQUE_ID_7 is shown in [UNIQUE_ID_7 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-369. UNIQUE_ID_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_7	R	0x0	Unique DIE ID byte 7

8.6.6.9 UNIQUE_ID_8 Register (Address = 0x8) [Default = 0x00]UNIQUE_ID_8 is shown in [UNIQUE_ID_8 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-370. UNIQUE_ID_8 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_8	R	0x0	Unique DIE ID byte 8

8.6.6.10 UNIQUE_ID_9 Register (Address = 0x9) [Default = 0x00]UNIQUE_ID_9 is shown in [UNIQUE_ID_9 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-371. UNIQUE_ID_9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_9	R	0x0	Unique DIE ID byte 9

8.6.6.11 UNIQUE_ID_10 Register (Address = 0x10) [Default = 0x00]UNIQUE_ID_10 is shown in [UNIQUE_ID_10 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-372. UNIQUE_ID_10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_10	R	0x0	Unique DIE ID byte 10

8.6.6.12 UNIQUE_ID_11 Register (Address = 0x11) [Default = 0x00]UNIQUE_ID_11 is shown in [UNIQUE_ID_11 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-373. UNIQUE_ID_11 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_11	R	0x0	Unique DIE ID byte 11

8.6.6.13 UNIQUE_ID_12 Register (Address = 0x12) [Default = 0x00]UNIQUE_ID_12 is shown in [UNIQUE_ID_12 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-374. UNIQUE_ID_12 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_12	R	0x0	Unique DIE ID byte 12

8.6.6.14 UNIQUE_ID_13 Register (Address = 0x13) [Default = 0x00]UNIQUE_ID_13 is shown in [UNIQUE_ID_13 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-375. UNIQUE_ID_13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_13	R	0x0	Unique DIE ID byte 13

8.6.6.15 UNIQUE_ID_14 Register (Address = 0x14) [Default = 0x00]UNIQUE_ID_14 is shown in [UNIQUE_ID_14 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-376. UNIQUE_ID_14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_14	R	0x0	Unique DIE ID byte 14

8.6.6.16 UNIQUE_ID_15 Register (Address = 0x15) [Default = 0x00]UNIQUE_ID_15 is shown in [UNIQUE_ID_15 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-377. UNIQUE_ID_15 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	UNIQUE_ID_15	R	0x0	Unique DIE ID byte 15

8.6.7 SAR_ADC Registers

[SAR_ADC Registers](#) lists the memory-mapped registers for the SAR_ADC registers. All register offset addresses not listed in [SAR_ADC Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-378. SAR_ADC Registers

Address	Acronym	Register Name	Section
0x4	SAR_ADC_CLK_SAMPLE_SEL	SAR_ADC_CLK_SAMPLE_SEL	Go
0x7	SAR_ADC_INPUT_EN_LSB	SAR_ADC_INPUT_EN_LSB	Go
0x8	SAR_ADC_INPUT_EN_MSB		Go
0xD	ADC_CTRL_MODE0	ADC_CTRL_MODE0	Go
0x13	TEMP_FINAL	TEMP_FINAL	Go
0x15	IV0_FINAL	IV0_FINAL	Go
0x16	IV1_FINAL	IV1_FINAL	Go
0x17	IV2_FINAL	IV2_FINAL	Go
0x18	IV3_FINAL	IV3_FINAL	Go
0x1B	EXT_VOL0_FINAL	EXT_VOL0_FINAL	Go
0x1C	EXT_VOL1_FINAL	EXT_VOL1_FINAL	Go
0x1D	LINE_FAULT0_FINAL	LINE_FAULT0_FINAL	Go
0x1E	LINE_FAULT1_FINAL	LINE_FAULT1_FINAL	Go
0x1F	LINE_FAULT2_FINAL	LINE_FAULT2_FINAL	Go
0x20	LINE_FAULT3_FINAL	LINE_FAULT3_FINAL	Go
0x23	INT_STATUS LSB_LOW	INT_STATUS LSB_LOW	Go
0x24	INT_STATUS MSB_LOW	INT_STATUS MSB_LOW	Go
0x25	INT_STATUS LSB_HIGH	INT_STATUS LSB_HIGH	Go
0x26	INT_STATUS MSB_HIGH	INT_STATUS MSB_HIGH	Go
0x27	INT_LINE_FAULT0_M0	INT_LINE_FAULT0_M0	Go

Table 8-378. SAR_ADC Registers (continued)

Address	Acronym	Register Name	Section
0x28	INT_LINE_FAULT1_M0	INT_LINE_FAULT1_M0	Go
0x2F	INT_LINE_FAULT_UNDEG	INT_LINE_FAULT_UNDEG	Go
0x30	INT_LINE_FAULT_SATURATE	INT_LINE_FAULT_SATURATE	Go
0x33	TEMP_HIGH	TEMP_HIGH	Go
0x34	TEMP_LOW	TEMP_LOW	Go
0x35	TEMP_ADC_OFFSET	TEMP_ADC_OFFSET	Go
0x39	IV0_HIGH	IV0_HIGH	Go
0x3A	IV0_LOW	IV0_LOW	Go
0x3B	IV0_ADC_OFFSET	IV0_ADC_OFFSET	Go
0x3C	IV1_HIGH	IV1_HIGH	Go
0x3D	IV1_LOW	IV1_LOW	Go
0x3E	IV1_ADC_OFFSET	IV1_ADC_OFFSET	Go
0x3F	IV2_HIGH	IV2_HIGH	Go
0x40	IV2_LOW	IV2_LOW	Go
0x41	IV2_ADC_OFFSET	IV2_ADC_OFFSET	Go
0x42	IV3_HIGH	IV3_HIGH	Go
0x43	IV3_LOW	IV3_LOW	Go
0x44	IV3_ADC_OFFSET	IV3_ADC_OFFSET	Go
0x4B	TEMP_IV_MASK	TEMP_IV_MASK	Go
0x4C	EXT_VOL0_HIGH	EXT_VOL0_HIGH	Go
0x4D	EXT_VOL0_LOW	EXT_VOL0_LOW	Go
0x4E	EXT_VOL0_ADC_OFFSET	EXT_VOL0_ADC_OFFSET	Go
0x4F	EXT_VOL1_HIGH	EXT_VOL1_HIGH	Go
0x50	EXT_VOL1_LOW	EXT_VOL1_LOW	Go
0x51	EXT_VOL1_ADC_OFFSET	EXT_VOL1_ADC_OFFSET	Go
0x52	EXT_VOL_MASK	EXT_VOL_MASK	Go
0x53	LINE_FAULT0_THRESH_0_HI_M0	LINE_FAULT0_THRESH_0_HI_M0	Go
0x54	LINE_FAULT0_THRESH_0_LO_M0	LINE_FAULT0_THRESH_0_LO_M0	Go
0x55	LINE_FAULT0_THRESH_1_HI_M0	LINE_FAULT0_THRESH_1_HI_M0	Go
0x56	LINE_FAULT0_THRESH_1_LO_M0	LINE_FAULT0_THRESH_1_LO_M0	Go
0x57	LINE_FAULT0_THRESH_2_HI_M0	LINE_FAULT0_THRESH_2_HI_M0	Go
0x58	LINE_FAULT0_THRESH_2_LO_M0	LINE_FAULT0_THRESH_2_LO_M0	Go
0x59	LINE_FAULT0_THRESH_3_HI_M0	LINE_FAULT0_THRESH_3_HI_M0	Go
0x5A	LINE_FAULT0_THRESH_3_LO_M0	LINE_FAULT0_THRESH_3_LO_M0	Go
0x5B	LINE_FAULT0_THRESH_4_HI_M0	LINE_FAULT0_THRESH_4_HI_M0	Go
0x5C	LINE_FAULT0_THRESH_4_LO_M0	LINE_FAULT0_THRESH_4_LO_M0	Go
0x5D	LINE_FAULT0_THRESH_5_HI_M0	LINE_FAULT0_THRESH_5_HI_M0	Go

Table 8-378. SAR_ADC Registers (continued)

Address	Acronym	Register Name	Section
0x5E	LINE_FAULT0_THRESH_5_LO_M0	LINE_FAULT0_THRESH_5_LO_M0	Go
0x5F	LINE_FAULT0_THRESH_6_HI_M0	LINE_FAULT0_THRESH_6_HI_M0	Go
0x60	LINE_FAULT0_THRESH_6_LO_M0	LINE_FAULT0_THRESH_6_LO_M0	Go
0x61	LINE_FAULT0_THRESH_7_HI_M0	LINE_FAULT0_THRESH_7_HI_M0	Go
0x62	LINE_FAULT0_THRESH_7_LO_M0	LINE_FAULT0_THRESH_7_LO_M0	Go
0x63	LINE_FAULT0_THRESH_MASK_M0	LINE_FAULT0_THRESH_MASK_M0	Go
0x64	LINE_FAULT0_ADC_OFFSET_M0	LINE_FAULT0_ADC_OFFSET_M0	Go
0x65	LINE_FAULT1_THRESH_0_HI_M0	LINE_FAULT1_THRESH_0_HI_M0	Go
0x66	LINE_FAULT1_THRESH_0_LO_M0	LINE_FAULT1_THRESH_0_LO_M0	Go
0x67	LINE_FAULT1_THRESH_1_HI_M0	LINE_FAULT1_THRESH_1_HI_M0	Go
0x68	LINE_FAULT1_THRESH_1_LO_M0	LINE_FAULT1_THRESH_1_LO_M0	Go
0x69	LINE_FAULT1_THRESH_2_HI_M0	LINE_FAULT1_THRESH_2_HI_M0	Go
0x6A	LINE_FAULT1_THRESH_2_LO_M0	LINE_FAULT1_THRESH_2_LO_M0	Go
0x6B	LINE_FAULT1_THRESH_3_HI_M0	LINE_FAULT1_THRESH_3_HI_M0	Go
0x6C	LINE_FAULT1_THRESH_3_LO_M0	LINE_FAULT1_THRESH_3_LO_M0	Go
0x6D	LINE_FAULT1_THRESH_4_HI_M0	LINE_FAULT1_THRESH_4_HI_M0	Go
0x6E	LINE_FAULT1_THRESH_4_LO_M0	LINE_FAULT1_THRESH_4_LO_M0	Go
0x6F	LINE_FAULT1_THRESH_5_HI_M0	LINE_FAULT1_THRESH_5_HI_M0	Go
0x70	LINE_FAULT1_THRESH_5_LO_M0	LINE_FAULT1_THRESH_5_LO_M0	Go
0x71	LINE_FAULT1_THRESH_6_HI_M0	LINE_FAULT1_THRESH_6_HI_M0	Go
0x72	LINE_FAULT1_THRESH_6_LO_M0	LINE_FAULT1_THRESH_6_LO_M0	Go
0x73	LINE_FAULT1_THRESH_7_HI_M0	LINE_FAULT1_THRESH_7_HI_M0	Go
0x74	LINE_FAULT1_THRESH_7_LO_M0	LINE_FAULT1_THRESH_7_LO_M0	Go
0x75	LINE_FAULT1_THRESH_MASK_M0	LINE_FAULT1_THRESH_MASK_M0	Go
0x76	LINE_FAULT1_ADC_OFFSET_M0	LINE_FAULT1_ADC_OFFSET_M0	Go
0x77	LINE_FAULT2_THRESH_0_HI_M0	LINE_FAULT2_THRESH_0_HI_M0	Go
0x78	LINE_FAULT2_THRESH_0_LO_M0	LINE_FAULT2_THRESH_0_LO_M0	Go

Table 8-378. SAR_ADC Registers (continued)

Address	Acronym	Register Name	Section
0x79	LINE_FAULT2_THRESH_1_HI_M0	LINE_FAULT2_THRESH_1_HI_M0	Go
0x7A	LINE_FAULT2_THRESH_1_LO_M0	LINE_FAULT2_THRESH_1_LO_M0	Go
0x7B	LINE_FAULT2_THRESH_2_HI_M0	LINE_FAULT2_THRESH_2_HI_M0	Go
0x7C	LINE_FAULT2_THRESH_2_LO_M0	LINE_FAULT2_THRESH_2_LO_M0	Go
0x7D	LINE_FAULT2_THRESH_3_HI_M0	LINE_FAULT2_THRESH_3_HI_M0	Go
0x7E	LINE_FAULT2_THRESH_3_LO_M0	LINE_FAULT2_THRESH_3_LO_M0	Go
0x7F	LINE_FAULT2_THRESH_4_HI_M0	LINE_FAULT2_THRESH_4_HI_M0	Go
0x80	LINE_FAULT2_THRESH_4_LO_M0	LINE_FAULT2_THRESH_4_LO_M0	Go
0x81	LINE_FAULT2_THRESH_5_HI_M0	LINE_FAULT2_THRESH_5_HI_M0	Go
0x82	LINE_FAULT2_THRESH_5_LO_M0	LINE_FAULT2_THRESH_5_LO_M0	Go
0x83	LINE_FAULT2_THRESH_6_HI_M0	LINE_FAULT2_THRESH_6_HI_M0	Go
0x84	LINE_FAULT2_THRESH_6_LO_M0	LINE_FAULT2_THRESH_6_LO_M0	Go
0x85	LINE_FAULT2_THRESH_7_HI_M0	LINE_FAULT2_THRESH_7_HI_M0	Go
0x86	LINE_FAULT2_THRESH_7_LO_M0	LINE_FAULT2_THRESH_7_LO_M0	Go
0x87	LINE_FAULT2_THRESH_MASK_M0	LINE_FAULT2_THRESH_MASK_M0	Go
0x88	LINE_FAULT2_ADC_OFFSET_M0	LINE_FAULT2_ADC_OFFSET_M0	Go
0x89	LINE_FAULT3_THRESH_0_HI_M0	LINE_FAULT3_THRESH_0_HI_M0	Go
0x8A	LINE_FAULT3_THRESH_0_LO_M0	LINE_FAULT3_THRESH_0_LO_M0	Go
0x8B	LINE_FAULT3_THRESH_1_HI_M0	LINE_FAULT3_THRESH_1_HI_M0	Go
0x8C	LINE_FAULT3_THRESH_1_LO_M0	LINE_FAULT3_THRESH_1_LO_M0	Go
0x8D	LINE_FAULT3_THRESH_2_HI_M0	LINE_FAULT3_THRESH_2_HI_M0	Go
0x8E	LINE_FAULT3_THRESH_2_LO_M0	LINE_FAULT3_THRESH_2_LO_M0	Go
0x8F	LINE_FAULT3_THRESH_3_HI_M0	LINE_FAULT3_THRESH_3_HI_M0	Go
0x90	LINE_FAULT3_THRESH_3_LO_M0	LINE_FAULT3_THRESH_3_LO_M0	Go
0x91	LINE_FAULT3_THRESH_4_HI_M0	LINE_FAULT3_THRESH_4_HI_M0	Go
0x92	LINE_FAULT3_THRESH_4_LO_M0	LINE_FAULT3_THRESH_4_LO_M0	Go
0x93	LINE_FAULT3_THRESH_5_HI_M0	LINE_FAULT3_THRESH_5_HI_M0	Go

Table 8-378. SAR_ADC Registers (continued)

Address	Acronym	Register Name	Section
0x94	LINE_FAULT3_THRESH_5_LO_M0	LINE_FAULT3_THRESH_5_LO_M0	Go
0x95	LINE_FAULT3_THRESH_6_HI_M0	LINE_FAULT3_THRESH_6_HI_M0	Go
0x96	LINE_FAULT3_THRESH_6_LO_M0	LINE_FAULT3_THRESH_6_LO_M0	Go
0x97	LINE_FAULT3_THRESH_7_HI_M0	LINE_FAULT3_THRESH_7_HI_M0	Go
0x98	LINE_FAULT3_THRESH_7_LO_M0	LINE_FAULT3_THRESH_7_LO_M0	Go
0x99	LINE_FAULT3_THRESH_MASK_M0	LINE_FAULT3_THRESH_MASK_M0	Go
0x9A	LINE_FAULT3_ADC_OFFSET_M0	LINE_FAULT3_ADC_OFFSET_M0	Go
0xE5	ADC_OFFSET_POL0	ADC_OFFSET_POL0	Go
0xE6	ADC_OFFSET_POL1	ADC_OFFSET_POL1	Go
0xE7	ADC_OFFSET_POL2	ADC_OFFSET_POL2	Go

8.6.7.1 SAR_ADC_CLK_SAMPLE_SEL Register (Address = 0x4) [Default = 0xD0]SAR_ADC_CLK_SAMPLE_SEL is shown in [SAR_ADC_CLK_SAMPLE_SEL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-379. SAR_ADC_CLK_SAMPLE_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	SAR_ADC_AVERAGING_SEL	R/W	0x3	Moving average sel 0: no avg 1: 2 samples 2: 4 samples 3: 8 samples
5-4	SAR_ADC_CTRL_CLK_DIV	R/W	0x1	Clock divider 0: 25Mhz 1: 12.5 Mhz 2: 8.33 Mhz 3: 6.25 Mhz //default 12.5, will be divided by extra 32 (different reg control) and need 10 cycle to get 8b, 12.5MHz/32/10= 39KHz sampling rate
3-0	RESERVED	R	0x0	Reserved

8.6.7.2 SAR_ADC_INPUT_EN_LSB Register (Address = 0x7) [Default = 0x3D]SAR_ADC_INPUT_EN_LSB is shown in [SAR_ADC_INPUT_EN_LSB Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-380. SAR_ADC_INPUT_EN_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SAR_ADC_INPUT_EN_LSB	R/W	0x3D	Enables for sar ADC and selects which inputs to sample SAR_ADC_INPUT_EN[0]= TEMP SAR_ADC_INPUT_EN[1]= RESERVED SAR_ADC_INPUT_EN[2]= IV1 (VDD18_FPD3) SAR_ADC_INPUT_EN[3]= IV2 (VDD18_P) SAR_ADC_INPUT_EN[4]= IV3 (VDD11_FPD23) SAR_ADC_INPUT_EN[5]= IV4 (VDD11L) SAR_ADC_INPUT_EN[6]= RESERVED SAR_ADC_INPUT_EN[7]= RESERVED

8.6.7.3 SAR_ADC_INPUT_EN_MSB Register (Address = 0x8) [Default = 0x00]SAR_ADC_INPUT_EN_MSB is shown in [SAR_ADC_INPUT_EN_MSB Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-381. SAR_ADC_INPUT_EN_MSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	SAR_ADC_INPUT_EN_MSB	R/W	0x0	Enable for sar ADC and selects which inputs to sample SAR_ADC_INPUT_EN[0]= EXT_VOL0 (GPIO_0) SAR_ADC_INPUT_EN[1]= EXT_VOL1 (GPIO_1) SAR_ADC_INPUT_EN[2]= LINE_FAULT0 (GPIO_2) SAR_ADC_INPUT_EN[3]= LINE_FAULT1 (GPIO_5) SAR_ADC_INPUT_EN[4]= LINE_FAULT2 (GPIO_6) SAR_ADC_INPUT_EN[5]= LINE_FAULT3 (GPIO_7) SAR_ADC_INPUT_EN[6]= RESERVED SAR_ADC_INPUT_EN[7]= RESERVED

8.6.7.4 ADC_CTRL_MODE0 Register (Address = 0xD) [Default = 0x80]ADC_CTRL_MODE0 is shown in [ADC_CTRL_MODE0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-382. ADC_CTRL_MODE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ADC_DISABLE	R/W	0x1	Setting 1 disables the ADC controller
6	RESERVED	R/W	0x0	Reserved
5-3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R	0x0	Reserved

8.6.7.5 TEMP_FINAL Register (Address = 0x13) [Default = 0x00]TEMP_FINAL is shown in [TEMP_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-383. TEMP_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_FINAL	R	0x0	Holds ADC value for TEMP_FINAL

8.6.7.6 IV0_FINAL Register (Address = 0x15) [Default = 0x00]IV0_FINAL is shown in [IV0_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-384. IV0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IV0_FINAL	R	0x0	Holds ADC value for IV0_FINAL

8.6.7.7 IV1_FINAL Register (Address = 0x16) [Default = 0x00]IV1_FINAL is shown in [IV1_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-385. IV1_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_FINAL	R	0x0	Holds ADC value for IV1_FINAL

8.6.7.8 IV2_FINAL Register (Address = 0x17) [Default = 0x00]IV2_FINAL is shown in [IV2_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-386. IV2_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV2_FINAL	R	0x0	Holds ADC value for IV2_FINAL

8.6.7.9 IV3_FINAL Register (Address = 0x18) [Default = 0x00]IV3_FINAL is shown in [IV3_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-387. IV3_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV3_FINAL	R	0x0	Holds ADC value for IV3_FINAL

8.6.7.10 EXT_VOL0_FINAL Register (Address = 0x1B) [Default = 0x00]EXT_VOL0_FINAL is shown in [EXT_VOL0_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-388. EXT_VOL0_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_FINAL	R	0x0	Holds ADC value for EXT_VOL0_FINAL

8.6.7.11 EXT_VOL1_FINAL Register (Address = 0x1C) [Default = 0x00]EXT_VOL1_FINAL is shown in [EXT_VOL1_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-389. EXT_VOL1_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_FINAL	R	0x0	Holds ADC value for EXT_VOL1_FINAL

8.6.7.12 LINE_FAULT0_FINAL Register (Address = 0x1D) [Default = 0x00]LINE_FAULT0_FINAL is shown in [LINE_FAULT0_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-390. LINE_FAULT0_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_FINAL	R	0x0	Holds ADC value for LINE_FAULT0_FINAL

8.6.7.13 LINE_FAULT1_FINAL Register (Address = 0x1E) [Default = 0x00]LINE_FAULT1_FINAL is shown in [LINE_FAULT1_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-391. LINE_FAULT1_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_FINAL	R	0x0	Holds ADC value for LINE_FAULT1_FINAL

8.6.7.14 LINE_FAULT2_FINAL Register (Address = 0x1F) [Default = 0x00]LINE_FAULT2_FINAL is shown in [LINE_FAULT2_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-392. LINE_FAULT2_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_FINAL	R	0x0	Holds ADC value for LINE_FAULT2_FINAL

8.6.7.15 LINE_FAULT3_FINAL Register (Address = 0x20) [Default = 0x00]LINE_FAULT3_FINAL is shown in [LINE_FAULT3_FINAL Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-393. LINE_FAULT3_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_FINAL	R/W	0x0	Holds ADC value for LINE_FAULT3_FINAL

8.6.7.16 INT_STATUS_LSB_LOW Register (Address = 0x23) [Default = 0x00]INT_STATUS_LSB_LOW is shown in [INT_STATUS_LSB_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-394. INT_STATUS_LSB_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_LSB_LOW		0x0	Interrupt status for temperature/internal voltages [0]= TEMP [1]= TEMP_100C [2]= IV1 [3]= IV2 [4]= IV3 [5]= IV4 [6]= RESERVED [7]= RESERVED

8.6.7.17 INT_STATUS_MSB_LOW Register (Address = 0x24) [Default = 0x00]INT_STATUS_MSB_LOW is shown in [INT_STATUS_MSB_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-395. INT_STATUS_MSB_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_MSB_LOW		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= EXT_VOL0 00000010= EXT_VOL1 00000100= RESERVED 00001000= RESERVED 00010000= RESERVED 00100000= RESERVED 01000000= RESERVED 10000000= RESERVED

8.6.7.18 INT_STATUS_LSB_HIGH Register (Address = 0x25) [Default = 0x00]INT_STATUS_LSB_HIGH is shown in [INT_STATUS_LSB_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-396. INT_STATUS_LSB_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_LSB_HIGH		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= TEMP 00000010= TEMP_100C 00000100= IV1 00001000= IV2 00010000= IV3 00100000= IV4 01000000= IV5 (RESERVED) 10000000= IV6 (RESERVED)

8.6.7.19 INT_STATUS_MSB_HIGH Register (Address = 0x26) [Default = 0x00]INT_STATUS_MSB_HIGH is shown in [INT_STATUS_MSB_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-397. INT_STATUS_MSB_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_STATUS_MSB_HIGH		0x0	Interrupt status for temperature/internal voltages (One-Hot) 00000001= EXT_VOL0 00000010= EXT_VOL1 00000100= RESERVED 00001000= RESERVED 00010000= RESERVED 00100000= RESERVED 01000000= RESERVED 10000000= RESERVED

8.6.7.20 INT_LINE_FAULT0_M0 Register (Address = 0x27) [Default = 0x00]INT_LINE_FAULT0_M0 is shown in [INT_LINE_FAULT0_M0 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-398. INT_LINE_FAULT0_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT0_M0		0x0	Interrupt status for LINE_FAULT0 (one-hot) 00000001= short to battery (threshold 0) 00000010= POC normal operation (threshold 1) 00000100= threshold 2 (RESERVED) 00001000= threshold 3 (RESERVED) 00010000= threshold 4 (RESERVED) 00100000= threshold 5 (RESERVED) 01000000= threshold 6 (RESERVED) 10000000= threshold 7 (RESERVED)

8.6.7.21 INT_LINE_FAULT1_M0 Register (Address = 0x28) [Default = 0x00]INT_LINE_FAULT1_M0 is shown in [INT_LINE_FAULT1_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-399. INT_LINE_FAULT1_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	INT_LINE_FAULT1_M0		0x0	Interrupt status for LINE_FAULT1 (one-hot) 00000001= short to battery (threshold 0) 00000010= POC normal operation (threshold 1) 00000100= threshold 2 (RESERVED) 00001000= threshold 3 (RESERVED) 00010000= threshold 4 (RESERVED) 00100000= threshold 5 (RESERVED) 01000000= threshold 6 (RESERVED) 10000000= threshold 7 (RESERVED)

8.6.7.22 INT_LINE_FAULT_UNDEG Register (Address = 0x2F) [Default = 0x00]INT_LINE_FAULT_UNDEG is shown in [INT_LINE_FAULT_UNDEG Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-400. INT_LINE_FAULT_UNDEG Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0x0	Reserved
3-0	INT_LINE_FAULT_UNDE F_M0		0x0	Interrupt status to signal ADC value in undefined range 0 - Line fault 0 1 - Line fault 1 2 - Line fault 2 3 - Line fault 3

8.6.7.23 INT_LINE_FAULT_SATURATE Register (Address = 0x30) [Default = 0x00]INT_LINE_FAULT_SATURATE is shown in [INT_LINE_FAULT_SATURATE Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-401. INT_LINE_FAULT_SATURATE Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0x0	Reserved
3	INT_LINE_FAULT3_SATU RATE		0x0	Indicates Line Fault Detection Saturated

Table 8-401. INT_LINE_FAULT_SATURATE Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	INT_LINE_FAULT2_SATURATE		0x0	Indicates Line Fault Detection Saturated
1	INT_LINE_FAULT1_SATURATE		0x0	Indicates Line Fault Detection Saturated
0	INT_LINE_FAULT0_SATURATE		0x0	Indicates Line Fault Detection Saturated

8.6.7.24 TEMP_HIGH Register (Address = 0x33) [Default = 0xCE]TEMP_HIGH is shown in [TEMP_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-402. TEMP_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_HIGH	R/W	0xCE	Upper threshold for TEMP

8.6.7.25 TEMP_LOW Register (Address = 0x34) [Default = 0x7E]TEMP_LOW is shown in [TEMP_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-403. TEMP_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_LOW	R/W	0x7E	Lower threshold for TEMP

8.6.7.26 TEMP_ADC_OFFSET Register (Address = 0x35) [Default = 0x00]TEMP_ADC_OFFSET is shown in [TEMP_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-404. TEMP_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	TEMP_ADC_OFFSET	R/W	0x0	ADC offset

8.6.7.27 IV0_HIGH Register (Address = 0x39) [Default = 0x86]IV0_HIGH is shown in [IV0_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-405. IV0_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_HIGH	R/W	0x86	Upper threshold for IV0

8.6.7.28 IV0_LOW Register (Address = 0x3A) [Default = 0x7A]IV0_LOW is shown in [IV0_LOW Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-406. IV0_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	IV0_LOW	R/W	0x7A	Lower threshold for IV0

8.6.7.29 IV0_ADC_OFFSET Register (Address = 0x3B) [Default = 0x00]IV0_ADC_OFFSET is shown in [IV0_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-407. IV0_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV0_ADC_OFFSET	R/W	0x0	ADC offset

8.6.7.30 IV1_HIGH Register (Address = 0x3C) [Default = 0x86]IV1_HIGH is shown in [IV1_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-408. IV1_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_HIGH	R/W	0x86	Upper threshold for IV1

8.6.7.31 IV1_LOW Register (Address = 0x3D) [Default = 0x7A]IV1_LOW is shown in [IV1_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-409. IV1_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_LOW	R/W	0x7A	Lower threshold for IV1

8.6.7.32 IV1_ADC_OFFSET Register (Address = 0x3E) [Default = 0x00]IV1_ADC_OFFSET is shown in [IV1_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-410. IV1_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV1_ADC_OFFSET	R/W	0x0	ADC offset

8.6.7.33 IV2_HIGH Register (Address = 0x3F) [Default = 0x86]IV2_HIGH is shown in [IV2_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-411. IV2_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV2_HIGH	R/W	0x86	Upper threshold for IV2

8.6.7.34 IV2_LOW Register (Address = 0x40) [Default = 0x7A]IV2_LOW is shown in [IV2_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-412. IV2_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV2_LOW	R/W	0x7A	Lower threshold for IV2

8.6.7.35 IV2_ADC_OFFSET Register (Address = 0x41) [Default = 0x00]IV2_ADC_OFFSET is shown in [IV2_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-413. IV2_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV2_ADC_OFFSET	R/W	0x0	ADC offset

8.6.7.36 IV3_HIGH Register (Address = 0x42) [Default = 0x86]IV3_HIGH is shown in [IV3_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-414. IV3_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV3_HIGH	R/W	0x86	Upper threshold for IV3

8.6.7.37 IV3_LOW Register (Address = 0x43) [Default = 0x7A]IV3_LOW is shown in [IV3_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-415. IV3_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV3_LOW	R/W	0x7A	Lower threshold for IV3

8.6.7.38 IV3_ADC_OFFSET Register (Address = 0x44) [Default = 0x00]IV3_ADC_OFFSET is shown in [IV3_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-416. IV3_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	IV3_ADC_OFFSET	R/W	0x0	ADC offset

8.6.7.39 TEMP_IV_MASK Register (Address = 0x4B) [Default = 0xC2]TEMP_IV_MASK is shown in [TEMP_IV_MASK Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-417. TEMP_IV_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	IV3_THRESH_MASK	R/W	0x0	1 means no interrupt
4	IV2_THRESH_MASK	R/W	0x0	1 means no interrupt
3	IV1_THRESH_MASK	R/W	0x0	1 means no interrupt
2	IV0_THRESH_MASK	R/W	0x0	1 means no interrupt
1	RESERVED	R/W	0x1	Reserved
0	TEMP_THRESH_MASK	R/W	0x0	1 means no interrupt

8.6.7.40 EXT_VOL0_HIGH Register (Address = 0x4C) [Default = 0x00]EXT_VOL0_HIGH is shown in [EXT_VOL0_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-418. EXT_VOL0_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_HIGH	R/W	0x0	Upper threshold for EXT_VOL0

8.6.7.41 EXT_VOL0_LOW Register (Address = 0x4D) [Default = 0x00]EXT_VOL0_LOW is shown in [EXT_VOL0_LOW Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-419. EXT_VOL0_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_LOW	R/W	0x0	Lower threshold for EXT_VOL0

8.6.7.42 EXT_VOL0_ADC_OFFSET Register (Address = 0x4E) [Default = 0x00]EXT_VOL0_ADC_OFFSET is shown in [EXT_VOL0_ADC_OFFSET Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-420. EXT_VOL0_ADC_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL0_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the VOL0 voltage conversion

8.6.7.43 EXT_VOL1_HIGH Register (Address = 0x4F) [Default = 0x00]EXT_VOL1_HIGH is shown in [EXT_VOL1_HIGH Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-421. EXT_VOL1_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_HIGH	R/W	0x0	Upper threshold for EXT_VOL1

8.6.7.44 EXT_VOL1_LOW Register (Address = 0x50) [Default = 0x00]

EXT_VOL1_LOW is shown in [EXT_VOL1_LOW Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-422. EXT_VOL1_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_LOW	R/W	0x0	Lower threshold for EXT_VOL1

8.6.7.45 EXT_VOL1_ADC_OFFSET Register (Address = 0x51) [Default = 0x00]

EXT_VOL1_ADC_OFFSET is shown in [EXT_VOL1_ADC_OFFSET Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-423. EXT_VOL1_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	EXT_VOL1_ADC_OFFSET	R/W	0x0	ADC offset added to the final ADC code after the VOL0 voltage conversion

8.6.7.46 EXT_VOL_MASK Register (Address = 0x52) [Default = 0x00]

EXT_VOL_MASK is shown in [EXT_VOL_MASK Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-424. EXT_VOL_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0x0	RESERVED
1	EXT_VOL1_THRESH_MASK	R/W	0x0	1 means no interrupt EXT_VOL1_THRESH_MASK
0	EXT_VOL0_THRESH_MASK	R/W	0x0	1 means no interrupt EXT_VOL0_THRESH_MASK

8.6.7.47 LINE_FAULT0_THRESH_0_HI_M0 Register (Address = 0x53) [Default = 0xFF]

LINE_FAULT0_THRESH_0_HI_M0 is shown in [LINE_FAULT0_THRESH_0_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-425. LINE_FAULT0_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_HI_M0	R/W	0xFF	Upper threshold 0 for LINE_FAULT0 (Mode0)

8.6.7.48 LINE_FAULT0_THRESH_0_LO_M0 Register (Address = 0x54) [Default = 0xD5]

LINE_FAULT0_THRESH_0_LO_M0 is shown in [LINE_FAULT0_THRESH_0_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-426. LINE_FAULT0_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_0_LO_M0	R/W	0xD5	Lower threshold 0 for LINE_FAULT0 (Mode0)

8.6.7.49 LINE_FAULT0_THRESH_1_HI_M0 Register (Address = 0x55) [Default = 0xC9]LINE_FAULT0_THRESH_1_HI_M0 is shown in [LINE_FAULT0_THRESH_1_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-427. LINE_FAULT0_THRESH_1_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_HI_M0	R/W	0xC9	Upper threshold 1 for LINE_FAULT0 (Mode0)

8.6.7.50 LINE_FAULT0_THRESH_1_LO_M0 Register (Address = 0x56) [Default = 0x92]LINE_FAULT0_THRESH_1_LO_M0 is shown in [LINE_FAULT0_THRESH_1_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-428. LINE_FAULT0_THRESH_1_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_1_LO_M0	R/W	0x92	Lower threshold 1 for LINE_FAULT0 (Mode0)

8.6.7.51 LINE_FAULT0_THRESH_2_HI_M0 Register (Address = 0x57) [Default = 0x00]LINE_FAULT0_THRESH_2_HI_M0 is shown in [LINE_FAULT0_THRESH_2_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-429. LINE_FAULT0_THRESH_2_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT0 (Mode0)

8.6.7.52 LINE_FAULT0_THRESH_2_LO_M0 Register (Address = 0x58) [Default = 0x00]LINE_FAULT0_THRESH_2_LO_M0 is shown in [LINE_FAULT0_THRESH_2_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-430. LINE_FAULT0_THRESH_2_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT0 (Mode0)

8.6.7.53 LINE_FAULT0_THRESH_3_HI_M0 Register (Address = 0x59) [Default = 0x00]LINE_FAULT0_THRESH_3_HI_M0 is shown in [LINE_FAULT0_THRESH_3_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-431. LINE_FAULT0_THRESH_3_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT0 (Mode0)

8.6.7.54 LINE_FAULT0_THRESH_3_LO_M0 Register (Address = 0x5A) [Default = 0x00]

LINE_FAULT0_THRESH_3_LO_M0 is shown in [LINE_FAULT0_THRESH_3_LO_M0 Register Field Descriptions](#).

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Table 8-432. LINE_FAULT0_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT0 (Mode0)

8.6.7.55 LINE_FAULT0_THRESH_4_HI_M0 Register (Address = 0x5B) [Default = 0x00]

LINE_FAULT0_THRESH_4_HI_M0 is shown in [LINE_FAULT0_THRESH_4_HI_M0 Register Field Descriptions](#).

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Table 8-433. LINE_FAULT0_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT0 (Mode0)

8.6.7.56 LINE_FAULT0_THRESH_4_LO_M0 Register (Address = 0x5C) [Default = 0x00]

LINE_FAULT0_THRESH_4_LO_M0 is shown in [LINE_FAULT0_THRESH_4_LO_M0 Register Field Descriptions](#).

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Table 8-434. LINE_FAULT0_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT0 (Mode0)

8.6.7.57 LINE_FAULT0_THRESH_5_HI_M0 Register (Address = 0x5D) [Default = 0x00]

LINE_FAULT0_THRESH_5_HI_M0 is shown in [LINE_FAULT0_THRESH_5_HI_M0 Register Field Descriptions](#).

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Table 8-435. LINE_FAULT0_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT0 (Mode0)

8.6.7.58 LINE_FAULT0_THRESH_5_LO_M0 Register (Address = 0x5E) [Default = 0x00]

LINE_FAULT0_THRESH_5_LO_M0 is shown in [LINE_FAULT0_THRESH_5_LO_M0 Register Field Descriptions](#).

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Table 8-436. LINE_FAULT0_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT0 (Mode0)

8.6.7.59 LINE_FAULT0_THRESH_6_HI_M0 Register (Address = 0x5F) [Default = 0x00]LINE_FAULT0_THRESH_6_HI_M0 is shown in [LINE_FAULT0_THRESH_6_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-437. LINE_FAULT0_THRESH_6_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT0 (Mode0)

8.6.7.60 LINE_FAULT0_THRESH_6_LO_M0 Register (Address = 0x60) [Default = 0x00]LINE_FAULT0_THRESH_6_LO_M0 is shown in [LINE_FAULT0_THRESH_6_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-438. LINE_FAULT0_THRESH_6_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT0 (Mode0)

8.6.7.61 LINE_FAULT0_THRESH_7_HI_M0 Register (Address = 0x61) [Default = 0x00]LINE_FAULT0_THRESH_7_HI_M0 is shown in [LINE_FAULT0_THRESH_7_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-439. LINE_FAULT0_THRESH_7_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT0 (Mode0)

8.6.7.62 LINE_FAULT0_THRESH_7_LO_M0 Register (Address = 0x62) [Default = 0x00]LINE_FAULT0_THRESH_7_LO_M0 is shown in [LINE_FAULT0_THRESH_7_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-440. LINE_FAULT0_THRESH_7_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT0 (Mode0)

8.6.7.63 LINE_FAULT0_THRESH_MASK_M0 Register (Address = 0x63) [Default = 0xFC]LINE_FAULT0_THRESH_MASK_M0 is shown in [LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-441. LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LINE_FAULT0_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

Table 8-441. LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	LINE_FAULT0_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT0_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
4	LINE_FAULT0_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT0_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT0_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT0_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT0_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

8.6.7.64 LINE_FAULT0_ADC_OFFSET_M0 Register (Address = 0x64) [Default = 0x00]LINE_FAULT0_ADC_OFFSET_M0 is shown in [LINE_FAULT0_ADC_OFFSET_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-442. LINE_FAULT0_ADC_OFFSET_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT0_ADC_OFFSET_M0	R/W	0x0	ADC offset added to the final ADC code after the line fault 0 voltage conversion

8.6.7.65 LINE_FAULT1_THRESH_0_HI_M0 Register (Address = 0x65) [Default = 0xFF]LINE_FAULT1_THRESH_0_HI_M0 is shown in [LINE_FAULT1_THRESH_0_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-443. LINE_FAULT1_THRESH_0_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_HI_M0	R/W	0xFF	Upper threshold 0 for LINE_FAULT1 (Mode0)

8.6.7.66 LINE_FAULT1_THRESH_0_LO_M0 Register (Address = 0x66) [Default = 0xD5]LINE_FAULT1_THRESH_0_LO_M0 is shown in [LINE_FAULT1_THRESH_0_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-444. LINE_FAULT1_THRESH_0_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_0_LO_M0	R/W	0xD5	Lower threshold 0 for LINE_FAULT1 (Mode0)

8.6.7.67 LINE_FAULT1_THRESH_1_HI_M0 Register (Address = 0x67) [Default = 0xC9]LINE_FAULT1_THRESH_1_HI_M0 is shown in [LINE_FAULT1_THRESH_1_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-445. LINE_FAULT1_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_HI_M0	R/W	0xC9	Upper threshold 1 for LINE_FAULT1 (Mode0)

8.6.7.68 LINE_FAULT1_THRESH_1_LO_M0 Register (Address = 0x68) [Default = 0x92]

LINE_FAULT1_THRESH_1_LO_M0 is shown in [LINE_FAULT1_THRESH_1_LO_M0 Register Field Descriptions](#).

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Table 8-446. LINE_FAULT1_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_1_LO_M0	R/W	0x92	Lower threshold 1 for LINE_FAULT1 (Mode0)

8.6.7.69 LINE_FAULT1_THRESH_2_HI_M0 Register (Address = 0x69) [Default = 0x00]

LINE_FAULT1_THRESH_2_HI_M0 is shown in [LINE_FAULT1_THRESH_2_HI_M0 Register Field Descriptions](#).

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Table 8-447. LINE_FAULT1_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT1 (Mode0)

8.6.7.70 LINE_FAULT1_THRESH_2_LO_M0 Register (Address = 0x6A) [Default = 0x00]

LINE_FAULT1_THRESH_2_LO_M0 is shown in [LINE_FAULT1_THRESH_2_LO_M0 Register Field Descriptions](#).

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Table 8-448. LINE_FAULT1_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT1 (Mode0)

8.6.7.71 LINE_FAULT1_THRESH_3_HI_M0 Register (Address = 0x6B) [Default = 0x00]

LINE_FAULT1_THRESH_3_HI_M0 is shown in [LINE_FAULT1_THRESH_3_HI_M0 Register Field Descriptions](#).

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Table 8-449. LINE_FAULT1_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT1 (Mode0)

8.6.7.72 LINE_FAULT1_THRESH_3_LO_M0 Register (Address = 0x6C) [Default = 0x00]

LINE_FAULT1_THRESH_3_LO_M0 is shown in [LINE_FAULT1_THRESH_3_LO_M0 Register Field Descriptions](#).

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Table 8-450. LINE_FAULT1_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT1 (Mode0)

8.6.7.73 LINE_FAULT1_THRESH_4_HI_M0 Register (Address = 0x6D) [Default = 0x00]

LINE_FAULT1_THRESH_4_HI_M0 is shown in [LINE_FAULT1_THRESH_4_HI_M0 Register Field Descriptions](#).

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Table 8-451. LINE_FAULT1_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT1 (Mode0)

8.6.7.74 LINE_FAULT1_THRESH_4_LO_M0 Register (Address = 0x6E) [Default = 0x00]

LINE_FAULT1_THRESH_4_LO_M0 is shown in [LINE_FAULT1_THRESH_4_LO_M0 Register Field Descriptions](#).

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Table 8-452. LINE_FAULT1_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT1 (Mode0)

8.6.7.75 LINE_FAULT1_THRESH_5_HI_M0 Register (Address = 0x6F) [Default = 0x00]

LINE_FAULT1_THRESH_5_HI_M0 is shown in [LINE_FAULT1_THRESH_5_HI_M0 Register Field Descriptions](#).

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Table 8-453. LINE_FAULT1_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT1 (Mode0)

8.6.7.76 LINE_FAULT1_THRESH_5_LO_M0 Register (Address = 0x70) [Default = 0x00]

LINE_FAULT1_THRESH_5_LO_M0 is shown in [LINE_FAULT1_THRESH_5_LO_M0 Register Field Descriptions](#).

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Table 8-454. LINE_FAULT1_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT1 (Mode0)

8.6.7.77 LINE_FAULT1_THRESH_6_HI_M0 Register (Address = 0x71) [Default = 0x00]

LINE_FAULT1_THRESH_6_HI_M0 is shown in [LINE_FAULT1_THRESH_6_HI_M0 Register Field Descriptions](#).

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Table 8-455. LINE_FAULT1_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT1 (Mode0)

8.6.7.78 LINE_FAULT1_THRESH_6_LO_M0 Register (Address = 0x72) [Default = 0x00]

LINE_FAULT1_THRESH_6_LO_M0 is shown in [LINE_FAULT1_THRESH_6_LO_M0 Register Field Descriptions](#).

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Table 8-456. LINE_FAULT1_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT1 (Mode0)

8.6.7.79 LINE_FAULT1_THRESH_7_HI_M0 Register (Address = 0x73) [Default = 0x00]

LINE_FAULT1_THRESH_7_HI_M0 is shown in [LINE_FAULT1_THRESH_7_HI_M0 Register Field Descriptions](#).

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Table 8-457. LINE_FAULT1_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT1 (Mode0)

8.6.7.80 LINE_FAULT1_THRESH_7_LO_M0 Register (Address = 0x74) [Default = 0x00]

LINE_FAULT1_THRESH_7_LO_M0 is shown in [LINE_FAULT1_THRESH_7_LO_M0 Register Field Descriptions](#).

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Table 8-458. LINE_FAULT1_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT1 (Mode0)

8.6.7.81 LINE_FAULT1_THRESH_MASK_M0 Register (Address = 0x75) [Default = 0xFC]

LINE_FAULT1_THRESH_MASK_M0 is shown in [LINE_FAULT1_THRESH_MASK_M0 Register Field Descriptions](#).

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Table 8-459. LINE_FAULT1_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT1_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT1_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT1_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

Table 8-459. LINE_FAULT1_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINE_FAULT1_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT1_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT1_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT1_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT1_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

8.6.7.82 LINE_FAULT1_ADC_OFFSET_M0 Register (Address = 0x76) [Default = 0x00]LINE_FAULT1_ADC_OFFSET_M0 is shown in [LINE_FAULT1_ADC_OFFSET_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-460. LINE_FAULT1_ADC_OFFSET_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT1_ADC_OFF_SET_M0	R/W	0x0	ADC offset added to the final ADC code after the line fault 0 voltage conversion

8.6.7.83 LINE_FAULT2_THRESH_0_HI_M0 Register (Address = 0x77) [Default = 0xFF]LINE_FAULT2_THRESH_0_HI_M0 is shown in [LINE_FAULT2_THRESH_0_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-461. LINE_FAULT2_THRESH_0_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_0_HI_M0	R/W	0xFF	Upper threshold 0 for LINE_FAULT2 (Mode0)

8.6.7.84 LINE_FAULT2_THRESH_0_LO_M0 Register (Address = 0x78) [Default = 0xD5]LINE_FAULT2_THRESH_0_LO_M0 is shown in [LINE_FAULT2_THRESH_0_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-462. LINE_FAULT2_THRESH_0_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_0_LO_M0	R/W	0xD5	Lower threshold 0 for LINE_FAULT2 (Mode0)

8.6.7.85 LINE_FAULT2_THRESH_1_HI_M0 Register (Address = 0x79) [Default = 0xC9]LINE_FAULT2_THRESH_1_HI_M0 is shown in [LINE_FAULT2_THRESH_1_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-463. LINE_FAULT2_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_1_HI_M0	R/W	0xC9	Upper threshold 1 for LINE_FAULT2 (Mode0)

8.6.7.86 LINE_FAULT2_THRESH_1_LO_M0 Register (Address = 0x7A) [Default = 0x92]

LINE_FAULT2_THRESH_1_LO_M0 is shown in [LINE_FAULT2_THRESH_1_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-464. LINE_FAULT2_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_1_LO_M0	R/W	0x92	Lower threshold 1 for LINE_FAULT2 (Mode0)

8.6.7.87 LINE_FAULT2_THRESH_2_HI_M0 Register (Address = 0x7B) [Default = 0x00]

LINE_FAULT2_THRESH_2_HI_M0 is shown in [LINE_FAULT2_THRESH_2_HI_M0 Register Field Descriptions](#).

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Table 8-465. LINE_FAULT2_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT2 (Mode0)

8.6.7.88 LINE_FAULT2_THRESH_2_LO_M0 Register (Address = 0x7C) [Default = 0x00]

LINE_FAULT2_THRESH_2_LO_M0 is shown in [LINE_FAULT2_THRESH_2_LO_M0 Register Field Descriptions](#).

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Table 8-466. LINE_FAULT2_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT2 (Mode0)

8.6.7.89 LINE_FAULT2_THRESH_3_HI_M0 Register (Address = 0x7D) [Default = 0x00]

LINE_FAULT2_THRESH_3_HI_M0 is shown in [LINE_FAULT2_THRESH_3_HI_M0 Register Field Descriptions](#).

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Table 8-467. LINE_FAULT2_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT2 (Mode0)

8.6.7.90 LINE_FAULT2_THRESH_3_LO_M0 Register (Address = 0x7E) [Default = 0x00]

LINE_FAULT2_THRESH_3_LO_M0 is shown in [LINE_FAULT2_THRESH_3_LO_M0 Register Field Descriptions](#).

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Table 8-468. LINE_FAULT2_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT2 (Mode0)

8.6.7.91 LINE_FAULT2_THRESH_4_HI_M0 Register (Address = 0x7F) [Default = 0x00]

LINE_FAULT2_THRESH_4_HI_M0 is shown in [LINE_FAULT2_THRESH_4_HI_M0 Register Field Descriptions](#).

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Table 8-469. LINE_FAULT2_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT2 (Mode0)

8.6.7.92 LINE_FAULT2_THRESH_4_LO_M0 Register (Address = 0x80) [Default = 0x00]

LINE_FAULT2_THRESH_4_LO_M0 is shown in [LINE_FAULT2_THRESH_4_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-470. LINE_FAULT2_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT2 (Mode0)

8.6.7.93 LINE_FAULT2_THRESH_5_HI_M0 Register (Address = 0x81) [Default = 0x00]

LINE_FAULT2_THRESH_5_HI_M0 is shown in [LINE_FAULT2_THRESH_5_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-471. LINE_FAULT2_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT2 (Mode0)

8.6.7.94 LINE_FAULT2_THRESH_5_LO_M0 Register (Address = 0x82) [Default = 0x00]

LINE_FAULT2_THRESH_5_LO_M0 is shown in [LINE_FAULT2_THRESH_5_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-472. LINE_FAULT2_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT2 (Mode0)

8.6.7.95 LINE_FAULT2_THRESH_6_HI_M0 Register (Address = 0x83) [Default = 0x00]

LINE_FAULT2_THRESH_6_HI_M0 is shown in [LINE_FAULT2_THRESH_6_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-473. LINE_FAULT2_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT2 (Mode0)

8.6.7.96 LINE_FAULT2_THRESH_6_LO_M0 Register (Address = 0x84) [Default = 0x00]

LINE_FAULT2_THRESH_6_LO_M0 is shown in [LINE_FAULT2_THRESH_6_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-474. LINE_FAULT2_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT2 (Mode0)

8.6.7.97 LINE_FAULT2_THRESH_7_HI_M0 Register (Address = 0x85) [Default = 0x00]

LINE_FAULT2_THRESH_7_HI_M0 is shown in [LINE_FAULT2_THRESH_7_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-475. LINE_FAULT2_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT2 (Mode0)

8.6.7.98 LINE_FAULT2_THRESH_7_LO_M0 Register (Address = 0x86) [Default = 0x00]

LINE_FAULT2_THRESH_7_LO_M0 is shown in [LINE_FAULT2_THRESH_7_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-476. LINE_FAULT2_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT2 (Mode0)

8.6.7.99 LINE_FAULT2_THRESH_MASK_M0 Register (Address = 0x87) [Default = 0xFC]

LINE_FAULT2_THRESH_MASK_M0 is shown in [LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-477. LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT2_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT2_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT2_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

Table 8-477. LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINE_FAULT2_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT2_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT2_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT2_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT2_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

8.6.7.100 LINE_FAULT2_ADC_OFFSET_M0 Register (Address = 0x88) [Default = 0x00]LINE_FAULT2_ADC_OFFSET_M0 is shown in [LINE_FAULT2_ADC_OFFSET_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-478. LINE_FAULT2_ADC_OFFSET_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT2_ADC_OFF_SET_M0	R/W	0x0	ADC offset added to the final ADC code after the line fault 0 voltage conversion

8.6.7.101 LINE_FAULT3_THRESH_0_HI_M0 Register (Address = 0x89) [Default = 0xFF]LINE_FAULT3_THRESH_0_HI_M0 is shown in [LINE_FAULT3_THRESH_0_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-479. LINE_FAULT3_THRESH_0_HI_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_0_HI_M0	R/W	0xFF	Upper threshold 0 for LINE_FAULT3 (Mode0)

8.6.7.102 LINE_FAULT3_THRESH_0_LO_M0 Register (Address = 0x8A) [Default = 0xD5]LINE_FAULT3_THRESH_0_LO_M0 is shown in [LINE_FAULT3_THRESH_0_LO_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-480. LINE_FAULT3_THRESH_0_LO_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_0_LO_M0	R/W	0xD5	Lower threshold 0 for LINE_FAULT3 (Mode0)

8.6.7.103 LINE_FAULT3_THRESH_1_HI_M0 Register (Address = 0x8B) [Default = 0xC9]LINE_FAULT3_THRESH_1_HI_M0 is shown in [LINE_FAULT3_THRESH_1_HI_M0 Register Field Descriptions](#).Return to the [Summary Table](#).

Table 8-481. LINE_FAULT3_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_1_HI_M0	R/W	0xC9	Upper threshold 1 for LINE_FAULT3 (Mode0)

8.6.7.104 LINE_FAULT3_THRESH_1_LO_M0 Register (Address = 0x8C) [Default = 0x92]

LINE_FAULT3_THRESH_1_LO_M0 is shown in [LINE_FAULT3_THRESH_1_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-482. LINE_FAULT3_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_1_LO_M0	R/W	0x92	Lower threshold 1 for LINE_FAULT3 (Mode0)

8.6.7.105 LINE_FAULT3_THRESH_2_HI_M0 Register (Address = 0x8D) [Default = 0x00]

LINE_FAULT3_THRESH_2_HI_M0 is shown in [LINE_FAULT3_THRESH_2_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-483. LINE_FAULT3_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_2_HI_M0	R/W	0x0	Upper threshold 2 for LINE_FAULT3 (Mode0)

8.6.7.106 LINE_FAULT3_THRESH_2_LO_M0 Register (Address = 0x8E) [Default = 0x00]

LINE_FAULT3_THRESH_2_LO_M0 is shown in [LINE_FAULT3_THRESH_2_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-484. LINE_FAULT3_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_2_LO_M0	R/W	0x0	Lower threshold 2 for LINE_FAULT3 (Mode0)

8.6.7.107 LINE_FAULT3_THRESH_3_HI_M0 Register (Address = 0x8F) [Default = 0x00]

LINE_FAULT3_THRESH_3_HI_M0 is shown in [LINE_FAULT3_THRESH_3_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-485. LINE_FAULT3_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_3_HI_M0	R/W	0x0	Upper threshold 3 for LINE_FAULT3 (Mode0)

8.6.7.108 LINE_FAULT3_THRESH_3_LO_M0 Register (Address = 0x90) [Default = 0x00]

LINE_FAULT3_THRESH_3_LO_M0 is shown in [LINE_FAULT3_THRESH_3_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-486. LINE_FAULT3_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_3_LO_M0	R/W	0x0	Lower threshold 3 for LINE_FAULT3 (Mode0)

8.6.7.109 LINE_FAULT3_THRESH_4_HI_M0 Register (Address = 0x91) [Default = 0x00]

LINE_FAULT3_THRESH_4_HI_M0 is shown in [LINE_FAULT3_THRESH_4_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-487. LINE_FAULT3_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_4_HI_M0	R/W	0x0	Upper threshold 4 for LINE_FAULT3 (Mode0)

8.6.7.110 LINE_FAULT3_THRESH_4_LO_M0 Register (Address = 0x92) [Default = 0x00]

LINE_FAULT3_THRESH_4_LO_M0 is shown in [LINE_FAULT3_THRESH_4_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-488. LINE_FAULT3_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_4_LO_M0	R/W	0x0	Lower threshold 4 for LINE_FAULT3 (Mode0)

8.6.7.111 LINE_FAULT3_THRESH_5_HI_M0 Register (Address = 0x93) [Default = 0x00]

LINE_FAULT3_THRESH_5_HI_M0 is shown in [LINE_FAULT3_THRESH_5_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-489. LINE_FAULT3_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_5_HI_M0	R/W	0x0	Upper threshold 5 for LINE_FAULT3 (Mode0)

8.6.7.112 LINE_FAULT3_THRESH_5_LO_M0 Register (Address = 0x94) [Default = 0x00]

LINE_FAULT3_THRESH_5_LO_M0 is shown in [LINE_FAULT3_THRESH_5_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-490. LINE_FAULT3_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_5_LO_M0	R/W	0x0	Lower threshold 5 for LINE_FAULT3 (Mode0)

8.6.7.113 LINE_FAULT3_THRESH_6_HI_M0 Register (Address = 0x95) [Default = 0x00]

LINE_FAULT3_THRESH_6_HI_M0 is shown in [LINE_FAULT3_THRESH_6_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-491. LINE_FAULT3_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_6_HI_M0	R/W	0x0	Upper threshold 6 for LINE_FAULT3 (Mode0)

8.6.7.114 LINE_FAULT3_THRESH_6_LO_M0 Register (Address = 0x96) [Default = 0x00]

LINE_FAULT3_THRESH_6_LO_M0 is shown in [LINE_FAULT3_THRESH_6_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-492. LINE_FAULT3_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_6_LO_M0	R/W	0x0	Lower threshold 6 for LINE_FAULT3 (Mode0)

8.6.7.115 LINE_FAULT3_THRESH_7_HI_M0 Register (Address = 0x97) [Default = 0x00]

LINE_FAULT3_THRESH_7_HI_M0 is shown in [LINE_FAULT3_THRESH_7_HI_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-493. LINE_FAULT3_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_7_HI_M0	R/W	0x0	Upper threshold 7 for LINE_FAULT3 (Mode0)

8.6.7.116 LINE_FAULT3_THRESH_7_LO_M0 Register (Address = 0x98) [Default = 0x00]

LINE_FAULT3_THRESH_7_LO_M0 is shown in [LINE_FAULT3_THRESH_7_LO_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-494. LINE_FAULT3_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_THRESH_7_LO_M0	R/W	0x0	Lower threshold 7 for LINE_FAULT3 (Mode0)

8.6.7.117 LINE_FAULT3_THRESH_MASK_M0 Register (Address = 0x99) [Default = 0xFC]

LINE_FAULT3_THRESH_MASK_M0 is shown in [LINE_FAULT3_THRESH_MASK_M0 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 8-495. LINE_FAULT3_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT3_THRESH_7_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
6	LINE_FAULT3_THRESH_6_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
5	LINE_FAULT3_THRESH_5_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

Table 8-495. LINE_FAULT3_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINE_FAULT3_THRESH_4_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
3	LINE_FAULT3_THRESH_3_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
2	LINE_FAULT3_THRESH_2_MASK_M0	R/W	0x1	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
1	LINE_FAULT3_THRESH_1_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt
0	LINE_FAULT3_THRESH_0_MASK_M0	R/W	0x0	1 - Mask Threshold Interrupt 0 - ADC output in this range will cause interrupt

8.6.7.118 LINE_FAULT3_ADC_OFFSET_M0 Register (Address = 0x9A) [Default = 0x00]LINE_FAULT3_ADC_OFFSET_M0 is shown in [LINE_FAULT3_ADC_OFFSET_M0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-496. LINE_FAULT3_ADC_OFFSET_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LINE_FAULT3_ADC_OFFSET_M0	R/W	0x0	ADC offset added to the final ADC code after the line fault 0 voltage conversion

8.6.7.119 ADC_OFFSET_POL0 Register (Address = 0xE5) [Default = 0x00]ADC_OFFSET_POL0 is shown in [ADC_OFFSET_POL0 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-497. ADC_OFFSET_POL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	IV3_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (IV3)
4	IV2_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (IV2)
3	IV1_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (IV1)
2	IV0_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (IV0)
1	RESERVED	R/W	0x0	Reserved
0	TEMP_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (temp)

8.6.7.120 ADC_OFFSET_POL1 Register (Address = 0xE6) [Default = 0x00]ADC_OFFSET_POL1 is shown in [ADC_OFFSET_POL1 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-498. ADC_OFFSET_POL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0x0	Reserved

Table 8-498. ADC_OFFSET_POL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	EXT_VOL1_ADC_OFFSET_T_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (EXT_VOL1)
0	EXT_VOL0_ADC_OFFSET_T_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (EXT_VOL0)

8.6.7.121 ADC_OFFSET_POL2 Register (Address = 0xE7) [Default = 0x00]ADC_OFFSET_POL2 is shown in [ADC_OFFSET_POL2 Register Field Descriptions](#).Return to the [Summary Table](#).**Table 8-499. ADC_OFFSET_POL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	LINE_FAULT3_M0_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (LINE_FAULT3_m0)
5	RESERVED	R/W	0x0	Reserved
4	LINE_FAULT2_M0_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (LINE_FAULT2_m0)
3	RESERVED	R/W	0x0	Reserved
2	LINE_FAULT1_M0_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (LINE_FAULT1_m0)
1	RESERVED	R/W	0x0	Reserved
0	LINE_FAULT0_M0_ADC_OFFSET_POL	R/W	0x0	Polarity of the ADC Offset added to the final ADC code after conversion (LINE_FAULT0_m0)

9 Application and Implementation**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

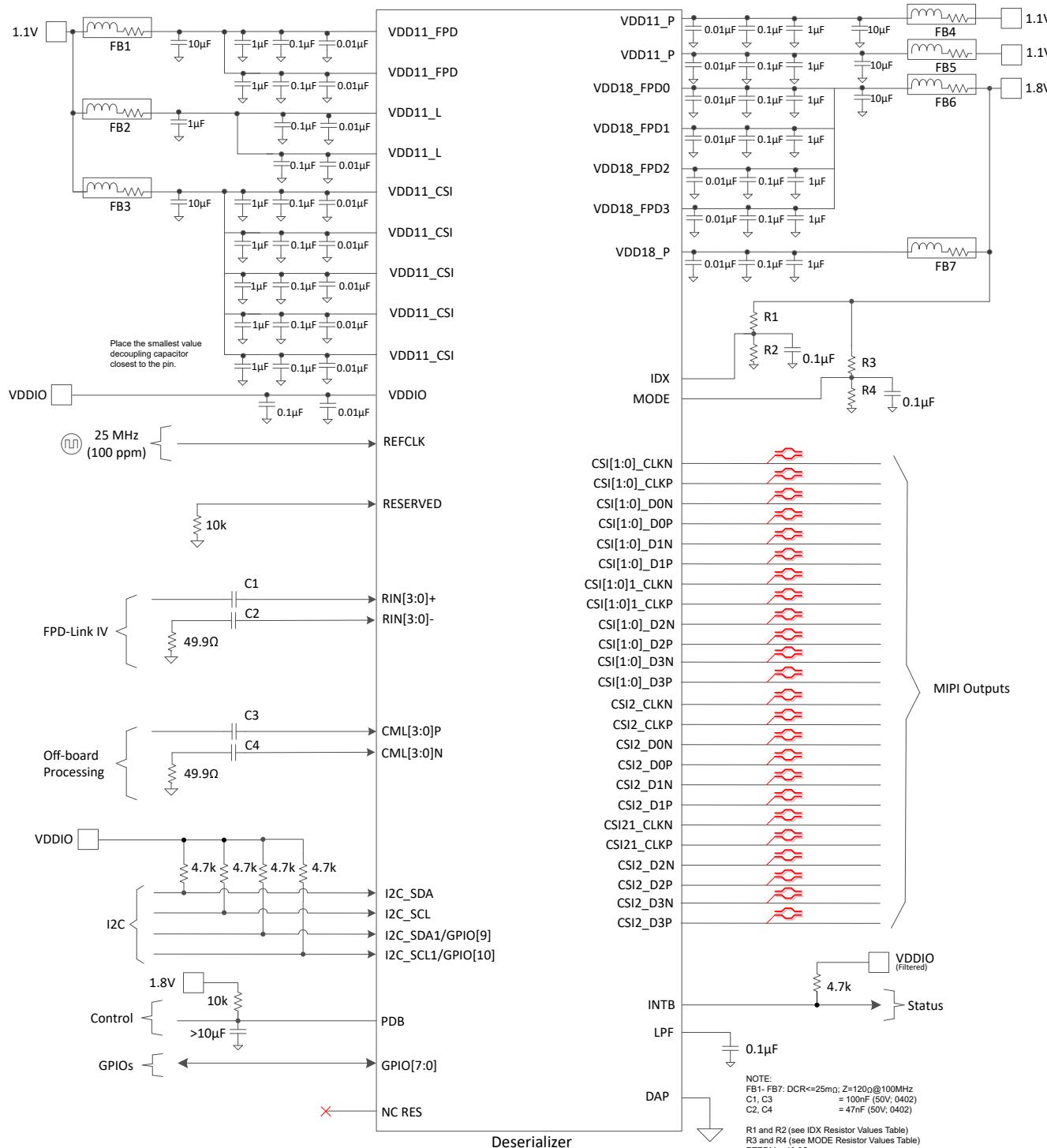


Figure 9-1. Typical Connection Diagram

9.1.1 Design Requirements

For the typical design application, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD11	1.1 V
VDD18	1.8 V
AC Coupling Capacitor for Synchronous Modes, Coaxial Connection: RIN+	100 nF (50 WV 0402)
AC Coupling Capacitor for Synchronous Modes, Coaxial Connection: RIN-	47 nF (50 WV 0402)
AC Coupling Capacitor for Synchronous Modes, STP Connection: RIN+ and RIN-	100 nF (50 WV 0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link signal path as shown in [Figure 9-2](#). For applications utilizing single-ended 50- Ω coaxial cable, terminate the unused data pins (RINx-) with an AC-coupling capacitor and a 50- Ω resistor.

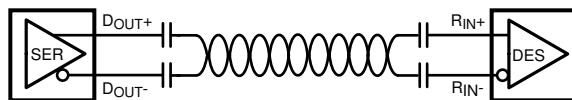


Figure 9-2. AC-Coupled Connection (STP)

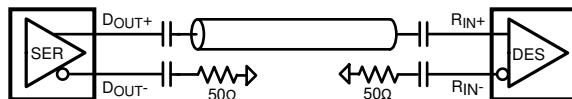


Figure 9-3. AC-Coupled Connection (Coaxial)

For high-speed FPD-Link transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

9.1.2 Detailed Design Procedure

[Section 9.1](#) shows a typical application circuit of the DS90UB971-Q1. The next sections highlight recommendations for the critical device pins.

9.1.3 Application Curves

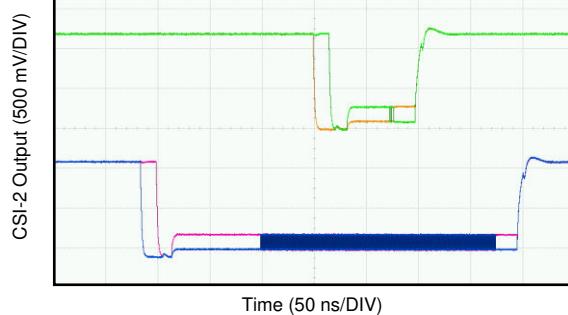


Figure 9-4. CSI-2 DATA and CLK Output

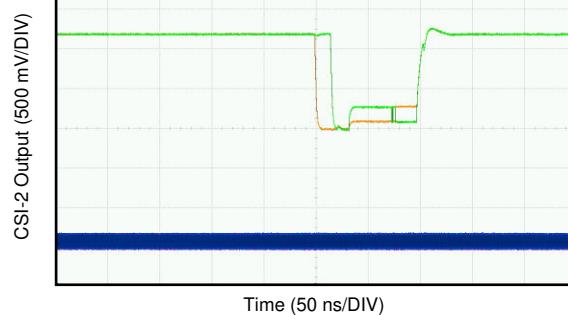


Figure 9-5. CSI-2 DATA and Continuous CLK Output

9.2 System Example

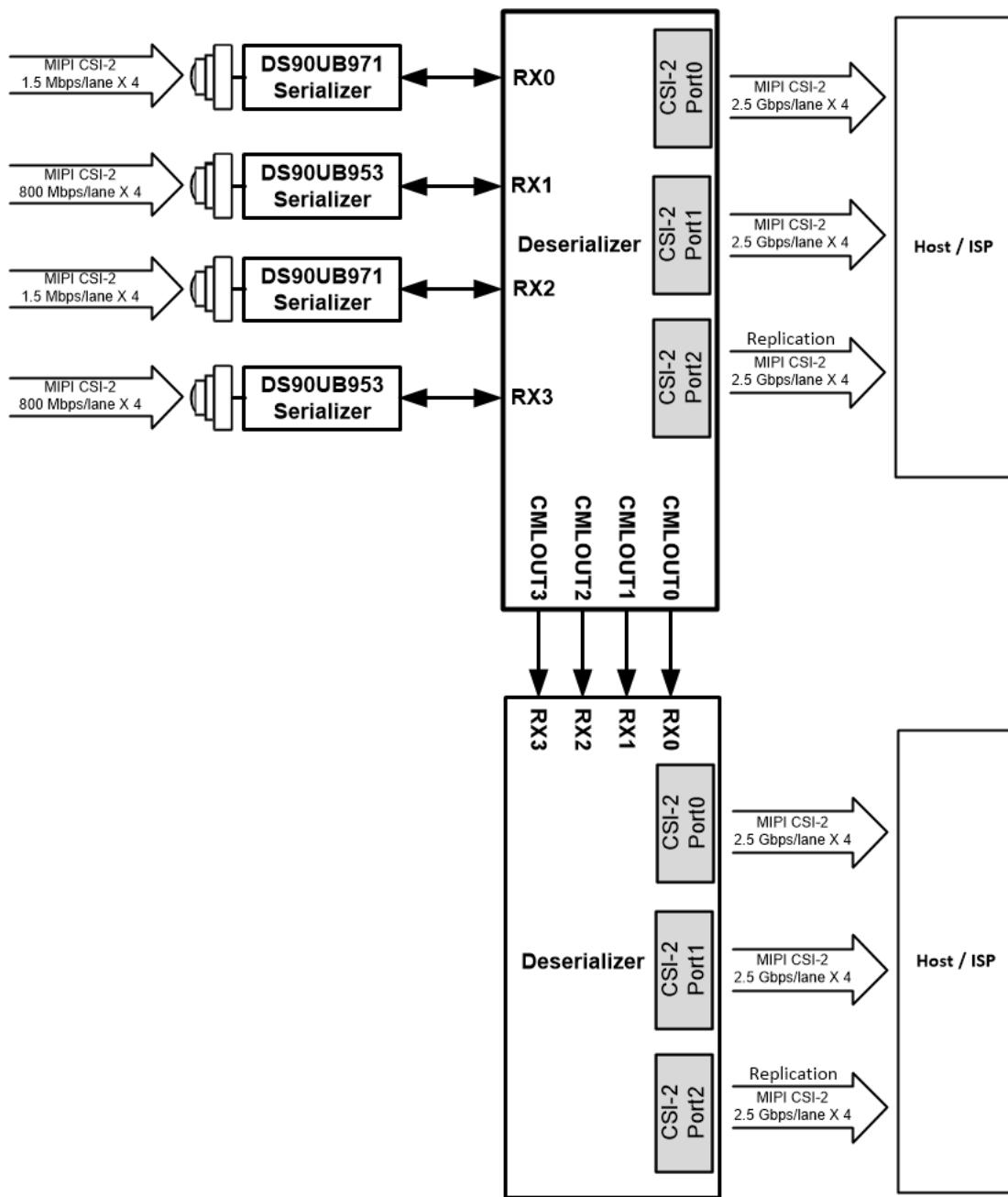


Figure 9-6. Example System with Multiple Camera Inputs

9.3 Power Over Coax

The device is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data and bi-directional control and diagnostics data transmission. The method utilizes passive networks or filters that isolate the transmission line from the loading of the DC-DC regulator circuits and their connecting power traces on both sides of the link as shown in [Figure 9-7](#).

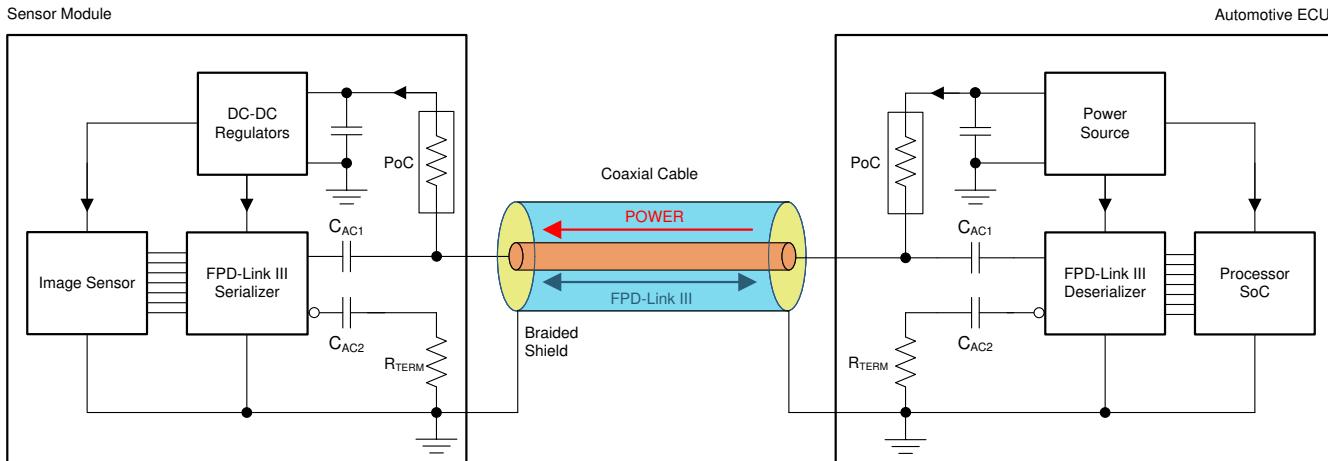
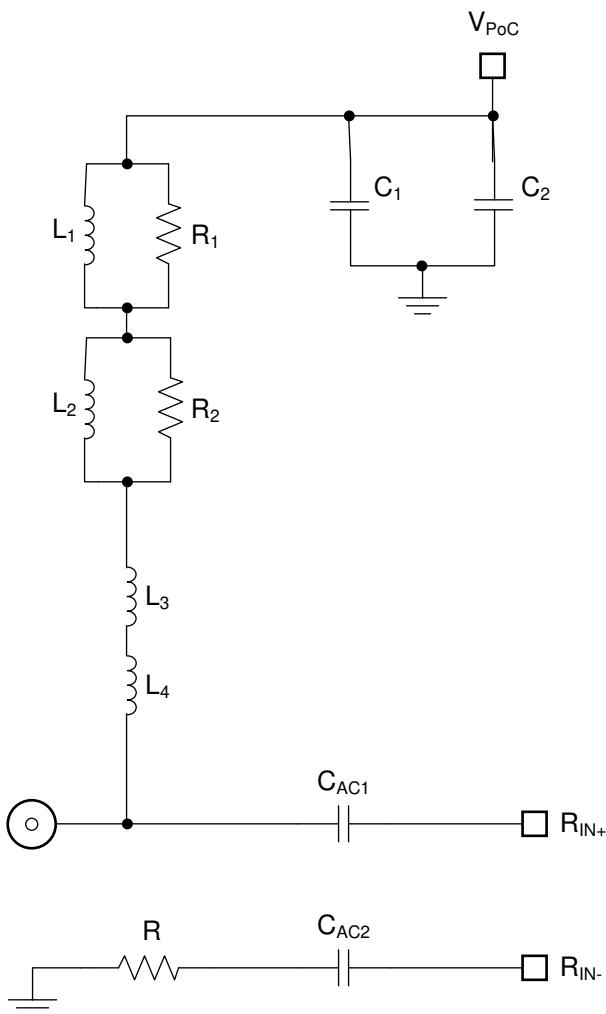


Figure 9-7. Power Over Coax (PoC) System Diagram

The lower limit of the frequency band is defined as $\frac{1}{2}$ of the bi-directional control channel's frequency, f_{BCC} . The upper limit of the frequency band is the frequency of the forward high-speed channel, f_{FC} .

9.3.1 Recommended PoC Network

The diagram here shows a PoC network recommended for FPD-Link consisting of DS90UB971/951/953/935/933/913A-Q1 and the deserializer pair with the bi-directional channel operating from 2.3594Mbps ($f \approx 2.3594\text{MHz}$) to 7.55Gbps ($f \approx 3.775\text{ GHz}$). This network can support up to 300mA of current. For higher current solutions or solutions to cover a different frequency range, contact TI for the application report *DS90UB97x-Q1 FPD-Link IV Power-Over-Coax Design Guidelines*.



The table below lists essential components for this particular PoC network.

Designator	Description	Part Number	Manufacturer
L1	Inductor, 100uH, 1400mΩ DCR, 450mA	LPS4018-104	Coilcraft
L2	Inductor, 6.8uH, 360mΩ DCR, 390mA	1205POC-682	Coilcraft
L3	Inductor, 180 nH, 210mΩ DCR, 900mA	PFL1005-181	Coilcraft
L4			
R1	2.61kΩ		
R2	3.6kΩ		
C1	0.1uF		
C2	10uF		

9.3.2 PoC Layout Considerations

In addition to the PoC network components selection, their placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of its pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.

- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the thru-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.
- Use coupled 100- Ω differential signal traces from the device pins to the ac-coupling caps. Use 50- Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9 Ω resistors.

9.3.3 PoC Noise Requirements

There are two separate noise requirements in a PoC network. The first requirement is on the side of the serializer measured at the input of the voltage regulator (denoted V_{poc} noise). The second requirement is on the deserializer side at R_{IN+} on the deserializer side (denoted R_{IN+} noise). It is imperative to make sure a system meets the PoC noise requirements in order to maintain good signal integrity in the link.

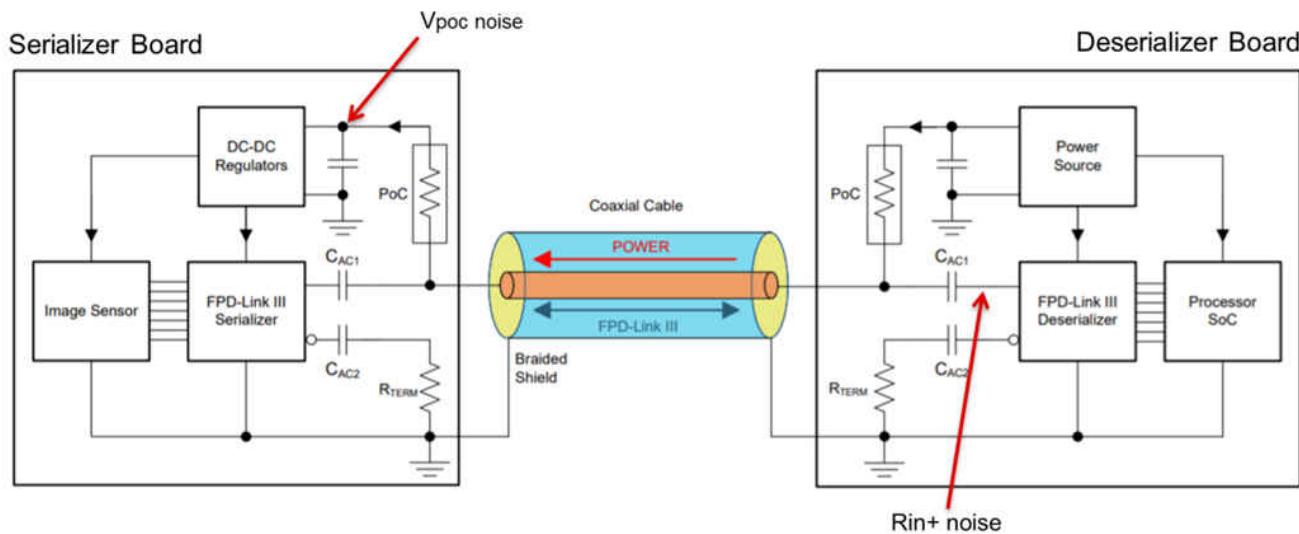


Figure 9-8. PoC Noise Measurements

V_{poc} noise is measured on the serializer board between the PoC network and the input of the voltage regulator. It should be measured with the deserializer, serializer, and imager powered on. The imager should be operating and providing data to the serializer, and the link should be running. The scope should be set to 0 - 50 MHz bandwidth.

Table 9-2. V_{poc} Noise Requirement

Parameter	Min	Typ	Max	Unit
V _{poc} Supply Noise			100	mVpp
V _{poc} Pulse (caused by imager sensor blanking and valid periods) @ imager refresh rate			500	mVpp
V _{poc} Pulse Slew Rate	100			us/V

R_{IN+} noise is measured on the deserializer board at the input of the R_{IN+} pin. It should be measured with the deserializer and serializer off (by pulling the PDB low). The scope should be set to 0 - 50MHz bandwidth.

Table 9-3. Rin Noise Requirement

Parameter	Min	Typ	Max	Unit
Rin Noise			10	mVpp

Increasing the V_{PoC} voltage and adding extra decoupling capacitance (> 10 μ F) can help reduce the amplitude and slew rate of V_{poc} fluctuations. For more information on PoC network selection and PoC noise, refer to application report DS90UB97x-Q1 FPD-Link IV Power-Over-Coax Design Guidelines

10 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The Pin Functions section provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Power Modes

The deserializer supports two main power modes: active mode and low power sleep mode.

10.1.1 Active Mode

In active mode, the deserializer operates normally.

10.1.2 Low Power Sleep Mode

In low power mode, the RX and CSI-2 ports are turned off, and the status of GPIO0, 1, 2, 5, 6, 7 are held. The device consumes less than 100mW of power in this mode.

Follow the below procedures to enter low power mode:

1. Ensure all supplies (VDD18, VDDIO, VDD11, and PDB) are stable
2. Write b'1 to GPIO_HOLD_B register bit
3. Write GPIO registers for desired output
4. Write b'0 to GPIO_HOLD_B register bit
5. Shut off external VDD11 supply

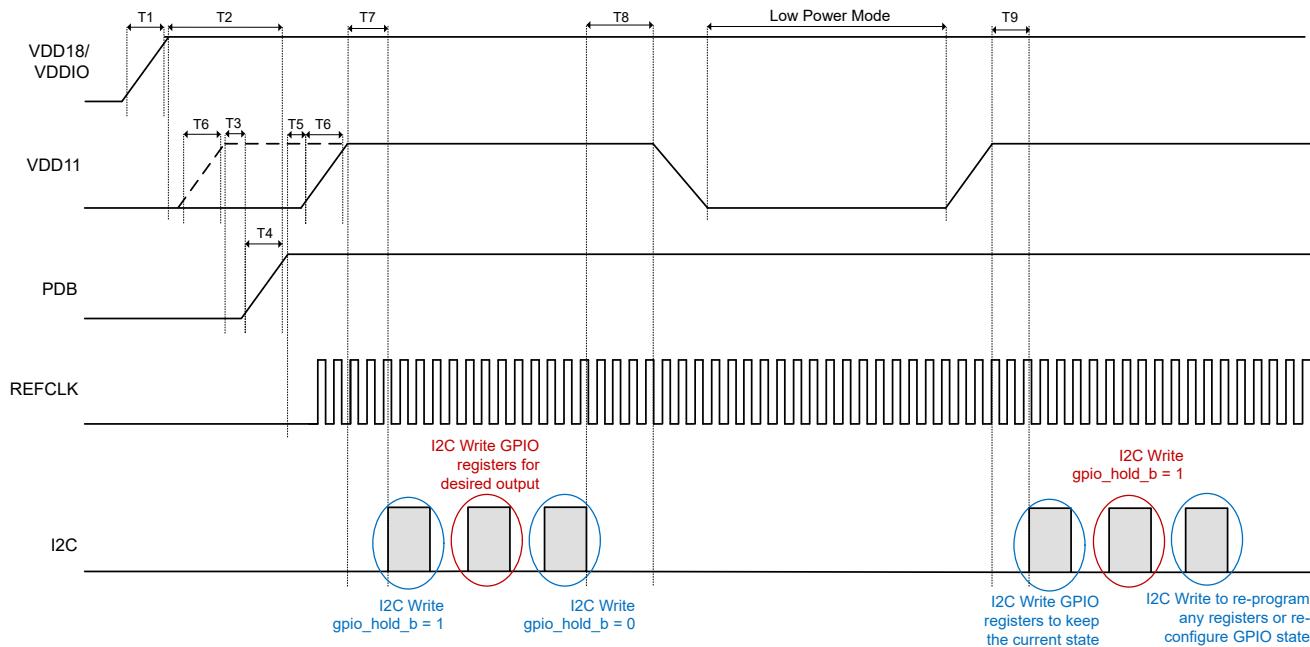
Follow the below procedures to exit low power mode:

1. Turn on VDD11 supply and wait for the supply to stabilize
2. Write GPIO registers to keep the current output state
3. Write b'1 to GPIO_HOLD_B register bit
4. Reprogram any registers or reconfigure the GPIO registers

Refer to [Section 10.1.3](#) for detailed timing requirements

10.1.3 Power-up Sequencing

[Figure 10-1](#) illustrates the power-up sequence requirements for the deserializer. VDD18 and VDDIO should come up before PDB, and PDB can come up before or after VDD11. During low power mode, VDD11 should be shut down, and all other signals can be kept ON.

**Figure 10-1. Power-up Sequence with Low Power Sleep Mode****Table 10-1. Power-up Sequence Timing Requirements**

Time	Description	Min	Typ	Max
T1	VDD18/VDDIO rise time (10% to 90%)	100us		
T2	VDD18 stable to PDB VIH	50us		
T3 ¹	VDD11 stable to PDB			
T4	PDB rise time (10% to 90%)	100us		
T5 ¹	PDB VIH to VDD11 applied			
T6	VDD11 rise time (10% to 90%)	100us		
T7	All supplies stable to first I2C transaction	2ms		
T8	I2C write to enter low power mode to bringing down VDD11	100us		
T9	VDD11 stable to first I2C transaction	2ms		

1. VDD11 can come up either before or after PDB.

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50- μ F to 100- μ F range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coaxial interconnect.

11.1.1 CSI-2 Guidelines

DPHY:

1. Route CSIx_D*P/N pairs with controlled 100- Ω differential impedance ($\pm 10\%$)
2. Keep away from other high-speed signals.
3. Keep length difference between a differential pair to 5 mils of each other.
4. Length matching should be near the location of mismatch.
5. Match trace lengths between pairs to be < 5 mils.
6. Each pair should be separated at least by 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer.
9. Keep the number of VIAS to a minimum — TI recommends keeping the VIA count to 2 or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the VQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP.

Example PCB layout is used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

These PCB layout examples are derived from the layout design of the DS90UB9702-Q1EVM Evaluation Board. The graphic and layout description are used to determine proper routing when designing the board. The high-speed FPD-Link III traces routed differentially up to the connector. A 100- Ω differential characteristic impedance and 50- Ω single-ended characteristic impedance traces are maintained as much as possible for both STP and coaxial applications. For the layout of a coaxial interconnects, coupled traces should be used with the RINx-termination near to the connector.

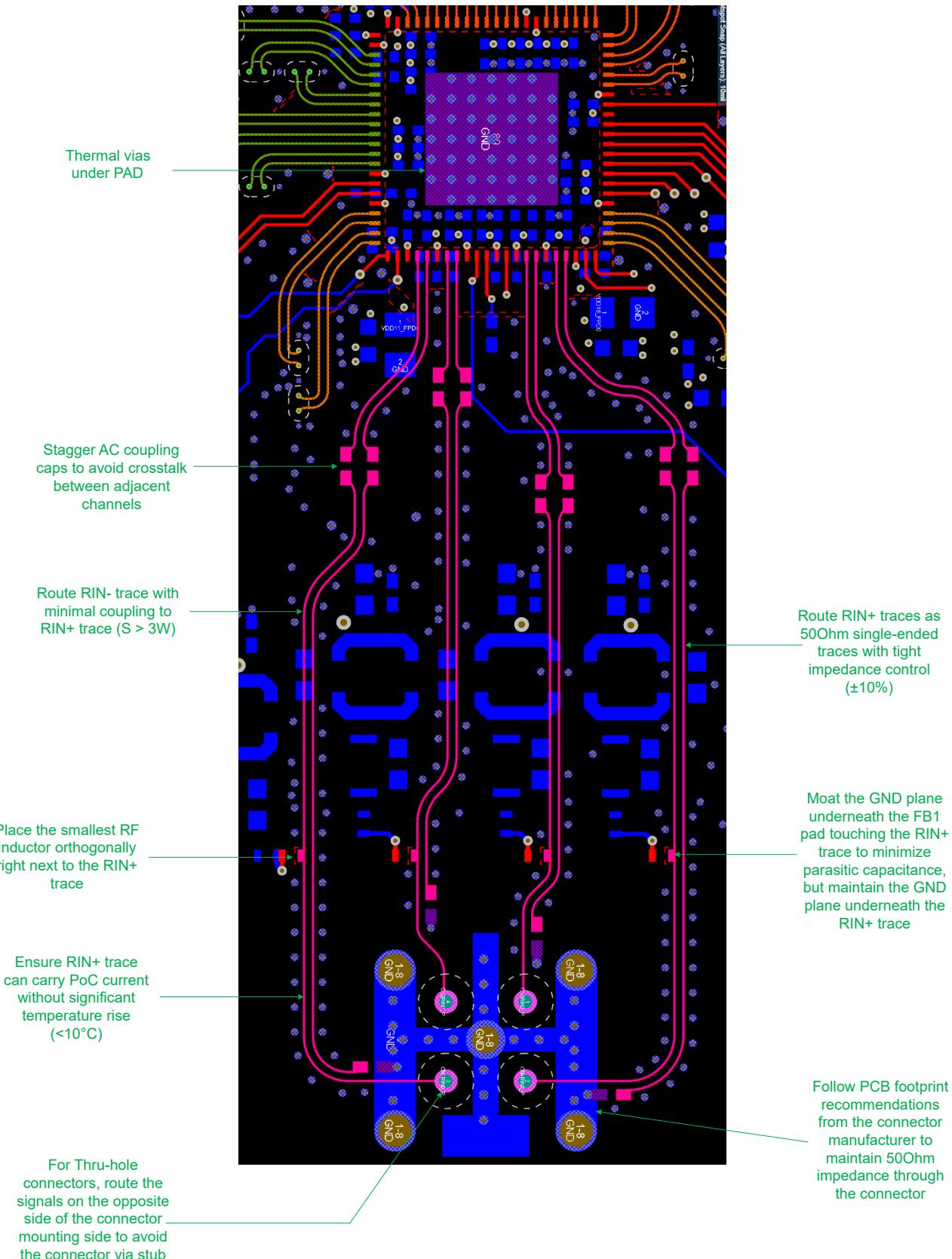
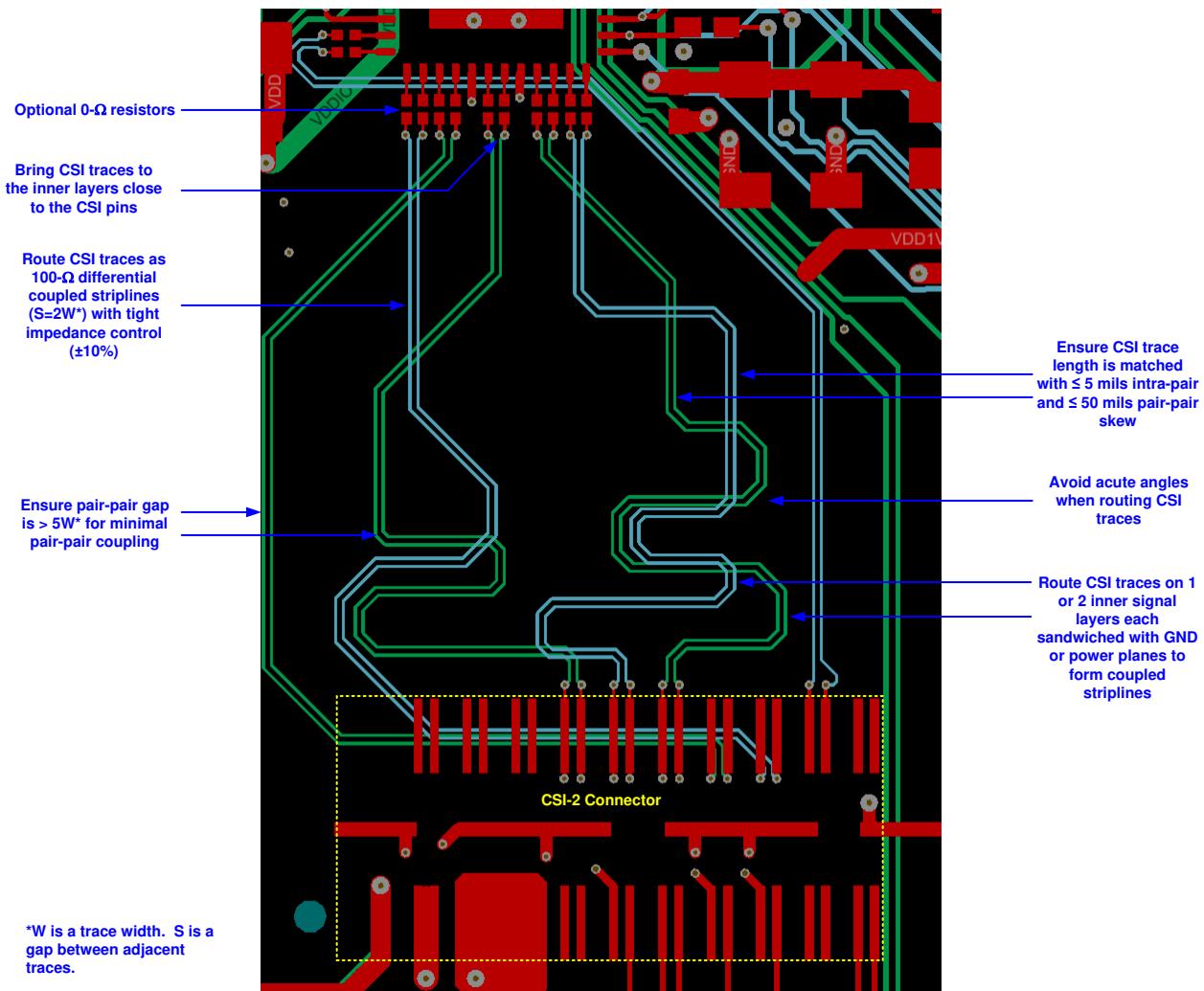


Figure 11-1. DS90UB9702-Q1 Example PCB Layout With Quad Mini-Fakra Connector


Figure 11-2. Example Routing of CSI-2 Traces

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [I²C Communication Over FPD-Link III with Bidirectional Control Channel](#)
- [I²C Bus Pull-Up Resistor Calculation](#)

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁴⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking
DS90UB9702T RURRQ1	ACTIVE	VQFNP	RUR088A	88	2500	RoHS & Green	Contact TI	Contact TI	-40 to 105	UB9702
DS90UB9702T RURTQ1	ACTIVE	VQFNP	RUR088A	88	250	RoHS & Green	Contact TI	Contact TI	-40 to 105	UB9702

- (1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

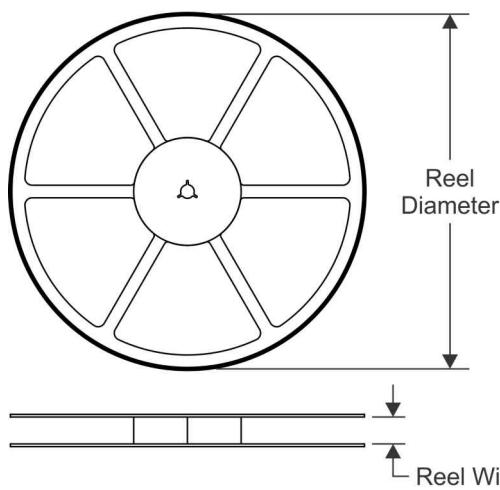
- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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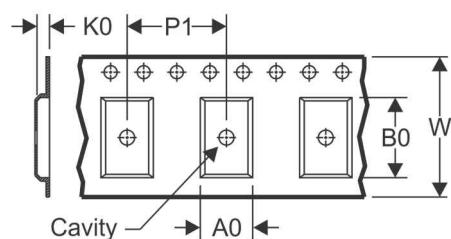
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13.2 Tape and Reel Information

REEL DIMENSIONS

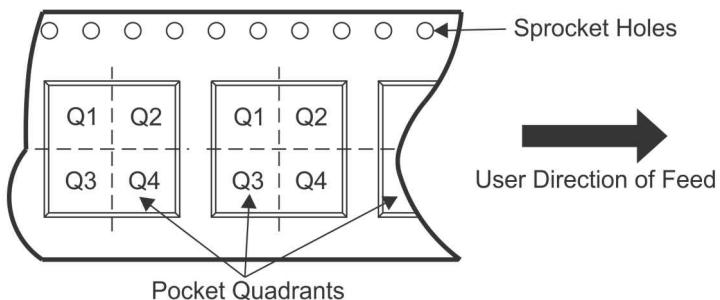


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

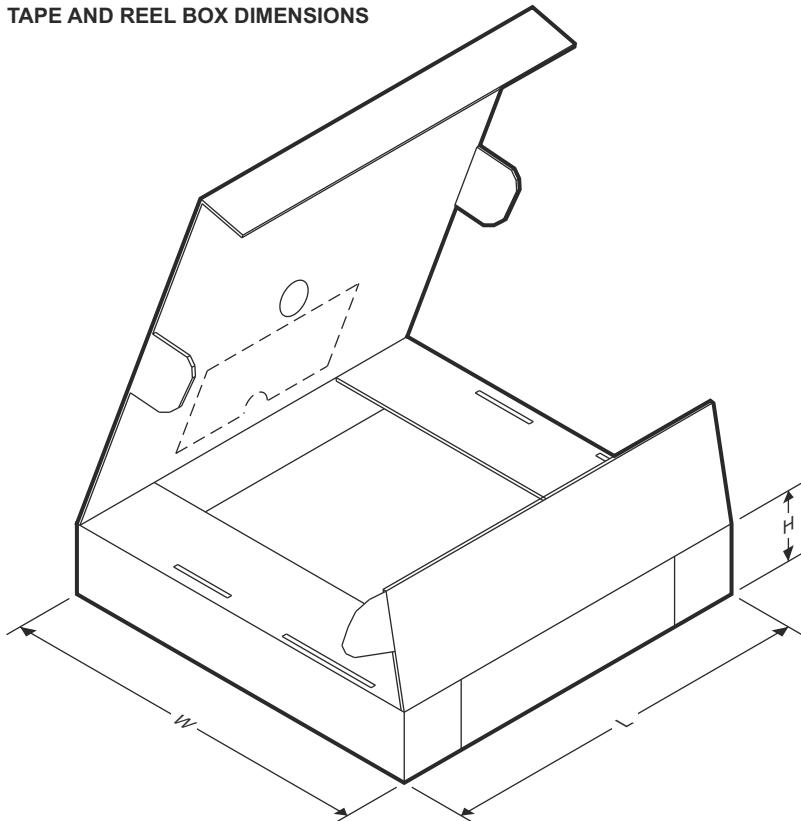
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



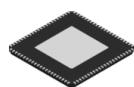
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB9702TRURRQ1	VQFNP	RUR0088E	88	2500	330	24.4	12.3	12.3	1.1	16	24	2
DS90UB9702TRURTQ1	VQFNP	RUR0088E	88	250	180	24.4	12.3	12.3	1.1	16	24	2

DS90UB9702-Q1
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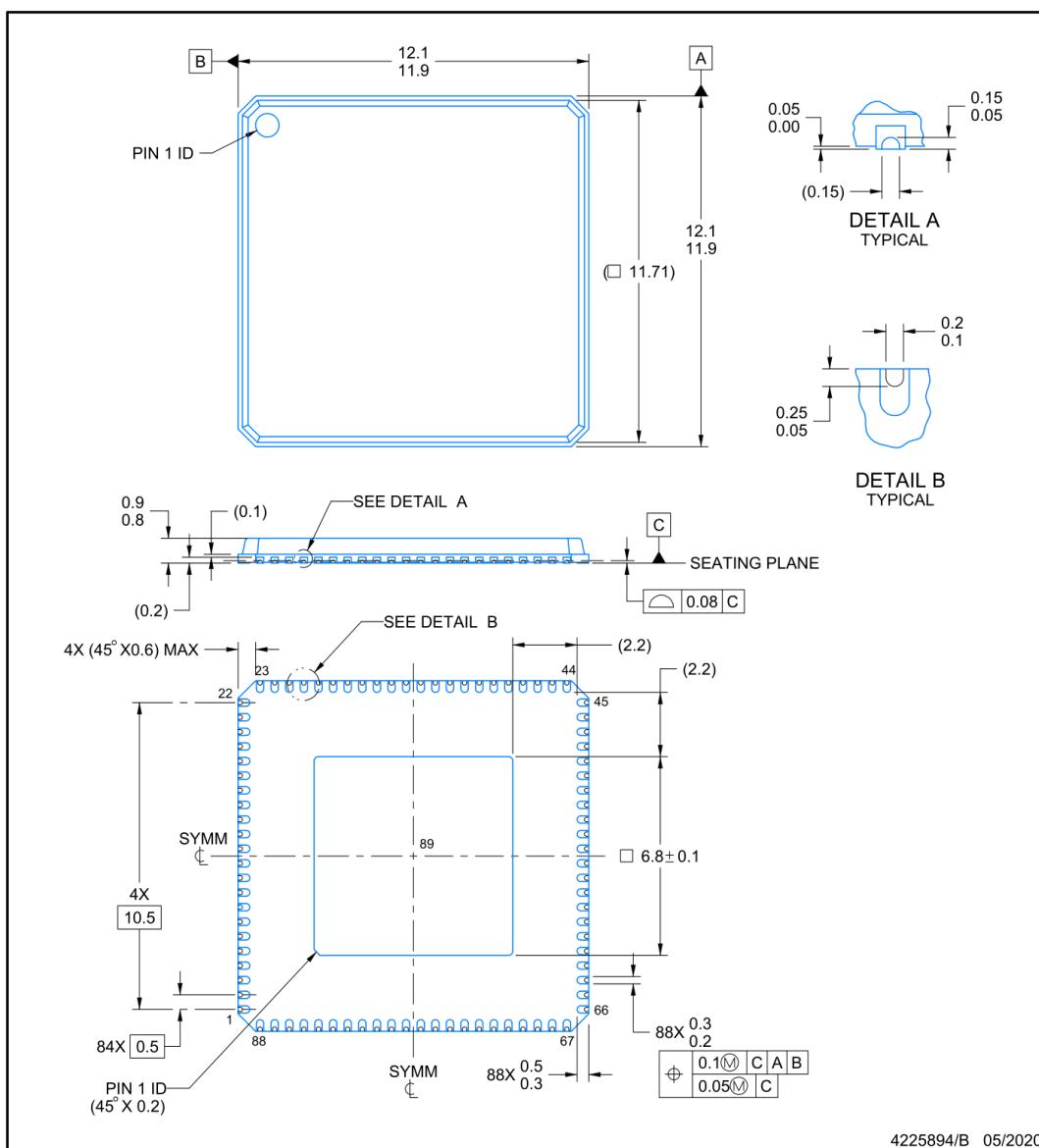
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB9702TRURRQ1	VQFNP	RUR0088E	88	2500	380	153	87
DS90UB9702TRURTQ1	VQFNP	RUR0088E	88	250	380	153	87

RUR0088E**PACKAGE OUTLINE****VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

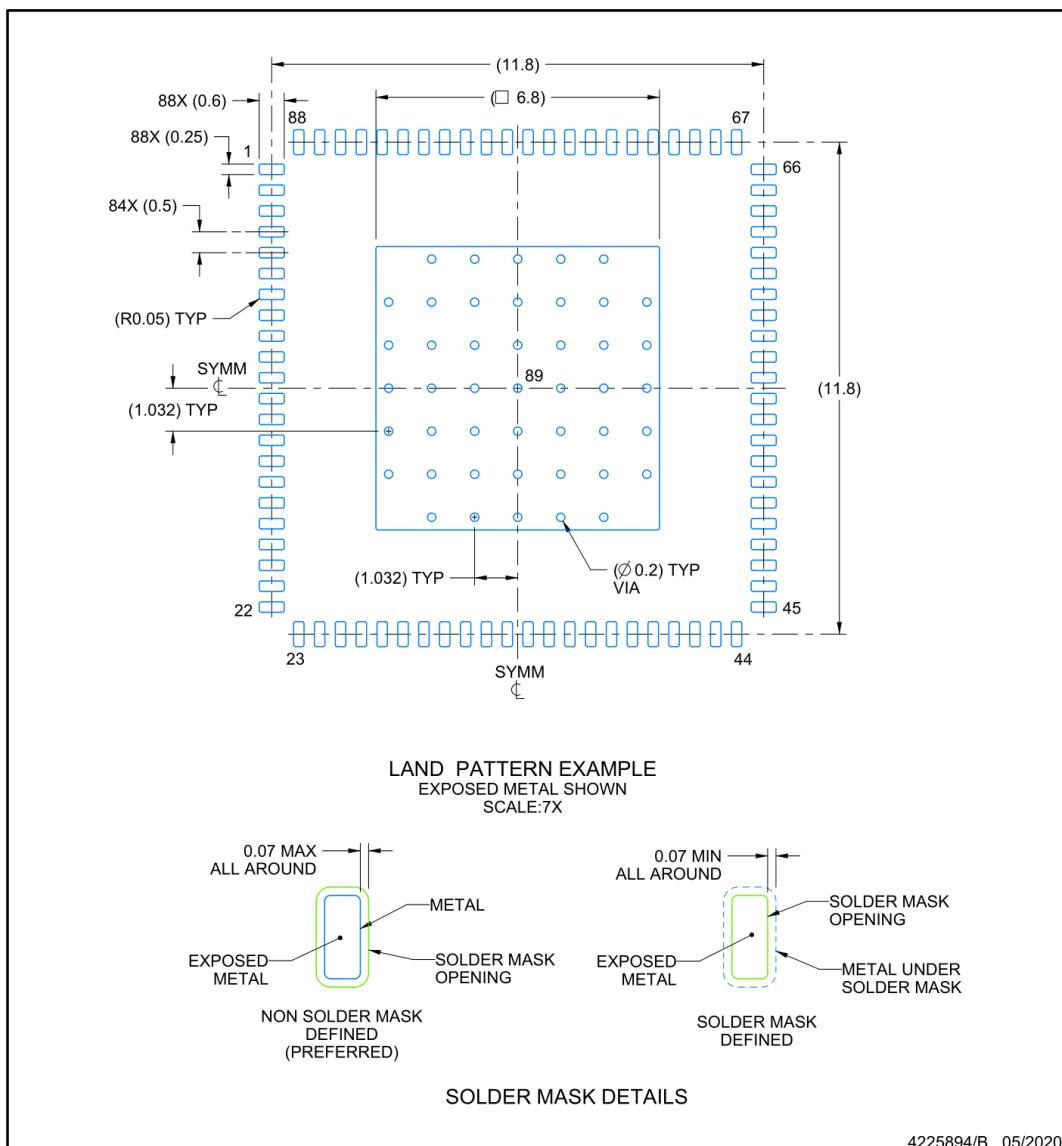
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RUR0088E

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



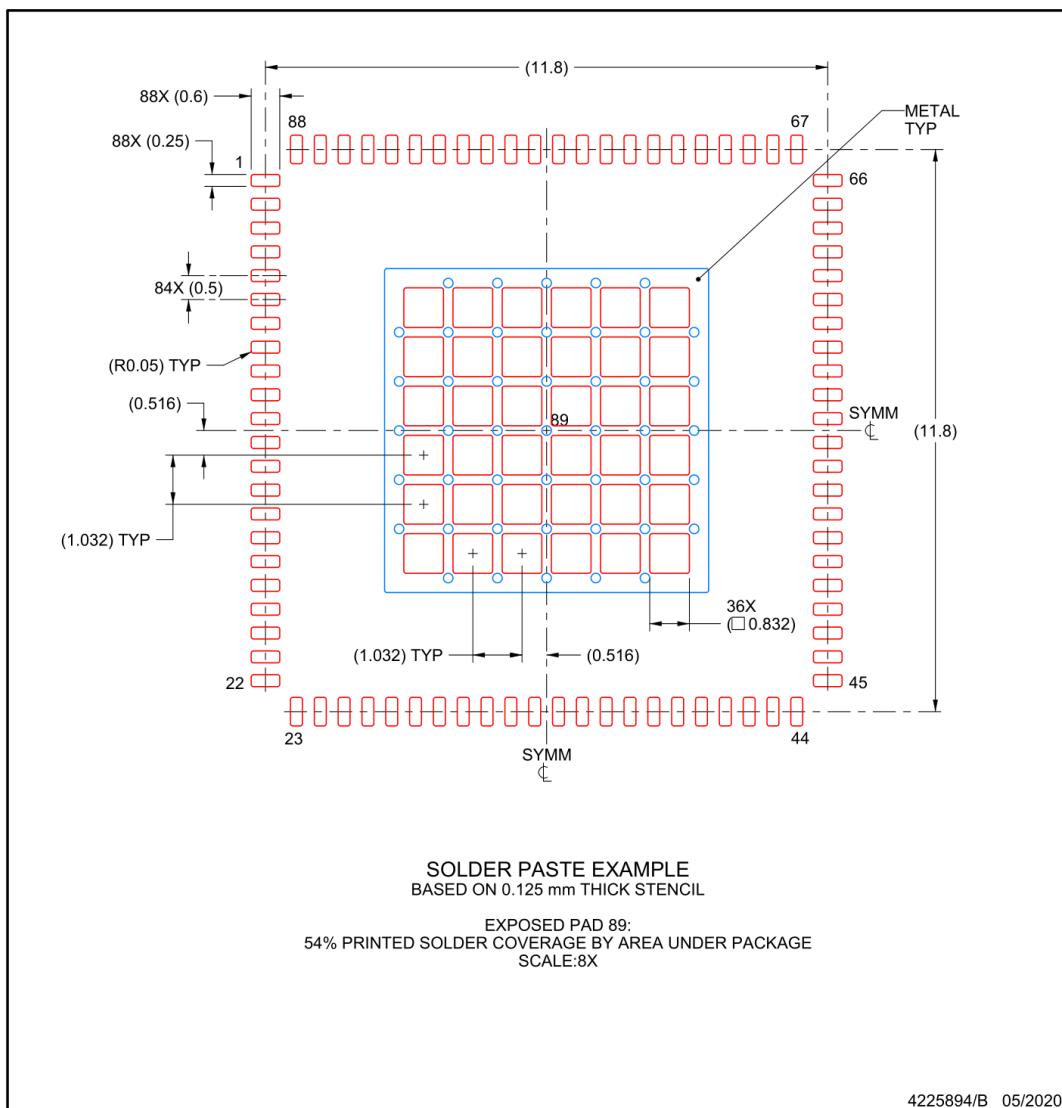
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUR0088E
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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