CptS260: Introduction to Computer Architecture - Homework 5

Jocelyn Strmec. **Due: Sunday 11/08/2020 @ 11.59 pm**

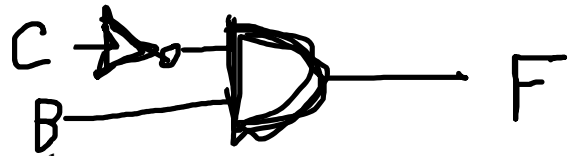
What and how to submit: *Please submit your zipped folder to* ***blackboard*** *by the due date.*

1. Write a Boolean SOP expression for this truth table, then simplify that expression as much as possible. Draw the circuits for simplified expressions.

a.

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

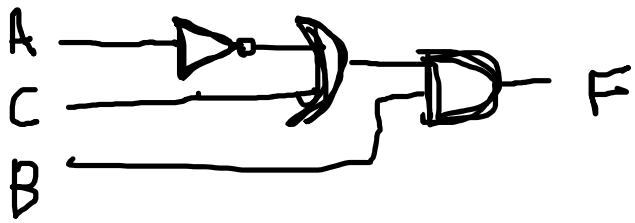
F=A'BC' +ABC'=(A'+A)BC'=BC'



b.

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

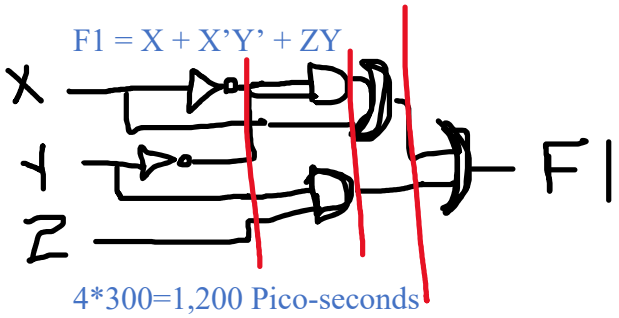
F=A'BC'+A'BC+ABC=A'B(C'+C)+ABC=A'B+ABC=B(A'+AC)= B(A'+C)



2. Simplify the below expressions:

   a. $F1 = X + X'Y' + ZY$

   F1 = X + X'Y' + ZY

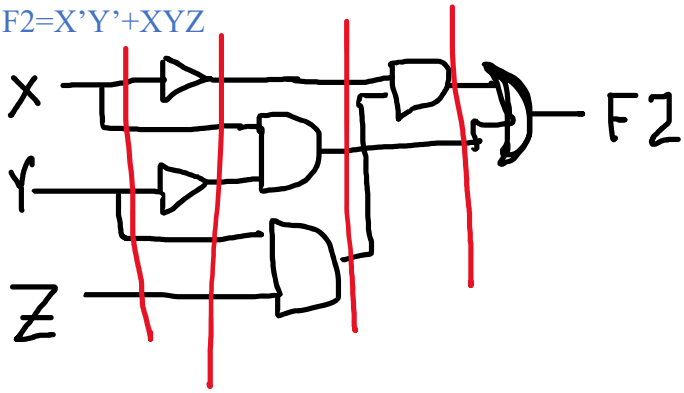


   4*300=1,200 Pico-seconds

   b. $F2 = X'Y' + X' + XYZ$

   F2=X'(Y'+1)+XYZ

   F2=X'Y'+XYZ



   4*300=1,200 Pico-seconds

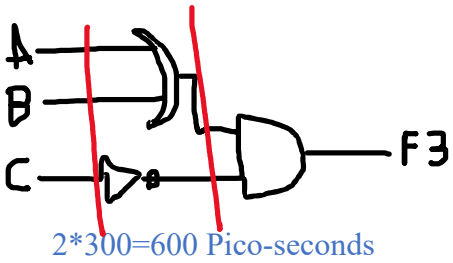
   c. $F3 = A'B'C' + AB'C' + A'BC'$

   F3 = A'C'(B'+B)+AB'C'

   F3 = A'C'+ABC'

   F3 = C'(A'+AB)

   F3 = C'(A+B)



   2*300=600 Pico-seconds

   d. Draw the circuits for simplified expressions using only two input NOT/OR/AND gates from part a, b, and c.

   e. What is the latency of each digital circuit in a, b, and c when the latency for each gate is 300 ps.

3. In this problem, you should design a two-bit comparator. This circuit should have three outputs named l, g, and eq. The circuit should get two digits binary numbers (00, 01, 10, 11), and the output should change based on these rules:

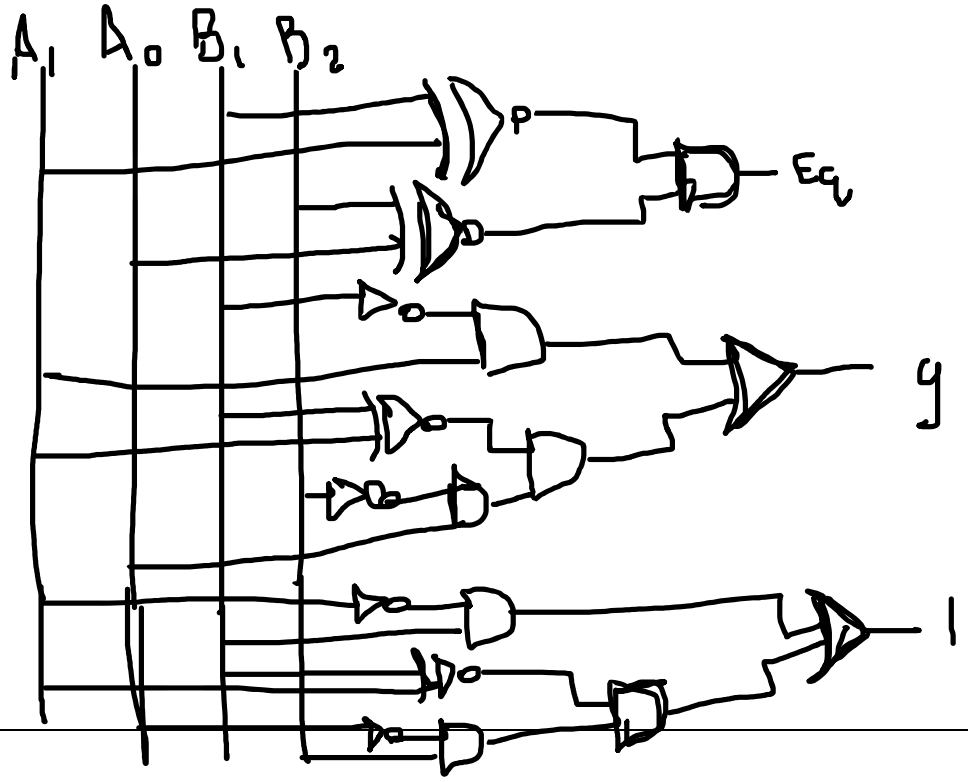
- If first number > second number then g = 1, l = 0, and eq = 0
- If first number < second number then g = 0, l = 1, and eq = 0
- If first number = second number then g = 0, l = 0, and eq = 1

Your circuit will have 4 input (2 bit for the first number, and 2 bits for the second number)

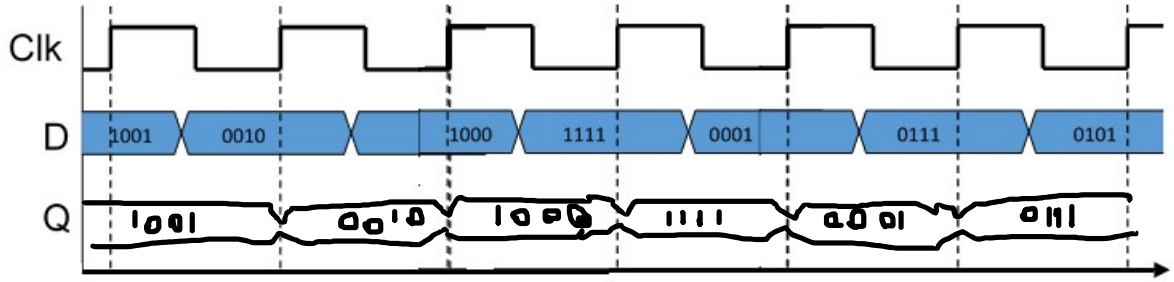
a. Draw the truth table for the comparator for unsigned numbers

A	B	G	L	EQ
00 $(0)_d$	00 $(0)_d$	0	0	1
00 $(0)_d$	01 $(1)_d$	0	1	0
00 $(0)_d$	10 $(2)_d$	0	1	0
00 $(0)_d$	11 $(3)_d$	0	1	0
01 $(1)_d$	00 $(0)_d$	1	0	0
01 $(1)_d$	01 $(1)_d$	0	0	1
01 $(1)_d$	10 $(2)_d$	0	1	0
01 $(1)_d$	11 $(3)_d$	0	1	0
10 $(2)_d$	00 $(0)_d$	1	0	0
10 $(2)_d$	01 $(1)_d$	1	0	0
10 $(2)_d$	10 $(2)_d$	0	0	1
10 $(2)_d$	11 $(3)_d$	0	1	0
11 $(3)_d$	00 $(0)_d$	1	0	0
11 $(3)_d$	01 $(1)_d$	1	0	0
11 $(3)_d$	10 $(2)_d$	1	0	0
11 $(3)_d$	11 $(3)_d$	0	0	1

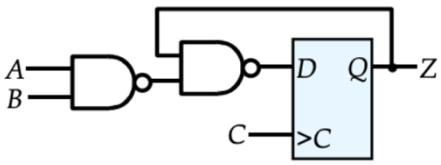
1. (**Extra Credit**) Show the circuit.

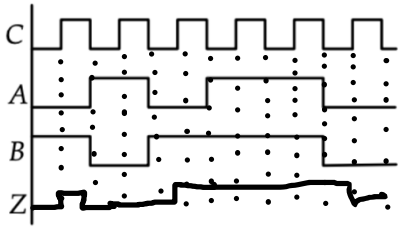


4. Assume you have an edge-triggered register with four bits. Fill out the output waveform data based on clk and input data (D).



5. Consider the positive edge triggered sequential circuit shown below. Fill in the waveform for output Z in the timing diagram.





D=((AB)'*Z)'=(AB'' +X')=AB+Z'

A	B	Z	D
1	1	1	1
1	1	0	1
1	0	1	0
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	0
0	0	0	1