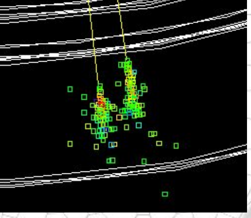


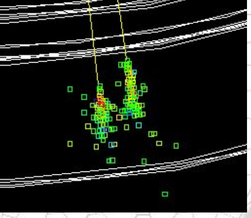
SiD ECal Progress

M. Breidenbach, D. Freytag, N. Graf, G. Haller, R. Herbst,
M. Oriunno, A. Tormada,K. Skarpaas, A. Dragone
SLAC National Accelerator Laboratory

J. Brau, R. Frey, C. Gallagher, D. Strom,
J. Barkeloo, A. Steinhebel (grad students),
U. Oregon, Eugene

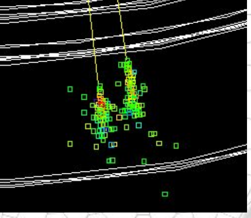
C. Neher, M. Tripathi
UC Davis

B. Schumm, L. d‘Hautuille (undergrad student)
UC Santa Cruz

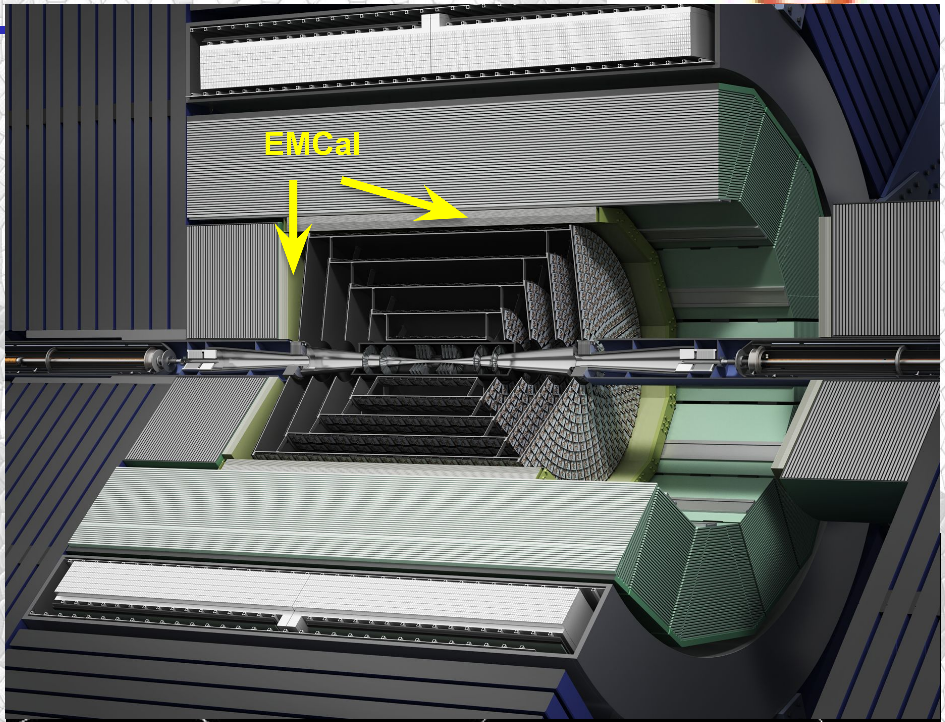


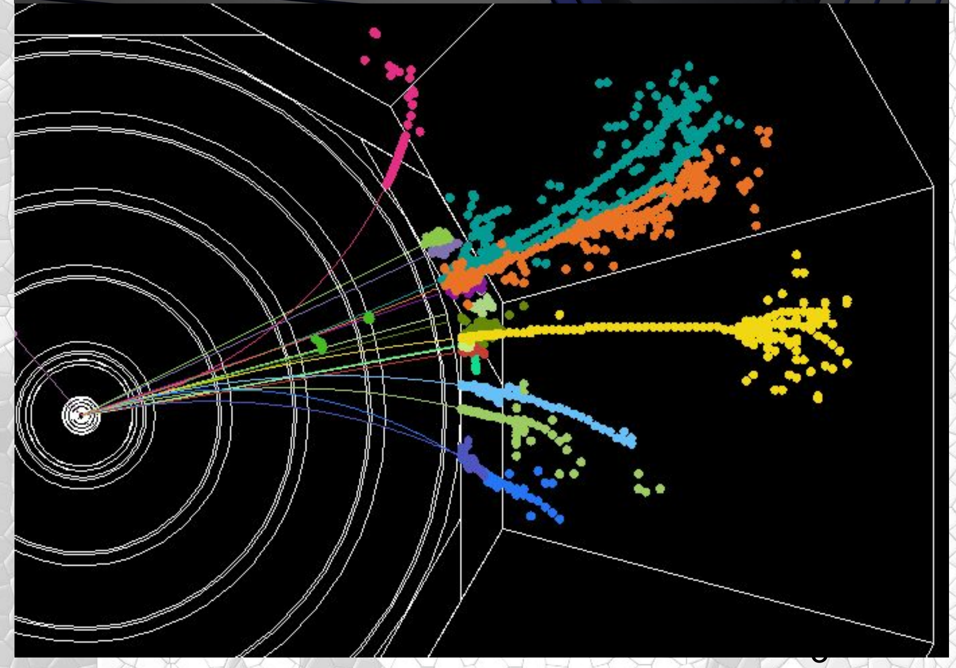
Outline

- Design Overview
- Mechanical Progress
- Beam Test & Simulation
- Sensor Upgrade Design
- Full Detector Simulation
- Future Studies



Particle Flow Calorimetry





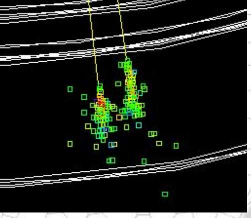
SiD is designed for Particle Flow Calorimetry: to measure all final states with precision

Promises superb jet energy resolution

- Tracker measures charged momentum
- Calorimeters measure neutral energy after excluding energy from charged tracks
- <u>Fine segmentation required!</u>
- Current invariant mass resolution <4% Z's to light quarks at ILC500

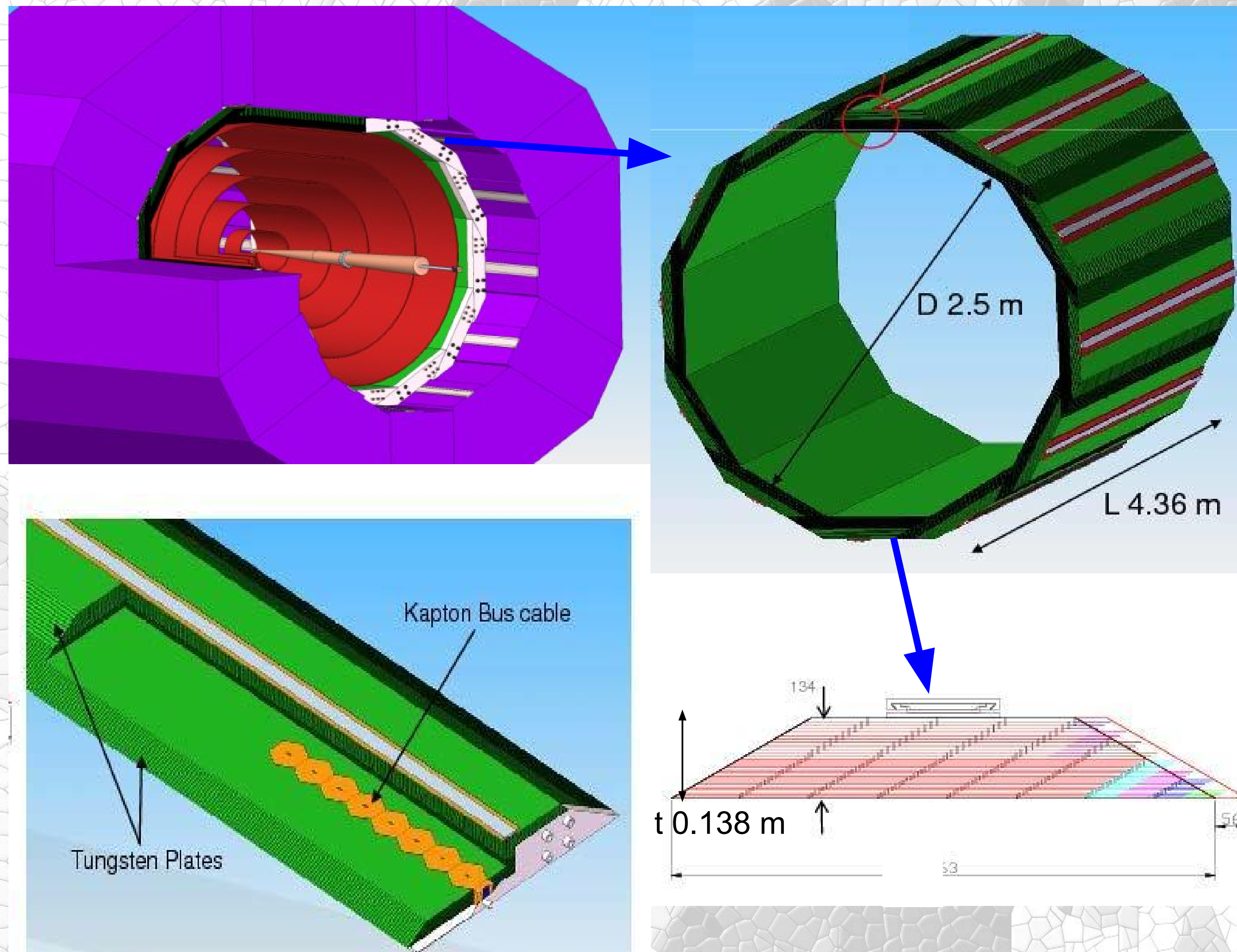
"Imaging ECal" is critical element

SiD has been developing a silicon-tungsten calorimeter to achieve the highly granular ECal requirements of the PFA concept



The SiD ECal Baseline

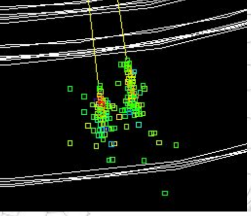
An imaging calorimeter: 30 layers tungsten interleaved with 30 layers pixelated silicon



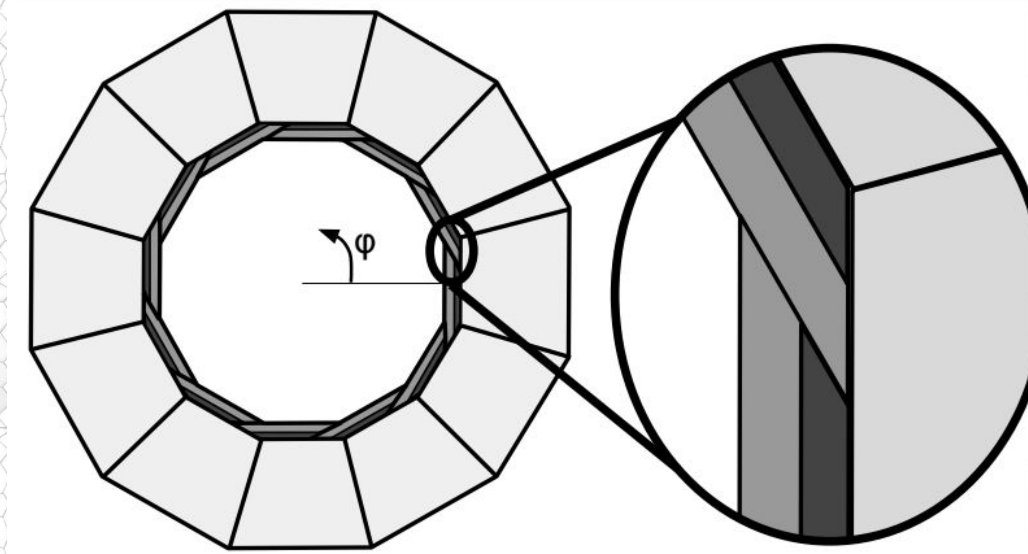
__DBD Baseline configuration:__

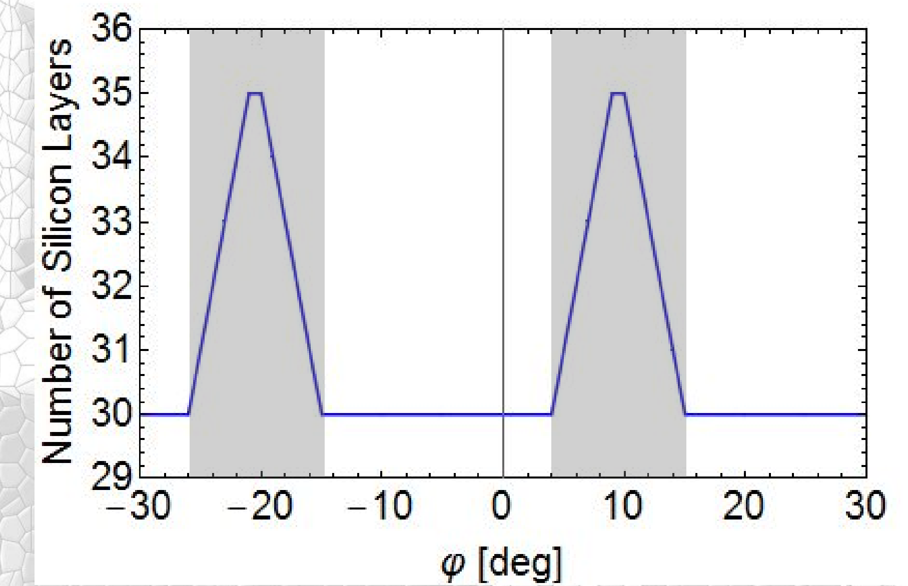
- transverse: 13 mm^2 pixels
- longitudinal: $(20 \times 0.65\ X_0) + (10 \times 1.30\ X_0)$ $\Rightarrow$ 17%/√(E)
- 1.25 mm readout gaps ⇒ 13 mm effective Molière radius

(preconceptual design)

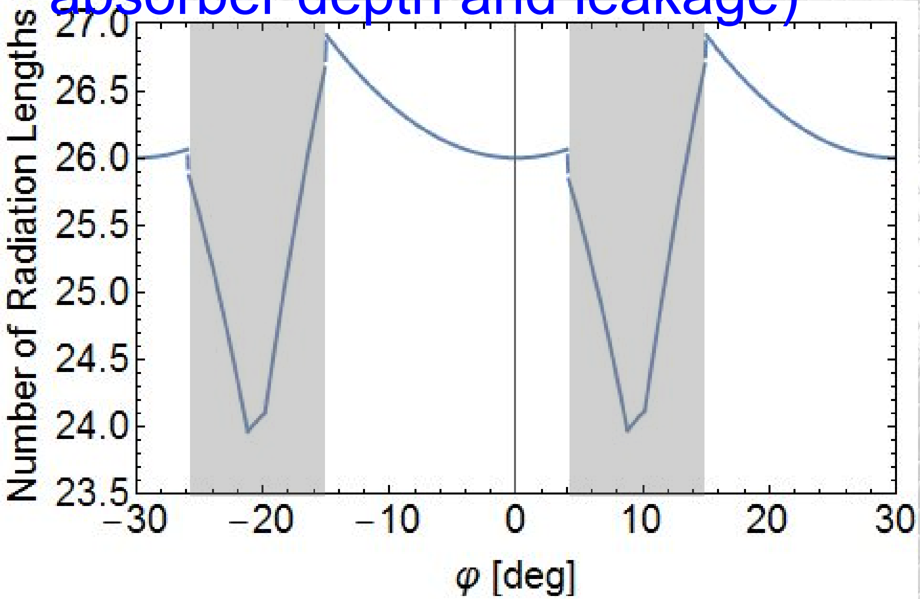


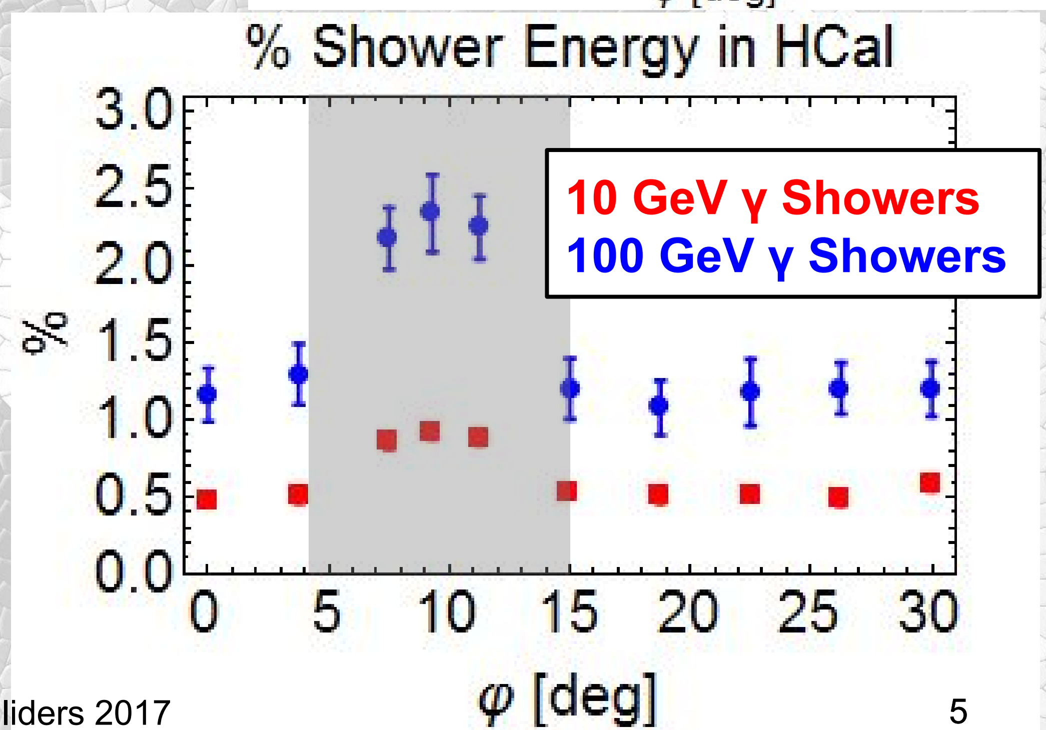
ECal Barrel Geometry Effects

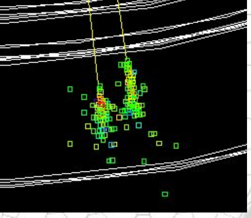




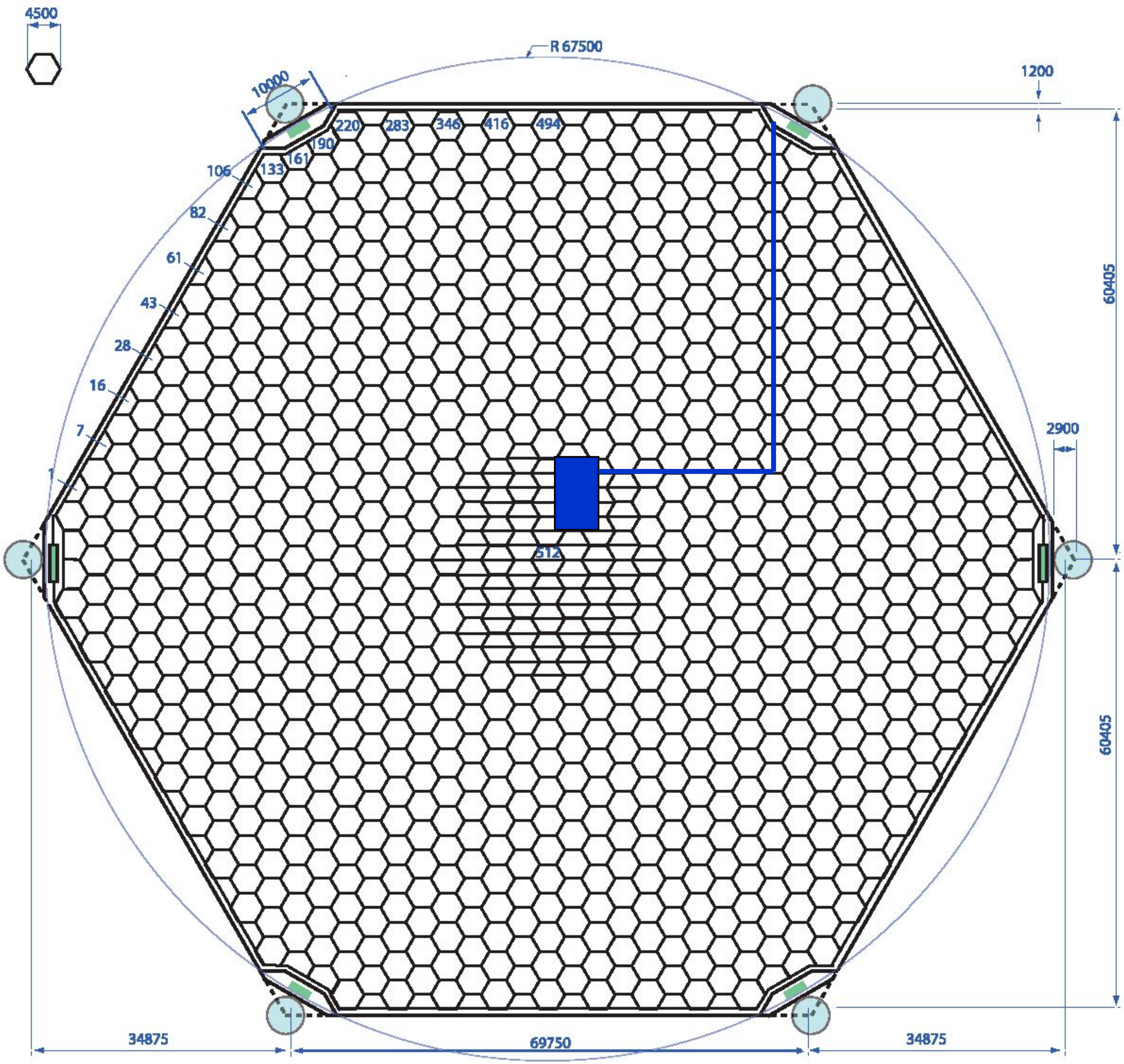
Geometry leaves physical effects (varied absorber depth and leakage)





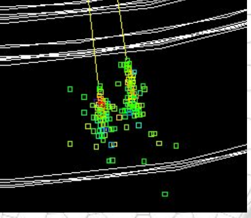


Si Sensors



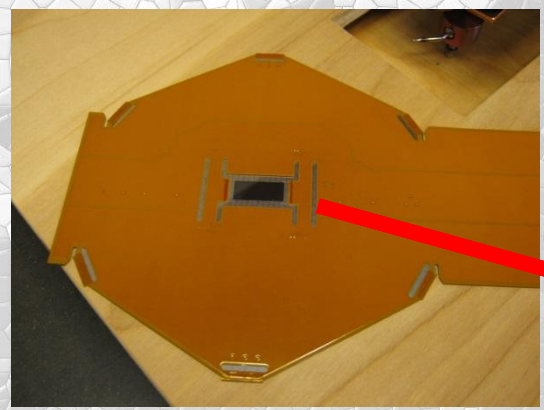
- 6 inch wafers
- 1024 13 mm^2 pixels
- KPiX readout and cable are bump-bonded directly to sensor

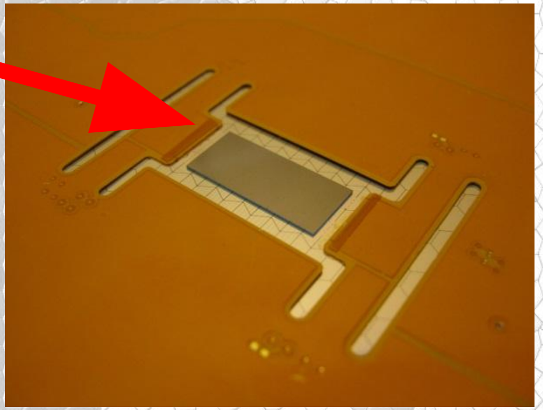
KPiX ASIC & sample trace

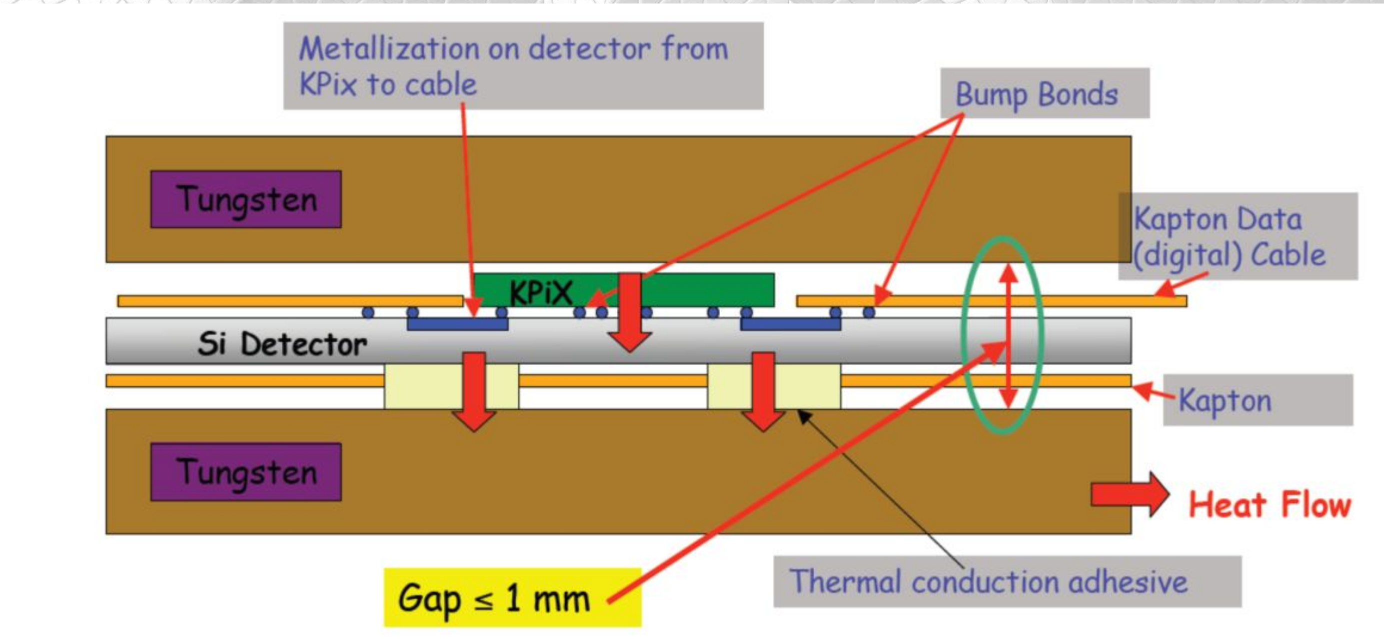


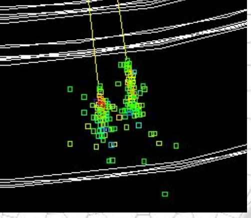
Gap Structure

- 1.25 mm gap: minimize Molière radius (13 mm effective), keep calorimeter compact
- Tungsten plates thermal bridge to cooling on edge



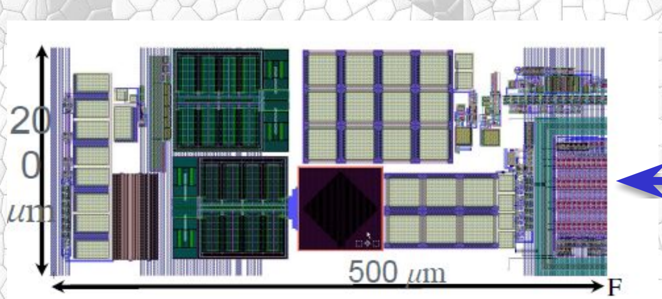




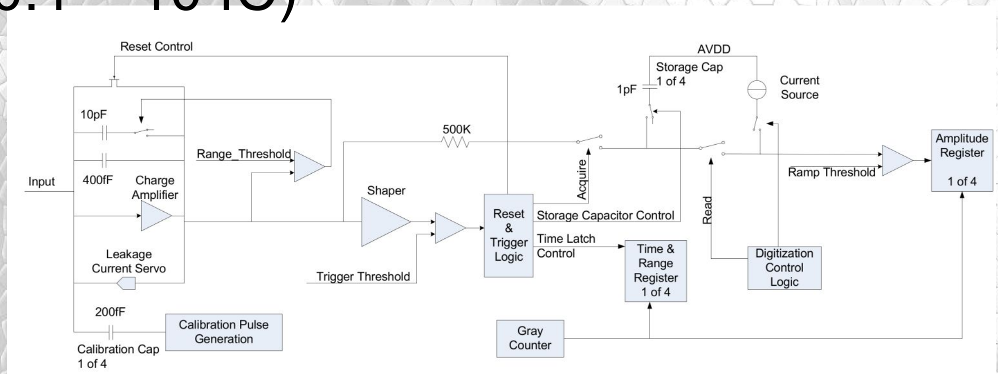


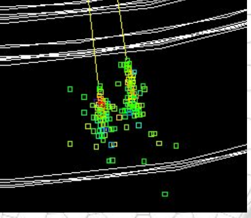
KPiX – System on a Chip

- KPiX is a 1024 channel ASIC to bump bond to Si detectors (Si Tracker and ECal), optimized for the ILC (1 ms trains, 5 Hz rate):
  - Low noise dual range charge amplifier w/ 17 bit dynamic range.
  - Power modulation w/ average power <20 µW/channel (ILC mode, front-end power down during inter-train periods).
  - Up to 4 measurements during ILC train; each measurement is amplitude and bunch number.
  - Digitization and readout during the inter-train period (199 ms)
  - Internal calibration system, pixel level trigger
  - Noise Floor: 0.15 fC (1000 e^-)
  - Peak signal (Auto-ranging) 10 pC
  - Trigger Threshold Selectable (0.1 – 10 fC)



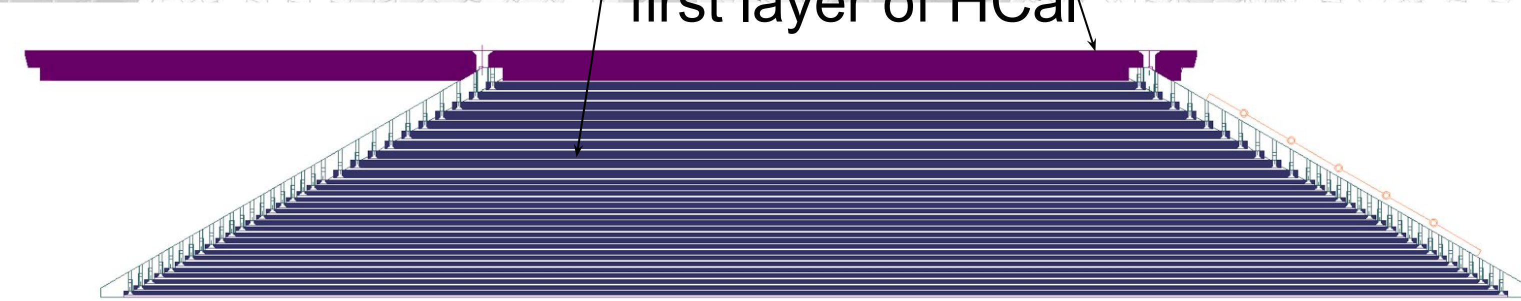
One pixel,
200 x 500 µm^2



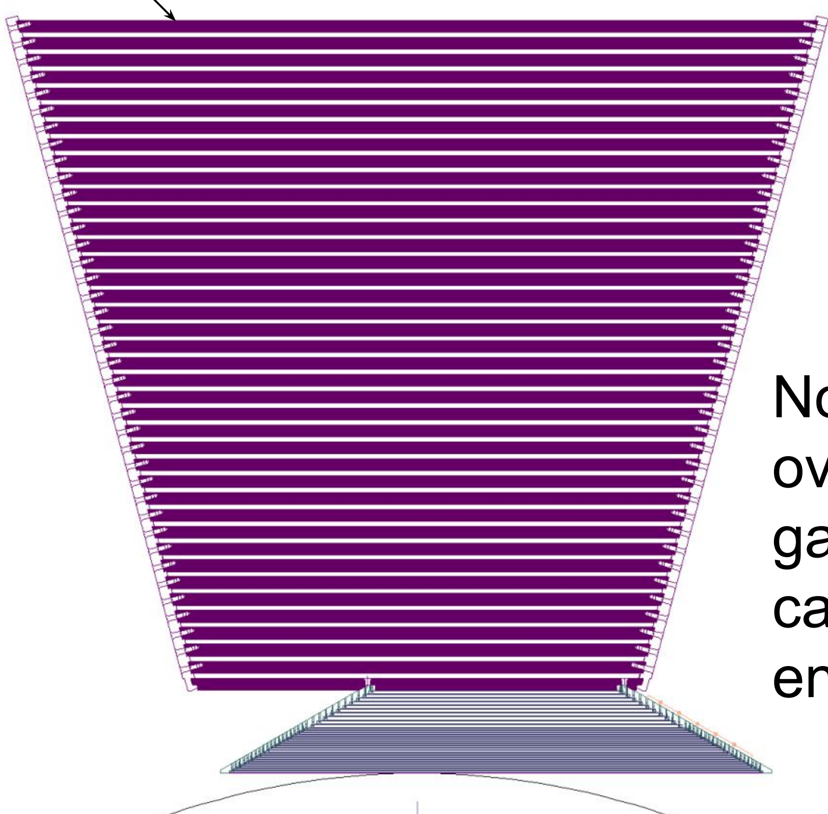


Mechanical Progress

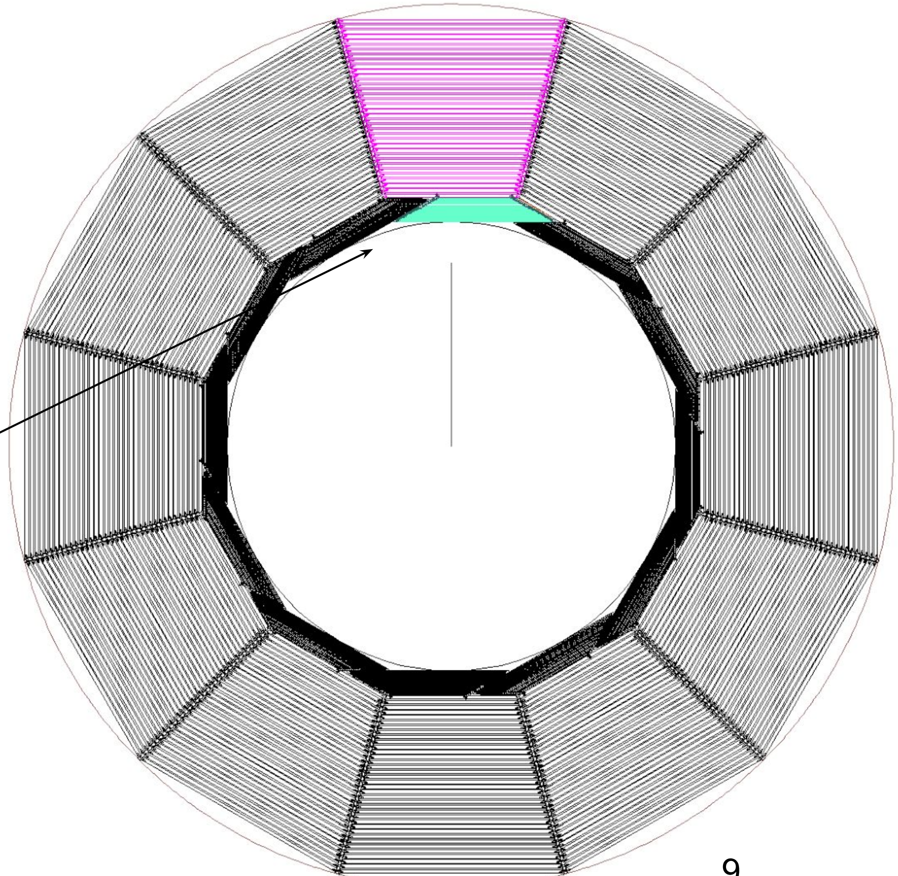
ECal module is built on first layer of HCal

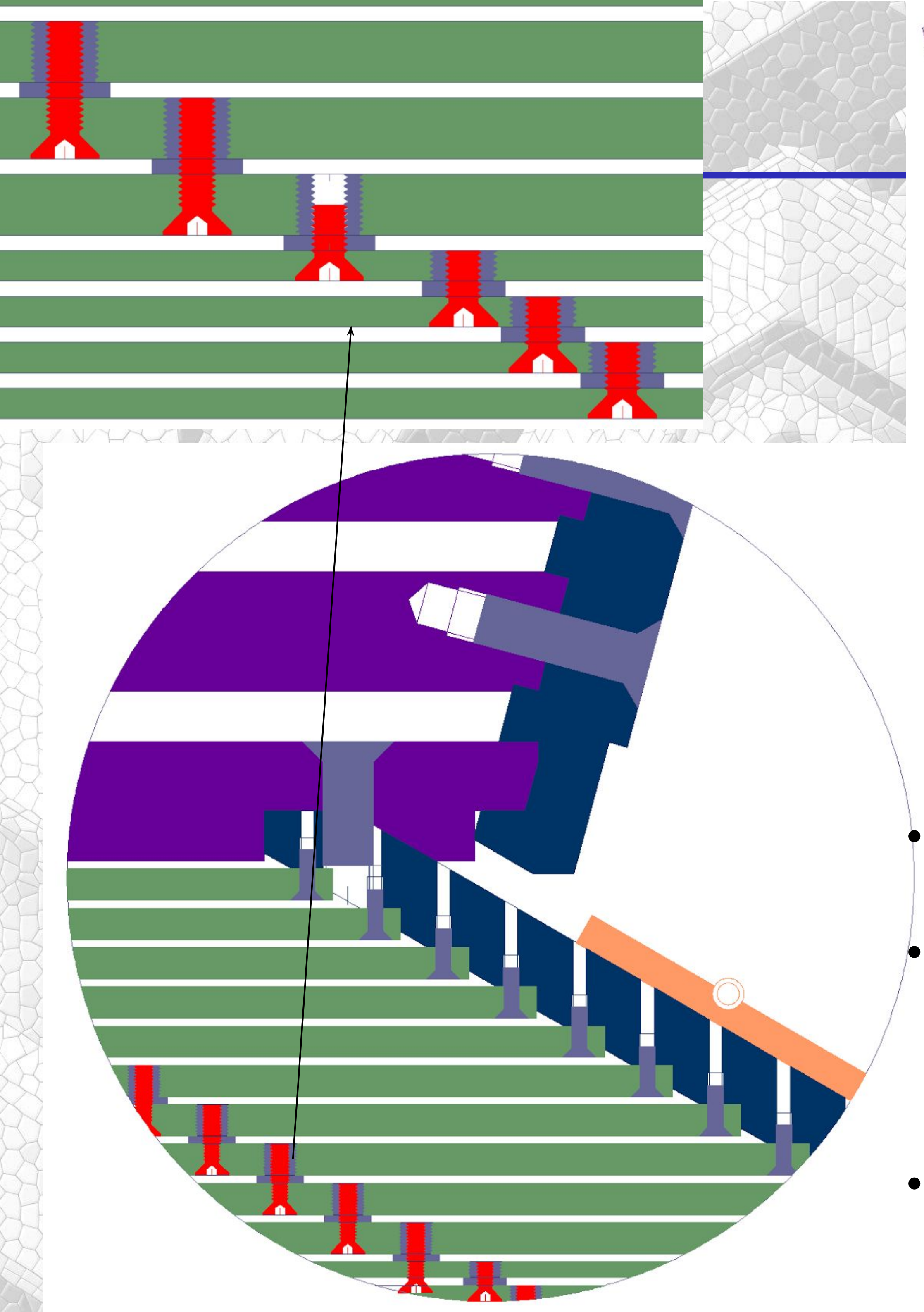


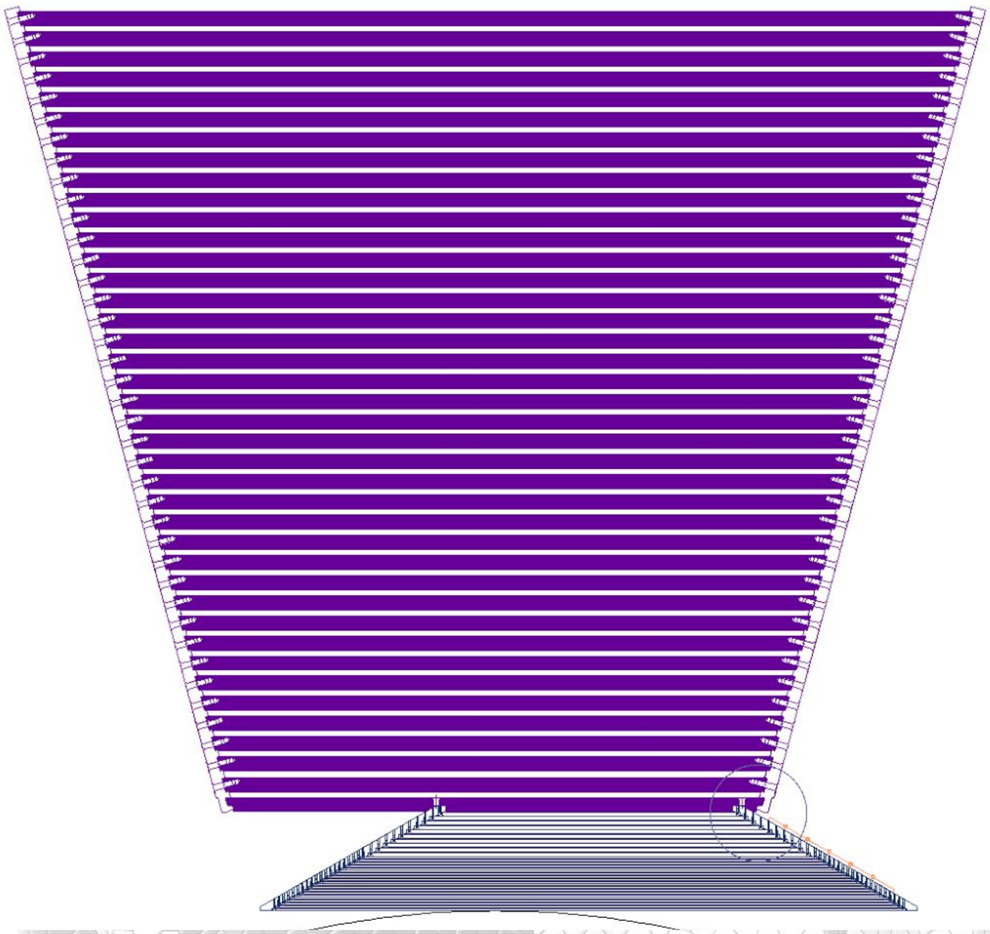
HCal module supports ECal module



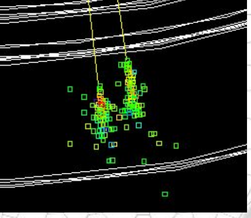
Note module overlap: No gaps; service cables at ends.





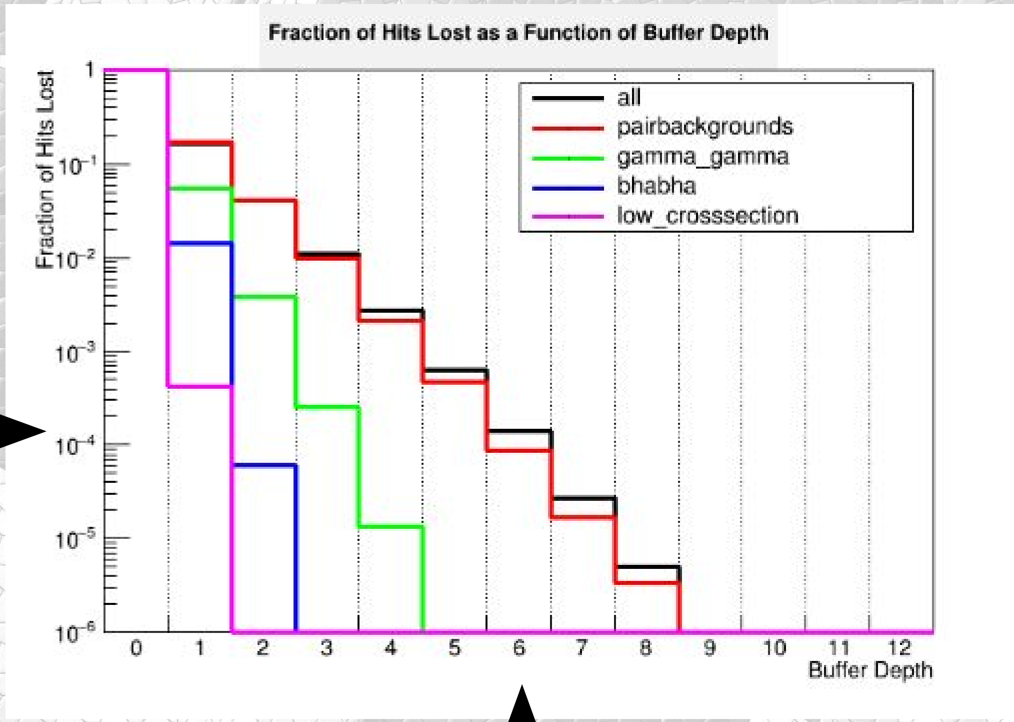


- HCal plates supported by interlaced grooved straps
- ECal plates screwed to support plates tied to inner HCal plate. Inner HCal plate “belongs” to ECal module.
- Tungsten plates tied to each other with plausible screws and spacers

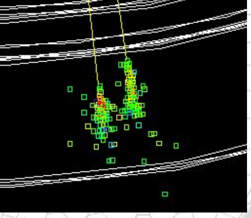


KPiX Buffer Multiplicity

- Long known that BeamCal required BEAN chip, which digitizes every pulse.
- Forward multiplicity might be more than 4 buffer KPiX (current design) could handle
  - Recent optimization studies indicate that 6 buffers will be adequate, taking into account all known processes.

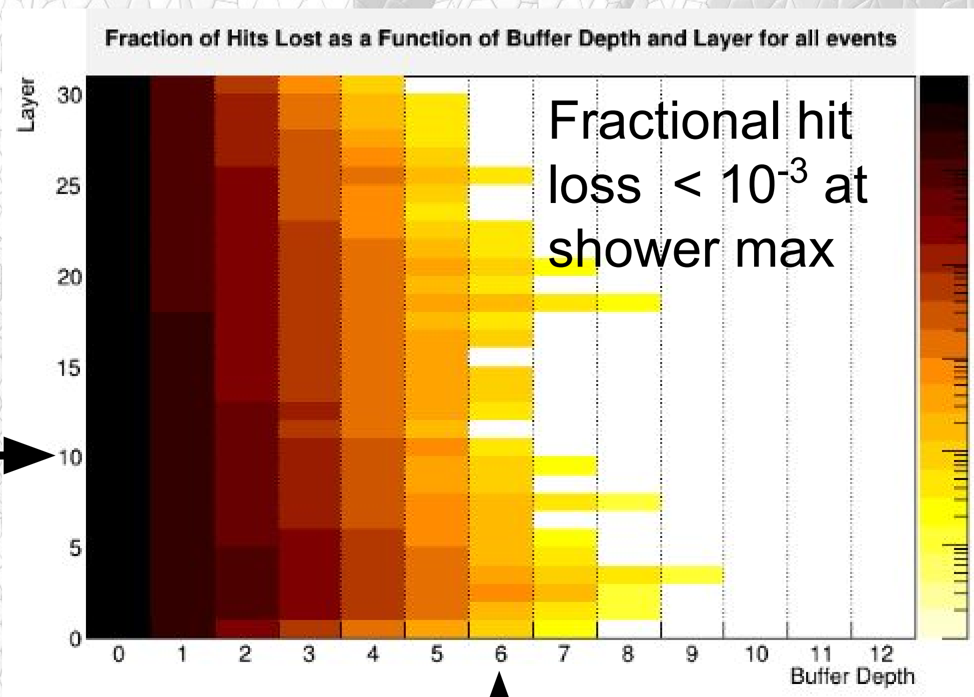


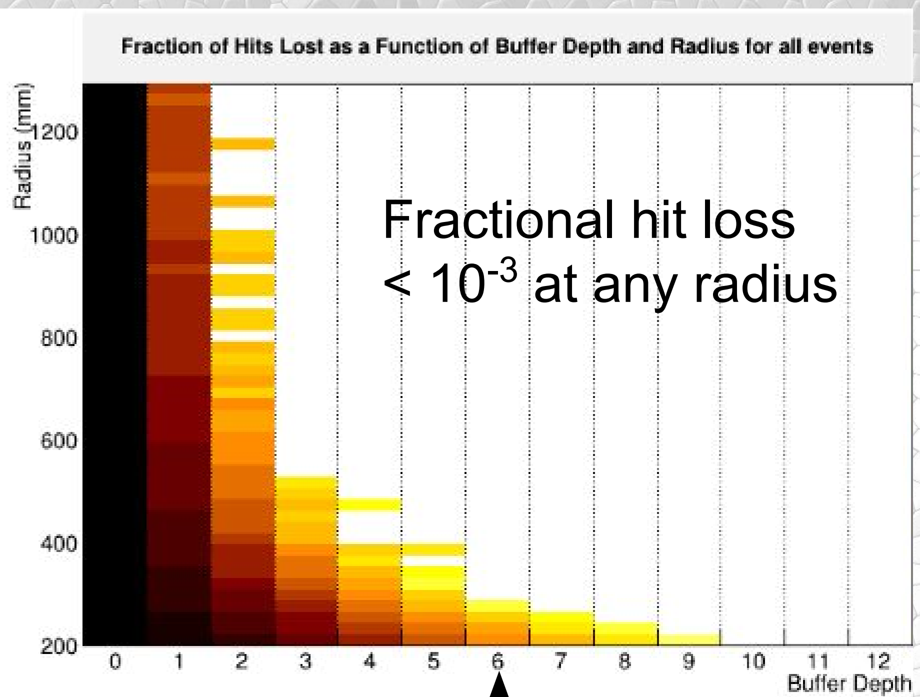
Work done at UCSC: B. Schumm, L. d'Hautuille

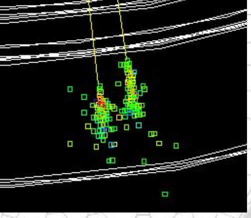


KPiX Buffer Multiplicity

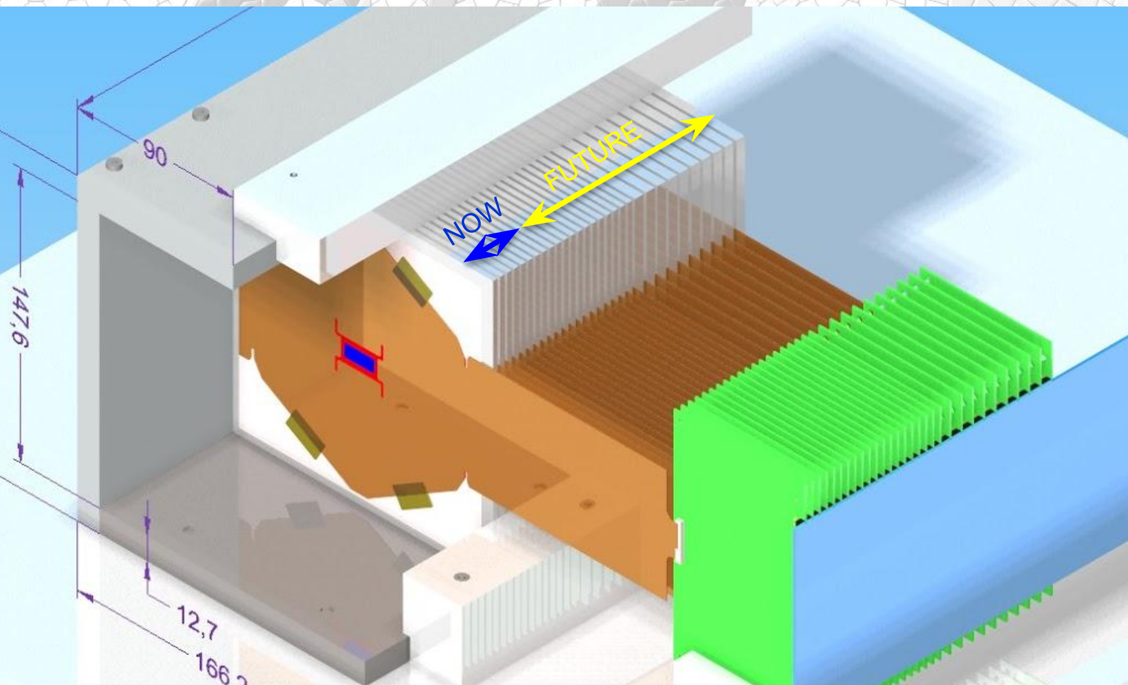
- 6 buffers also improve fractional hit loss within detector at shower max and radially
- Study KPiX to see if more buffers might be added, preserving architecture.
- Study somewhat different architecture – preconceptual ideas only…

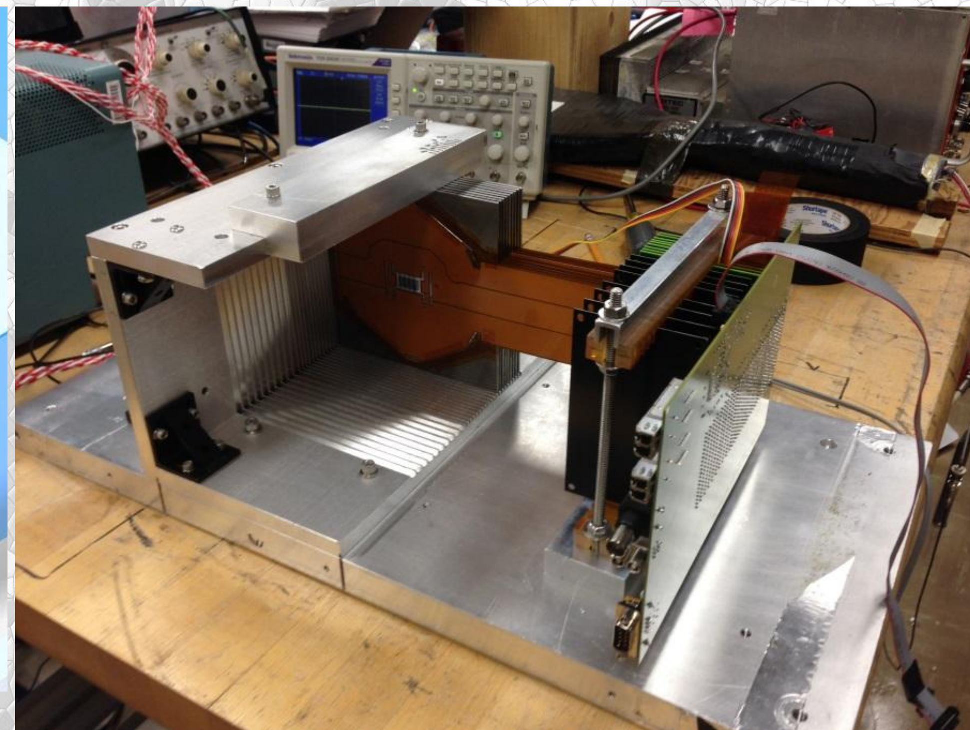




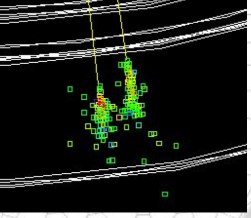


Initial test beam module for T-511 only 9 Si + 8 W layers (~ 6 X_0)

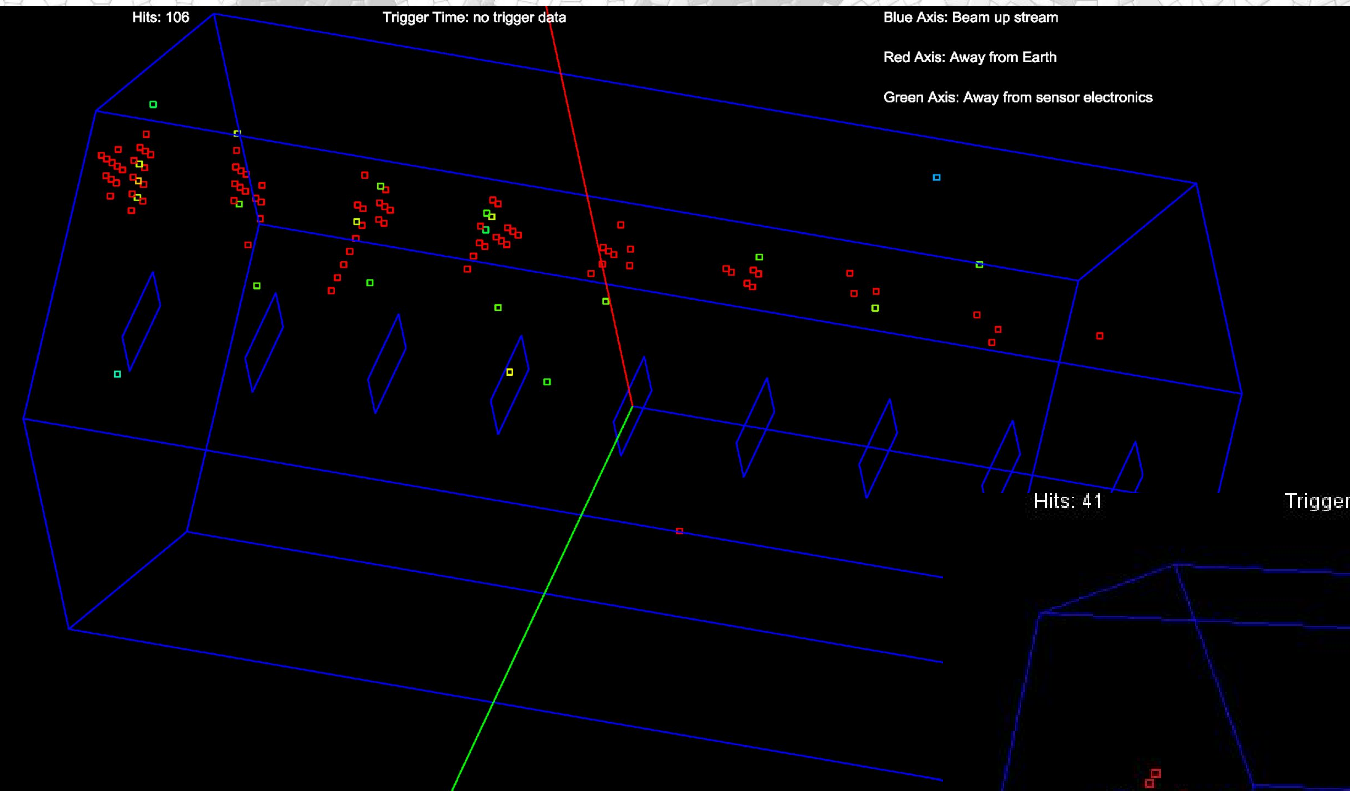


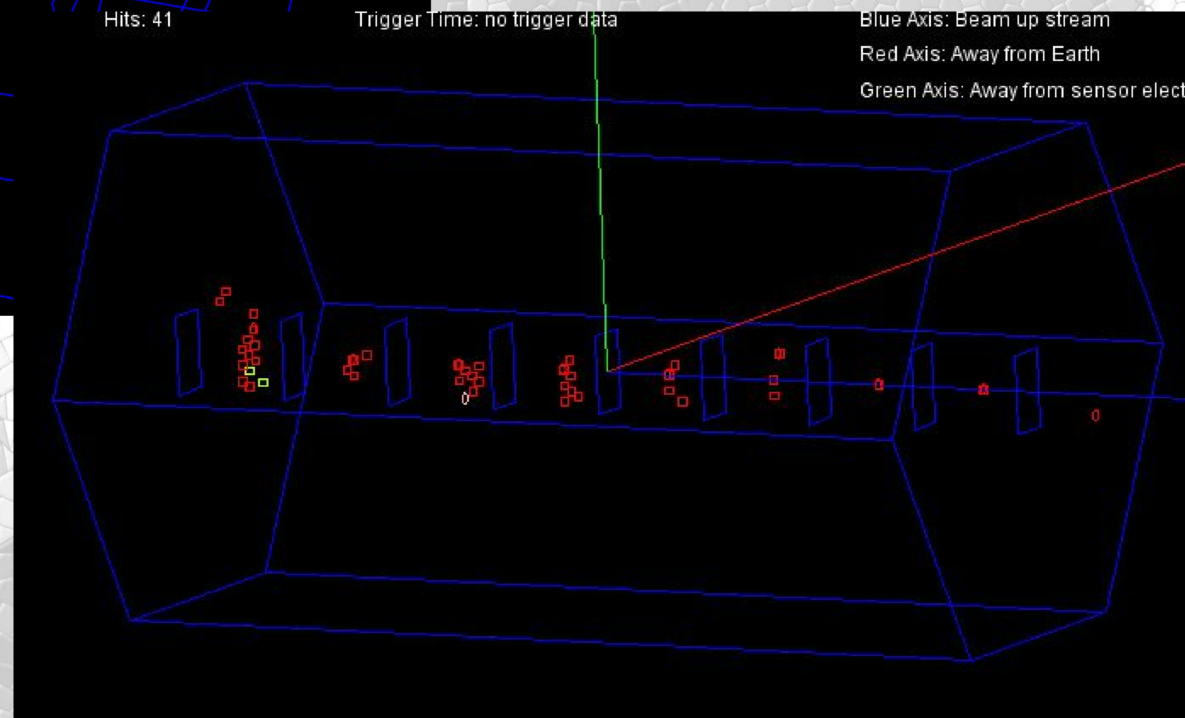


- First system test ECal sensors in SLAC End Station A beam at 12.1 GeV
- Utilized successfully bump bonded KPiX to sensor and sensor to cable
- Uncovered issues related to many pixels triggered simultaneously.

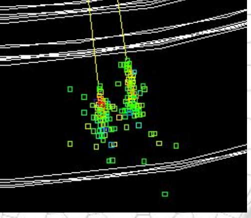


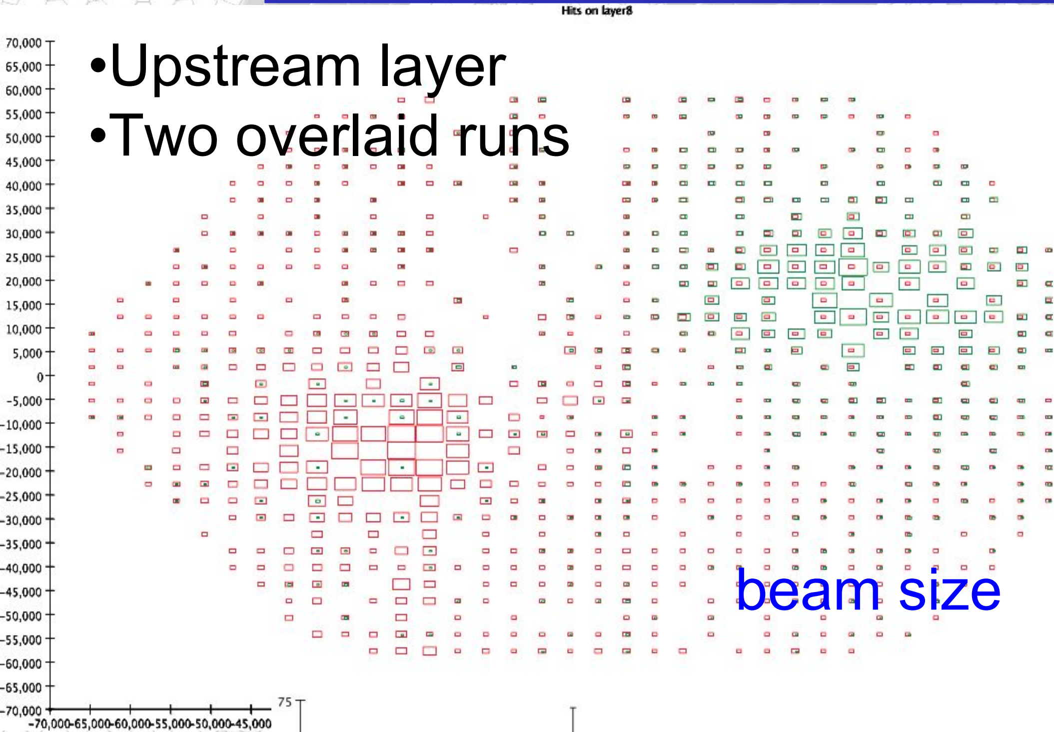
Single-Electron Showers



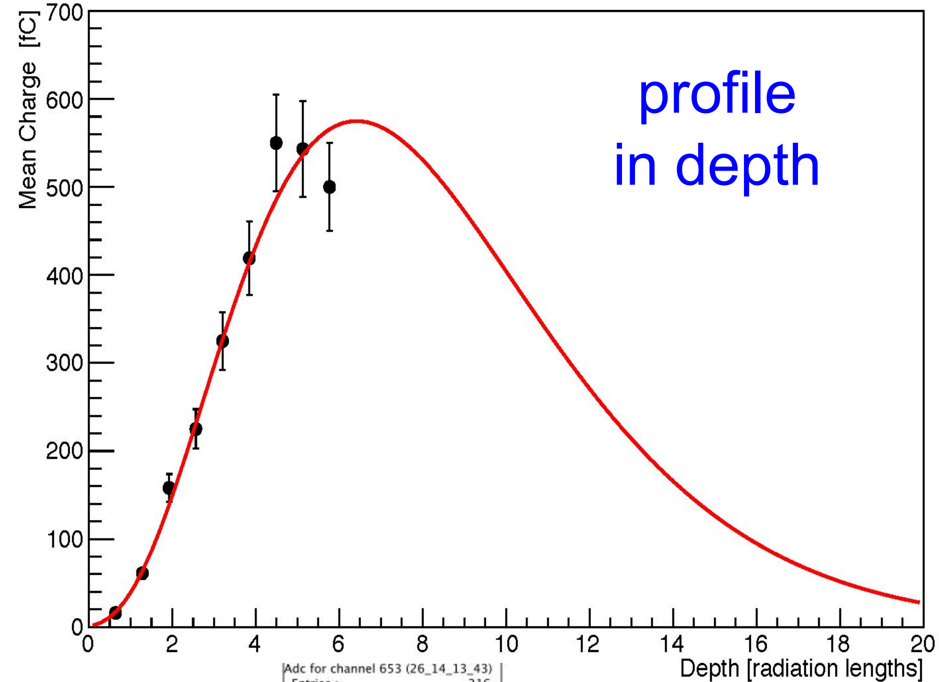


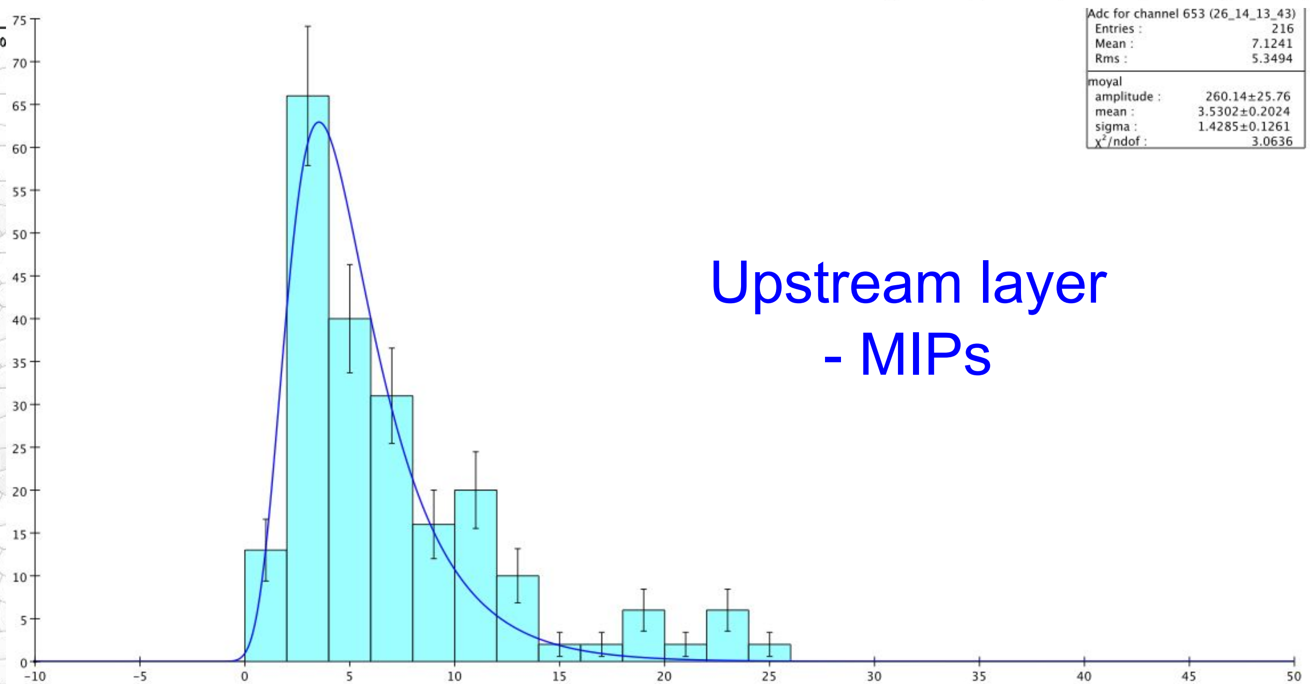
Test Beam Results

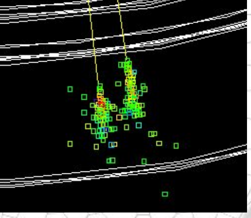




- Upstream layer
- Two overlaid runs

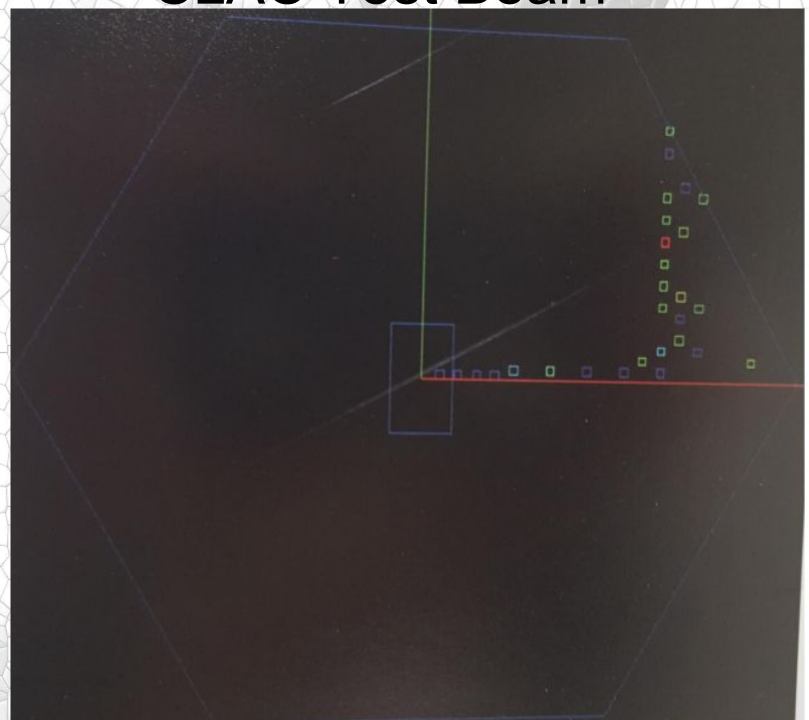




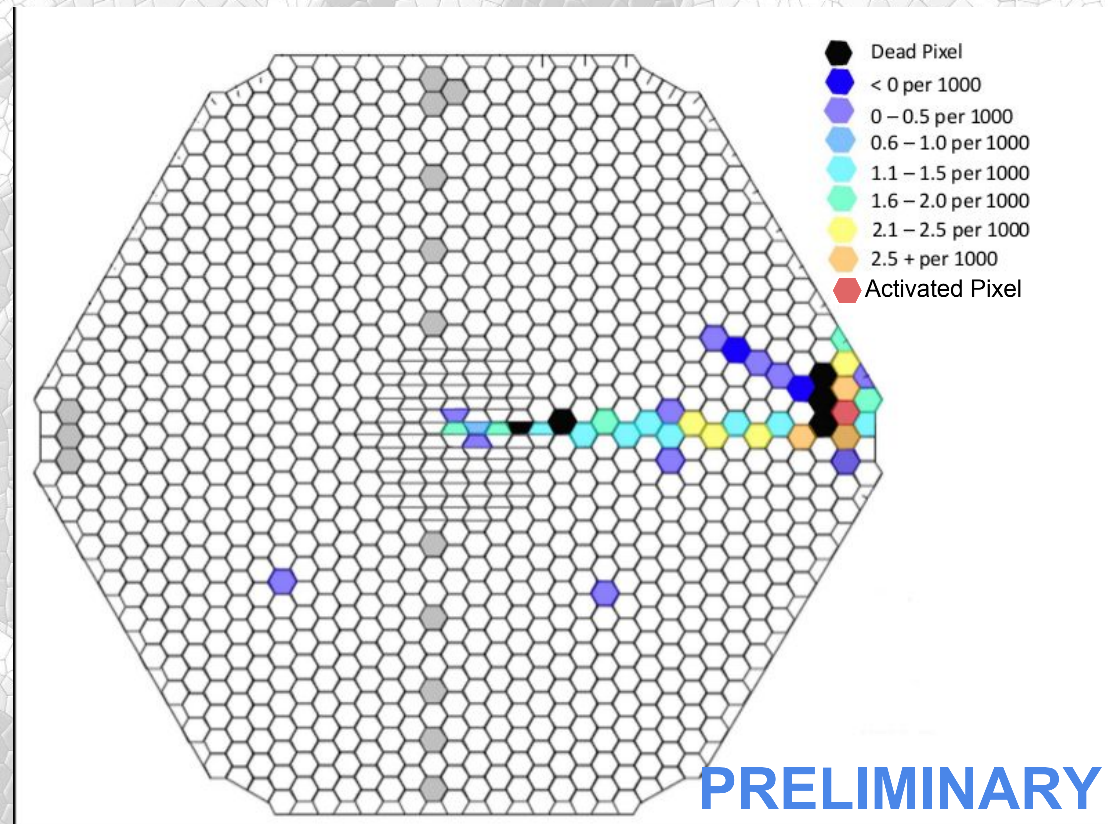


Cross-Talk on Test Beam Senor

SLAC Test Beam



Probe-Tested Sensor

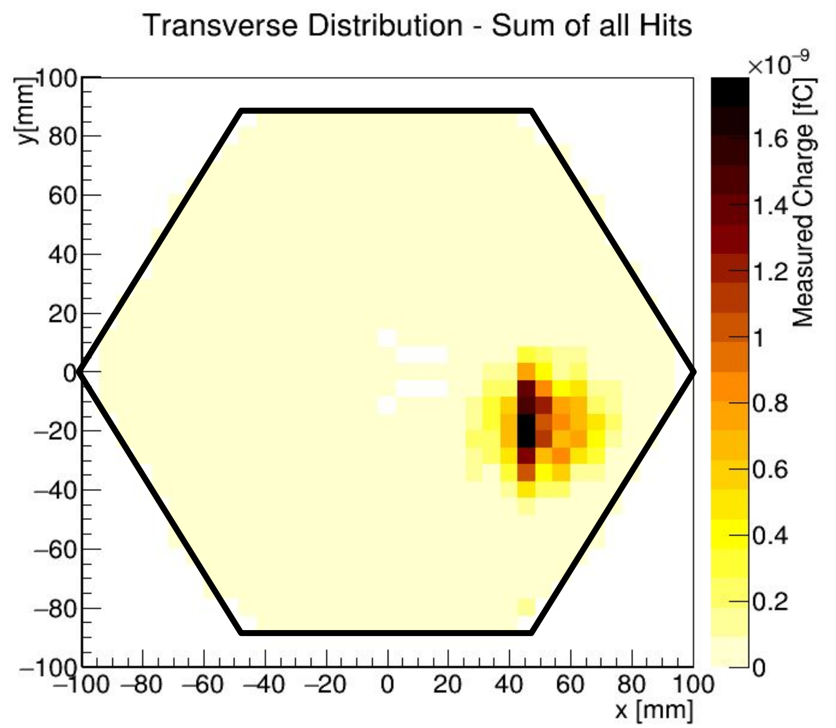


- Additional signal detected in pixels along trace of activated pixel (cross talk)
- Should be reduced with new shielded KPiX model

Work done at the University of Oregon:
C. Gallagher

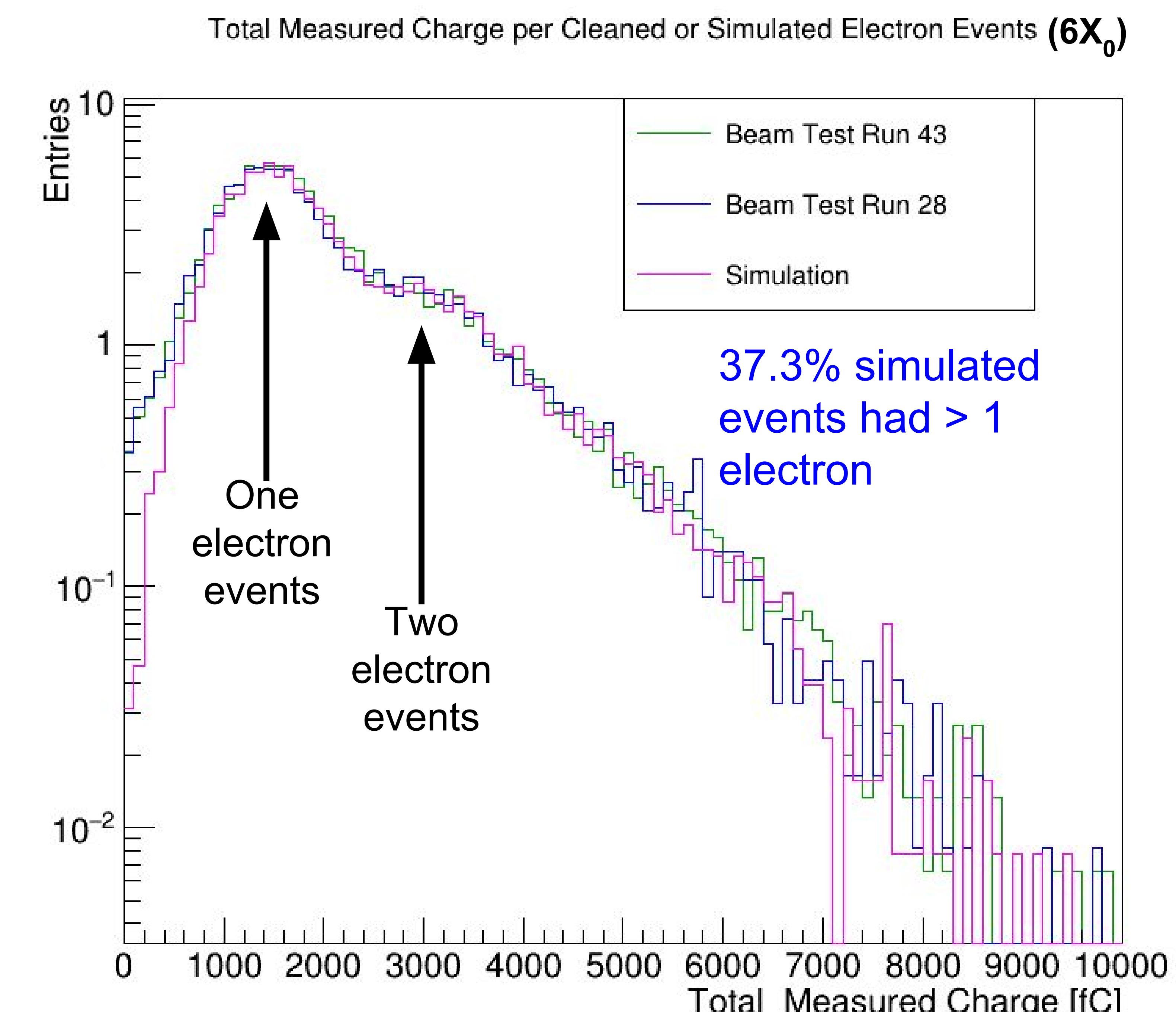
Simulation of Test Beam

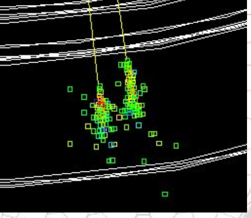
- Geant4 - generated electron showers through 9 simulated Si layers (6 X_0tungsten)
- Poisson distribution of events with 1, 2, 3, 4, or 5 simultaneous electrons
  - <n>=0.8725
- Random exclusion of “dead pixels”
- Normal distribution of events shifted from center



Work done at the University of Oregon: A. Steinhebel, J. Barkeloo, D. Mead

Simulation vs. Data

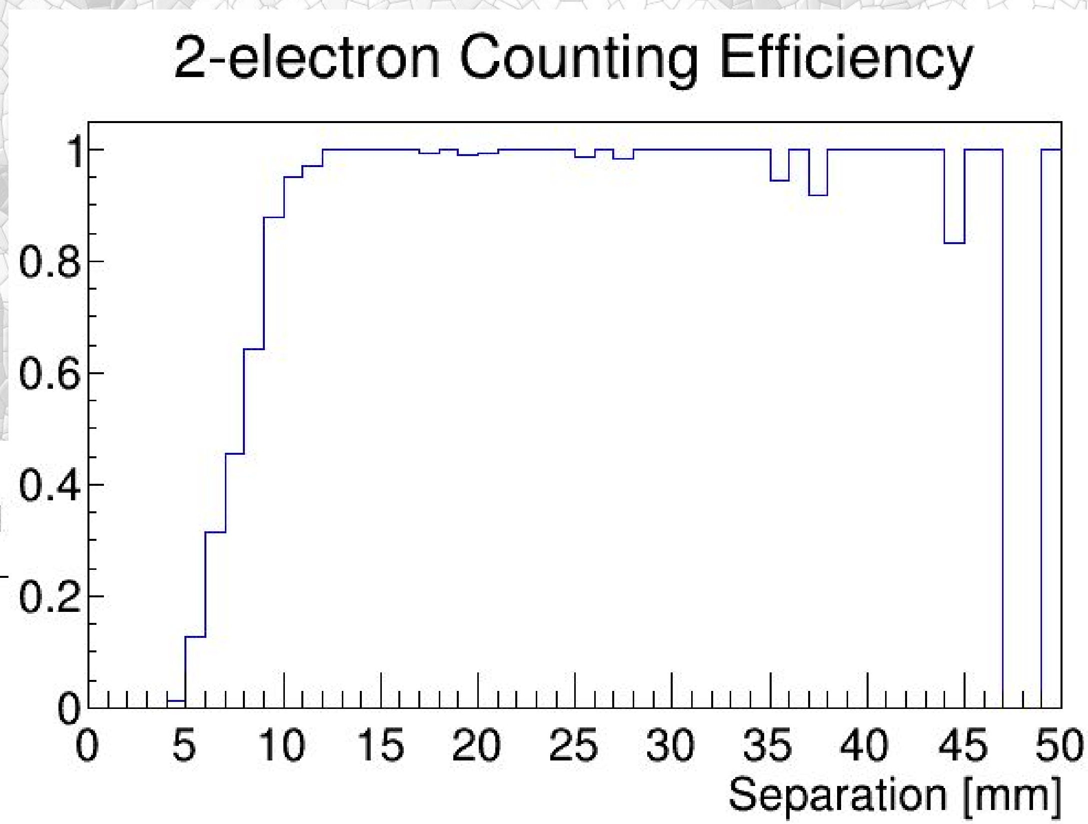


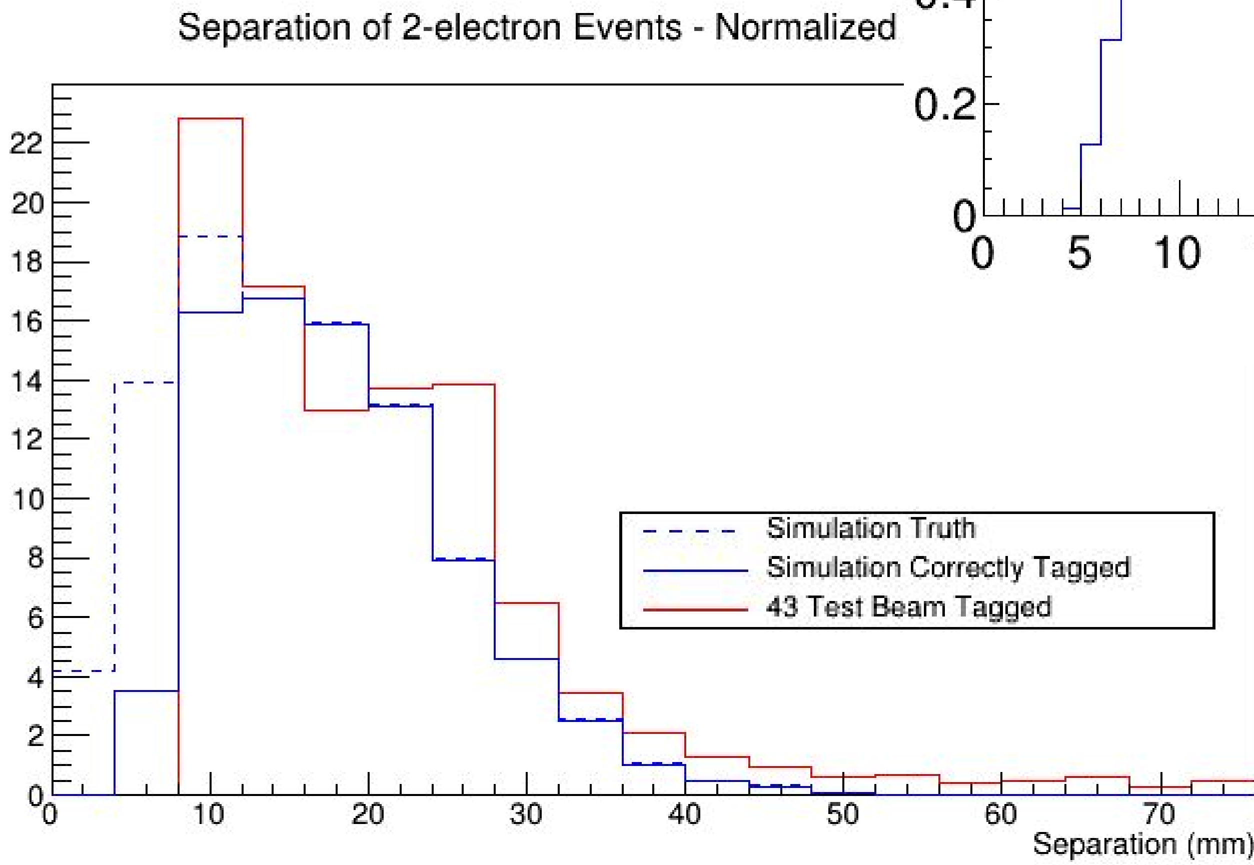


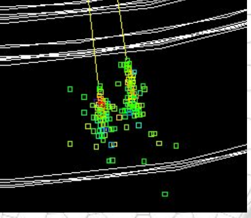
Correct Counting Efficiency

Simulated Two Electron Events

Correctly counted 2-electron events with 98.5% average efficiency when separated by >1 cm

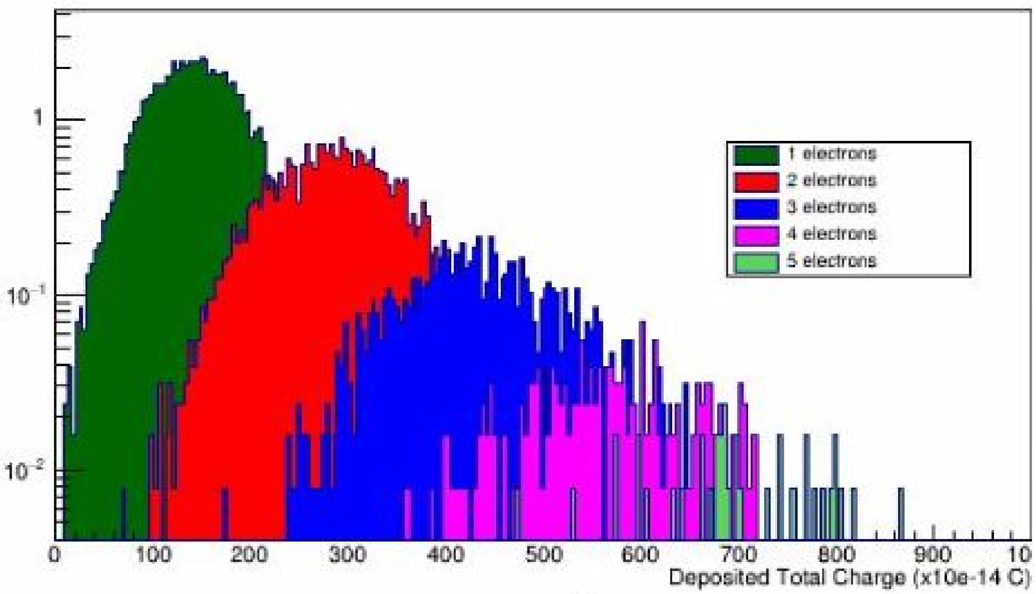




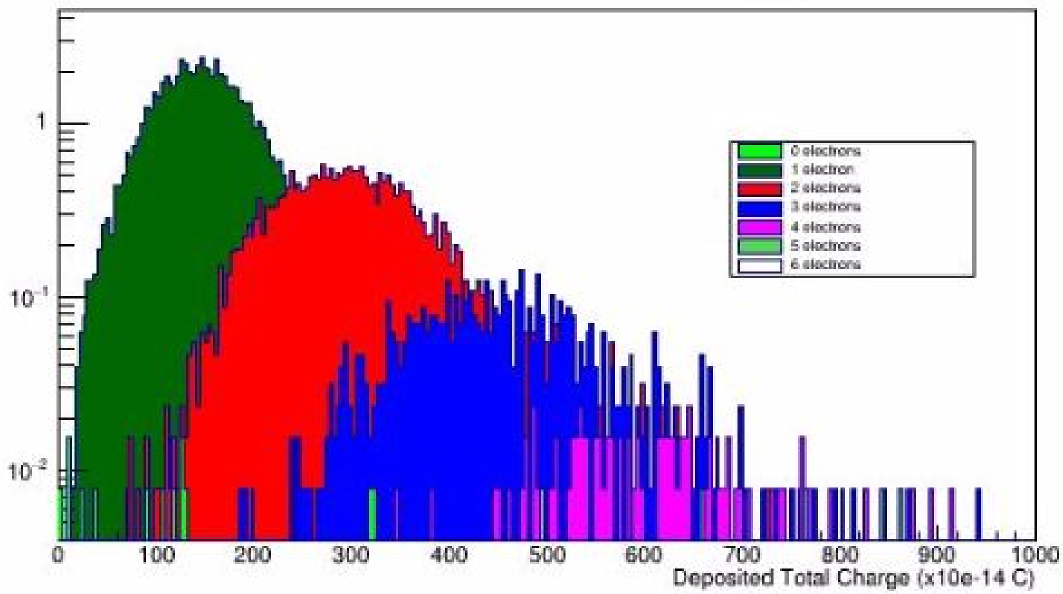


Counting Electrons

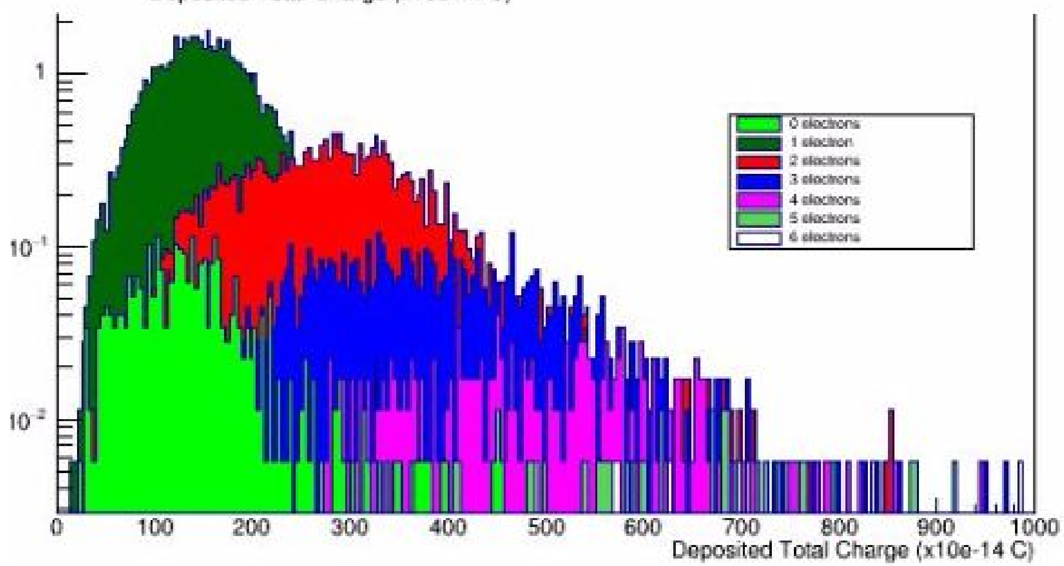
Electron Events -Simulation Truth



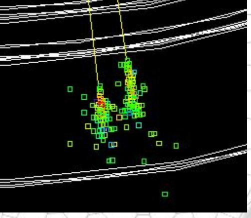
Electron Events -Simulation Tagged



Electron Events -
Test Beam Tagged

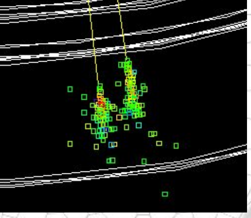


0 electrons
1 electron
2 electrons
3 electrons
4 electrons
5 electrons
6 electrons



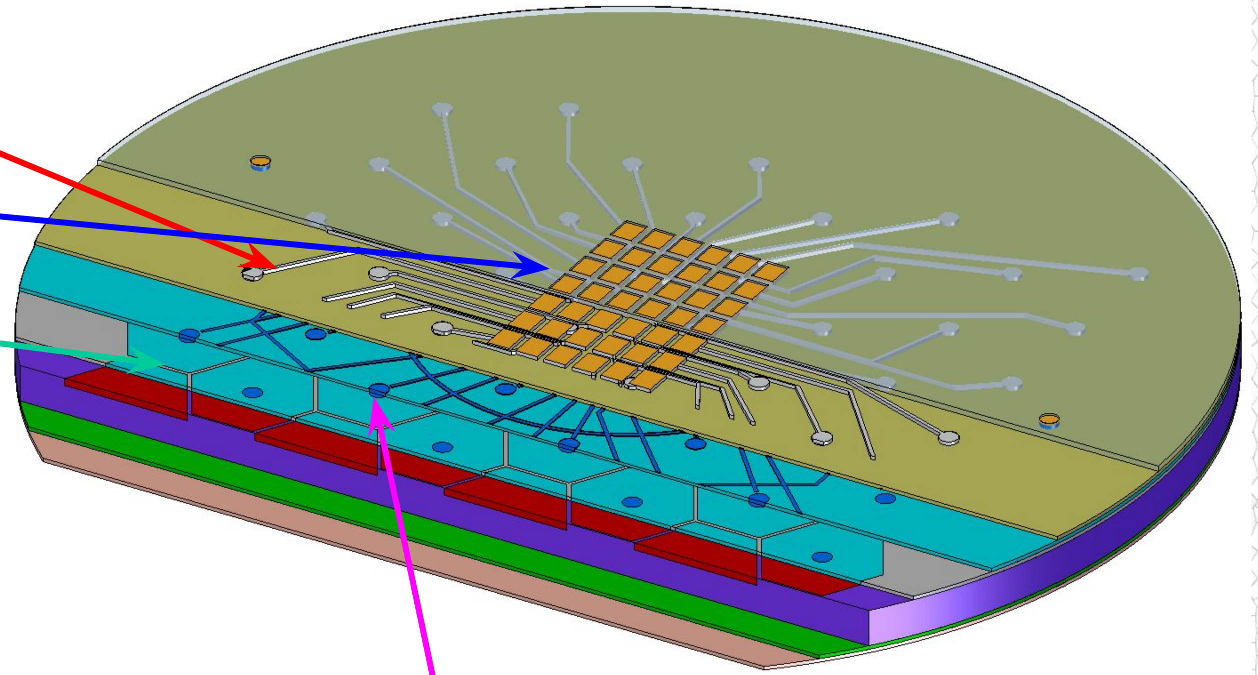
Major Lessons (so far)

- ECal can have huge number of pixels hit simultaneously, causing synchronous disturbances as pixels reset
    - Problem understood, small changes in design
- Bump bonding to sensors with Al pads can be very difficult…
    - Require sensor foundry build final pad stack.
    - Now have Under Bump Metallization with Au pads and shielding in second-generation ECal sensors
- Sensors with ROC’s can have issues with parasitic couplings…



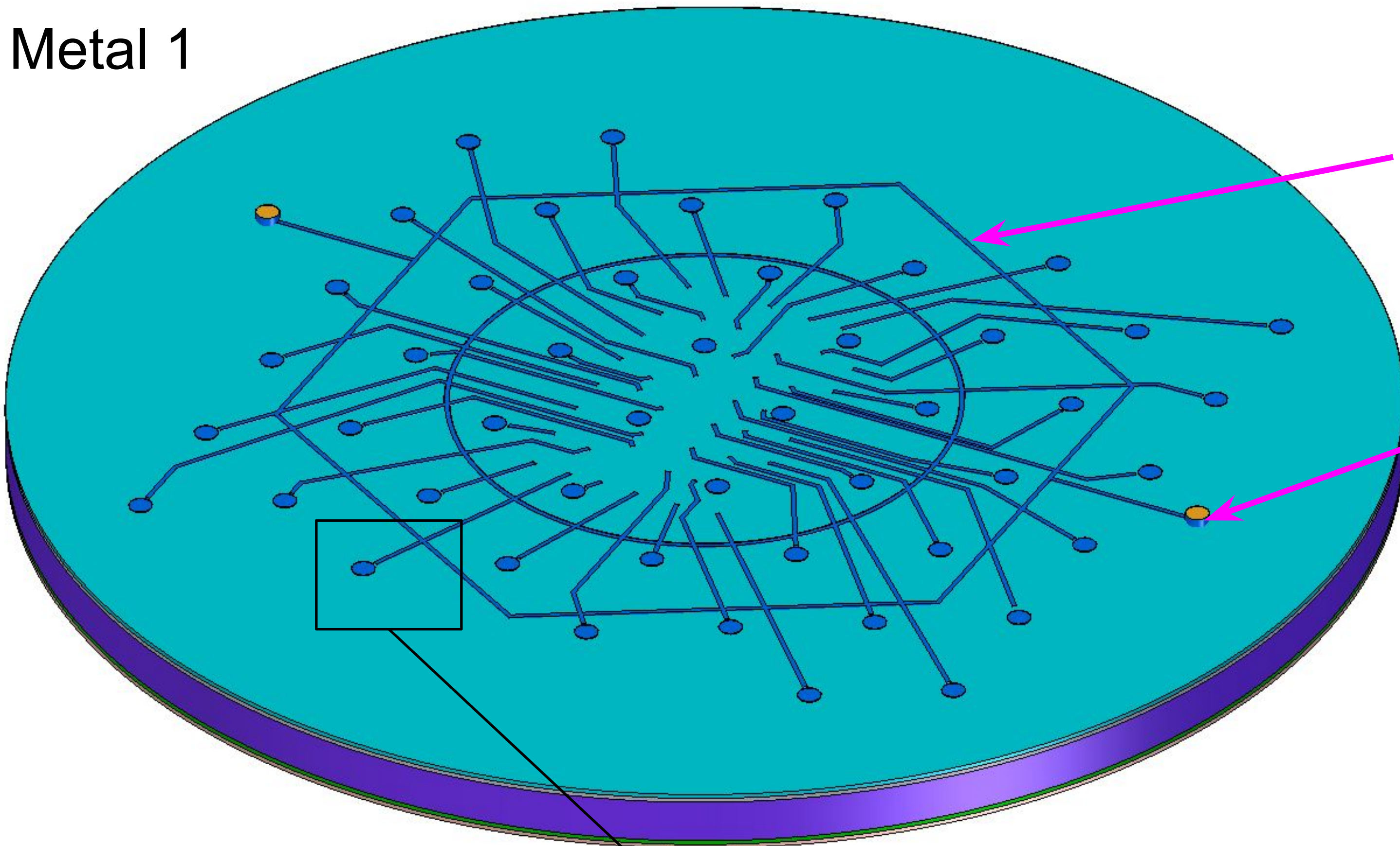
Sensor Traces

In present design, **metal 2 traces** from **pixels** to **pad array** run over other pixels: parasitic capacitances cause crosstalk.



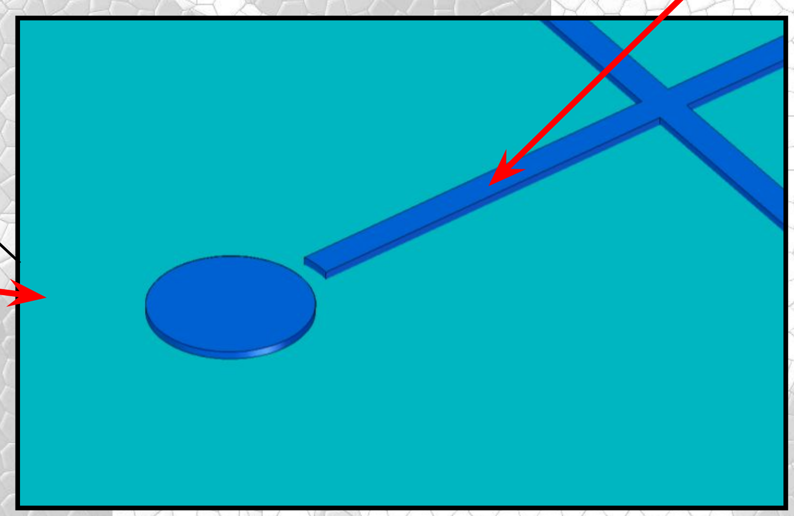
New scheme has “same” metal 2 traces, but a fixed potential metal 1 trace shields the signal traces from the pixels.

Metal 1



All shield traces are tied together, and brought to a metal 2 pad.

Shield trace running under Metal 2 signal trace.

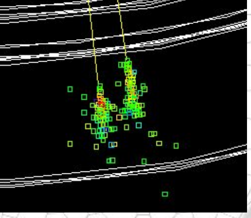


connection of implant to metal 2 trace to pad.

New Hamamatsu Sensors

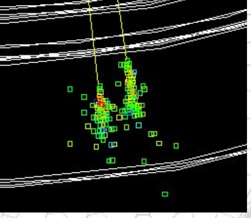
- The **original** Hamamatsu sensors have Aluminum pads, which are extremely difficult (and expensive) to bump bond.
  - Hamamatsu has provided suitable Under Bump Metallization instead.

- We have **new** set of sensors with gold pads, UBM, and the new shield structure
  - Awaiting rigorous testing



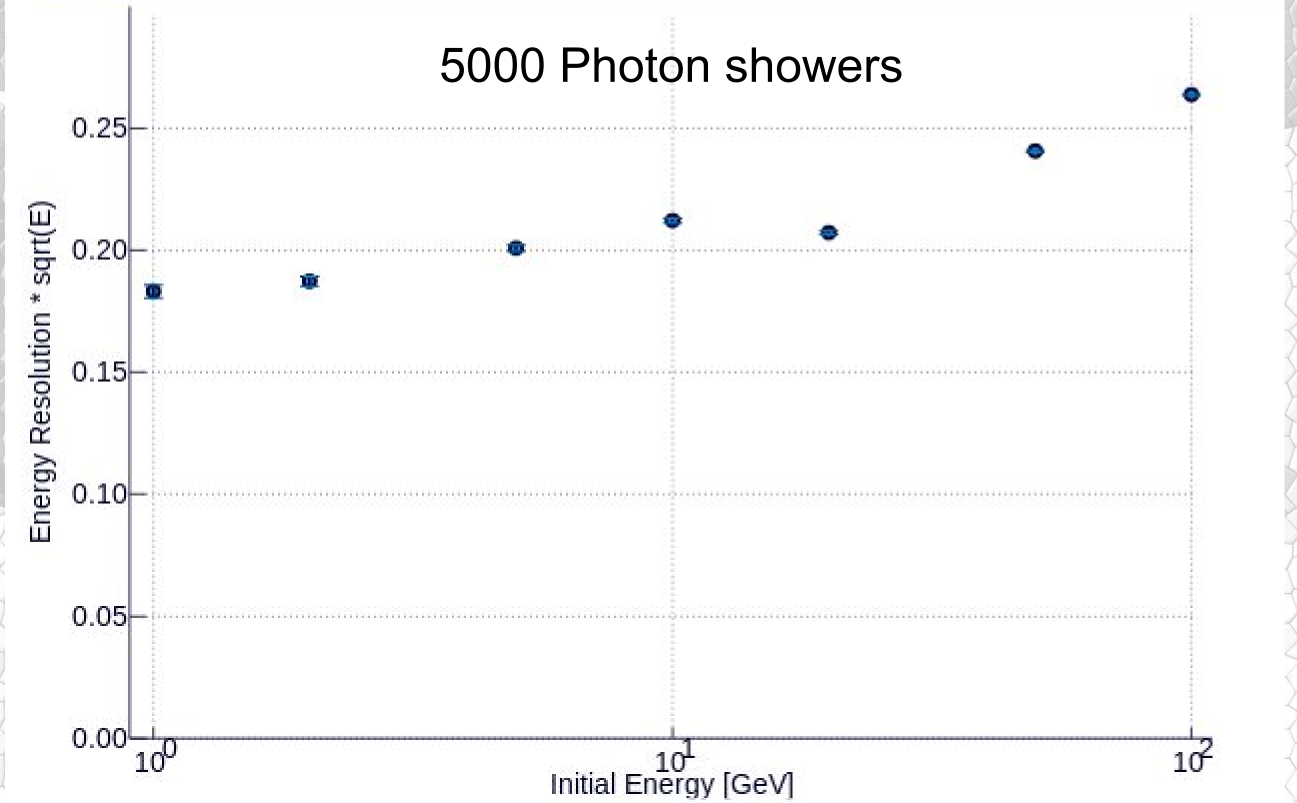
Monolithic Active Pixels

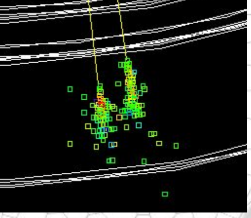
- An alternative sensor structure will be studied for the SiD EMCal with the sensor built from HV-CMOS, which would completely eliminate the bump bonding problem.
    - A. Dragone, 29/06 9am Kalvi Auditorium bldg. 51
- This approach would solve the multiplicity concern about KPiX by having more buffers, and eliminate the range switching by using smaller pixels than possible with KPiX.
- A pre-conceptual design has been developed. This approach would also be useful for the SiD tracker.



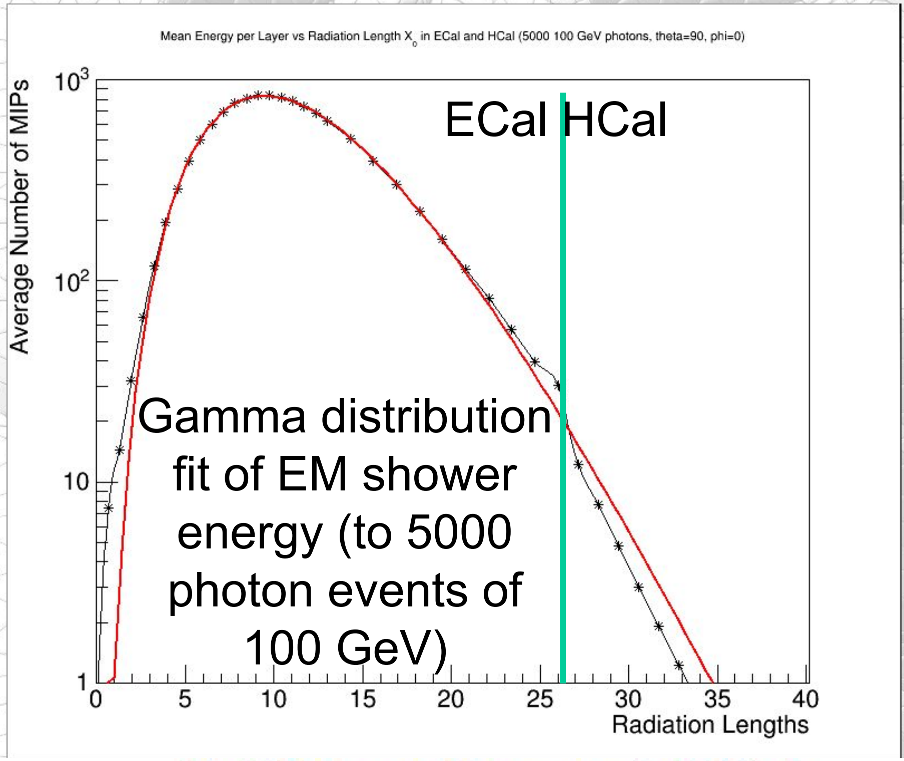
SiD Detector Simulation

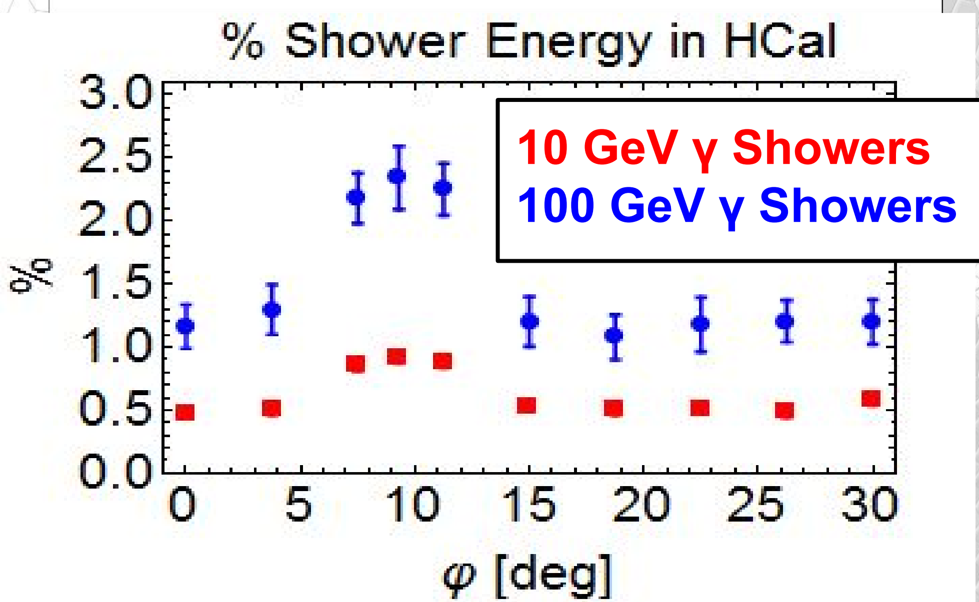
- SiD_o2_v02
  - Active work toward SiD_o3_v01
- Full DD4HEP integration
- Standard Digitization and Reconstruction processors
  - RealisticCaloDigiSilicon, RealisticCaloRecoSilicon
- Features realistic subdetector geometry (including overlapping ECal modules)





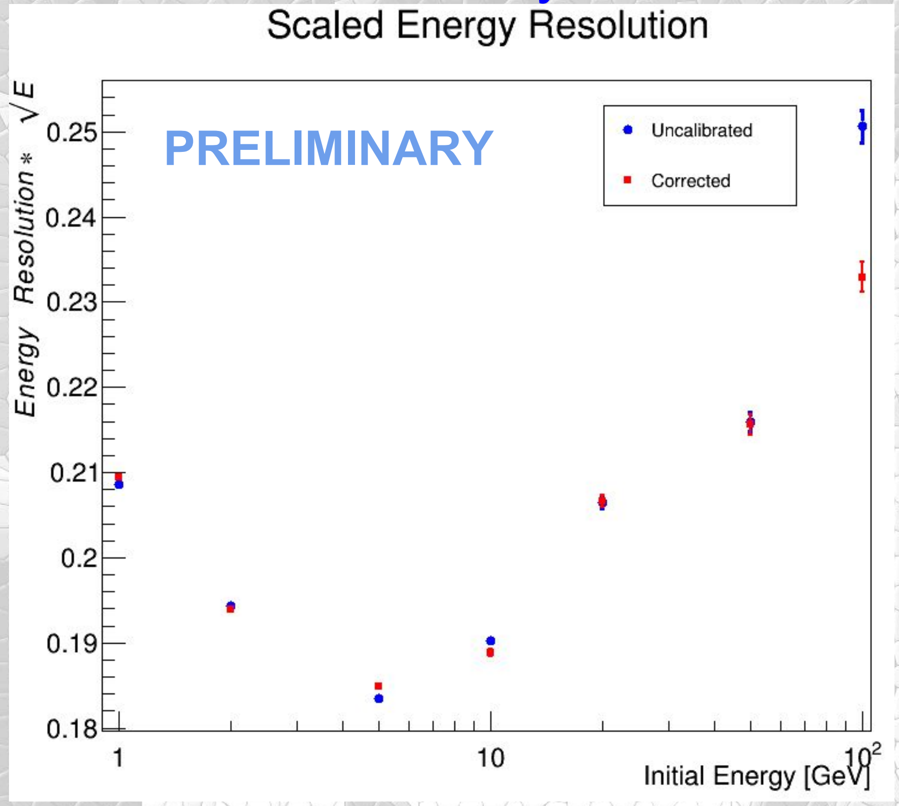
ECal Leakage to Inform Calibration

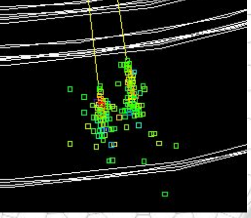




- Fit shower of each event to predict HCal leakage
    - ~ 1% of shower for 100 GeV γ
- Correct for leakage on event - by - event basis
- Ongoing work

More information: Friday SiD Session





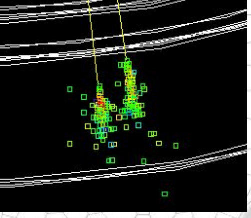
Ongoing / Future Studies

- KPiX cross talk
- Large area MAPs
- Second iteration of test beam with second generation sensors
- Thorough ECal/HCal detector calibration within simulation
- Physics effect of decreasing calorimeter depth or number of active layers
- Shower separation for particle flow applications
- Edge wafer configuration

Resources limited (human and financial)

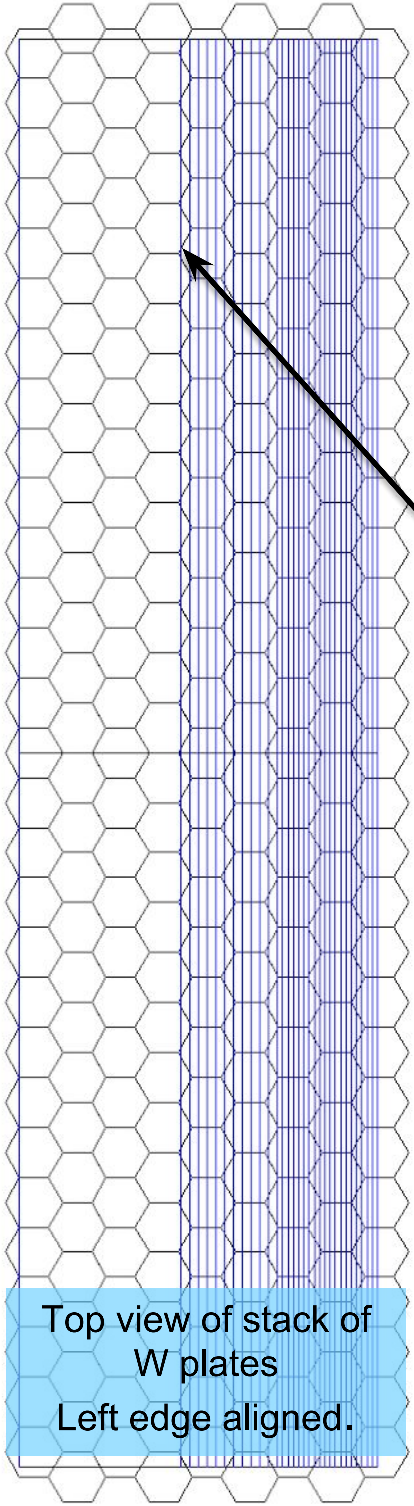
Summary

- There is slow progress towards a mechanical conceptual design of the ECal
- There is a shielding concept for the next sensor generation.
- Monolithic Active Pixels are being studied for both the ECal and the Tracker.
- Effects of overlapping module geometry has been studied and largely understood



EXTRAS

Tiling Issues

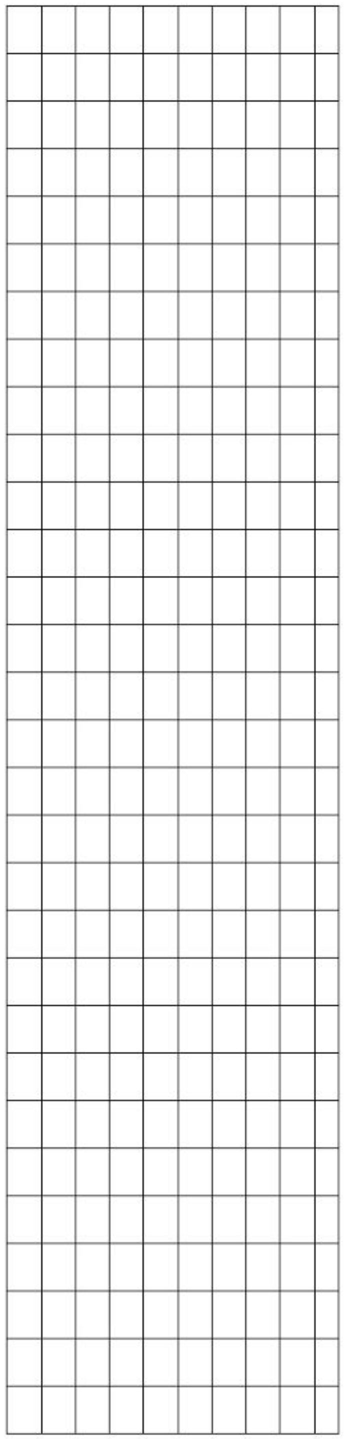


Range of widths of plates makes tiling challenging!

Pre-conceptual design:

Worry about tiling later!

(Hexagons make efficient use of the wafer though…)



Next iteration:

Efficient tiling is possible with two different sized rectangles.

Penalty is ~30% more wafers.

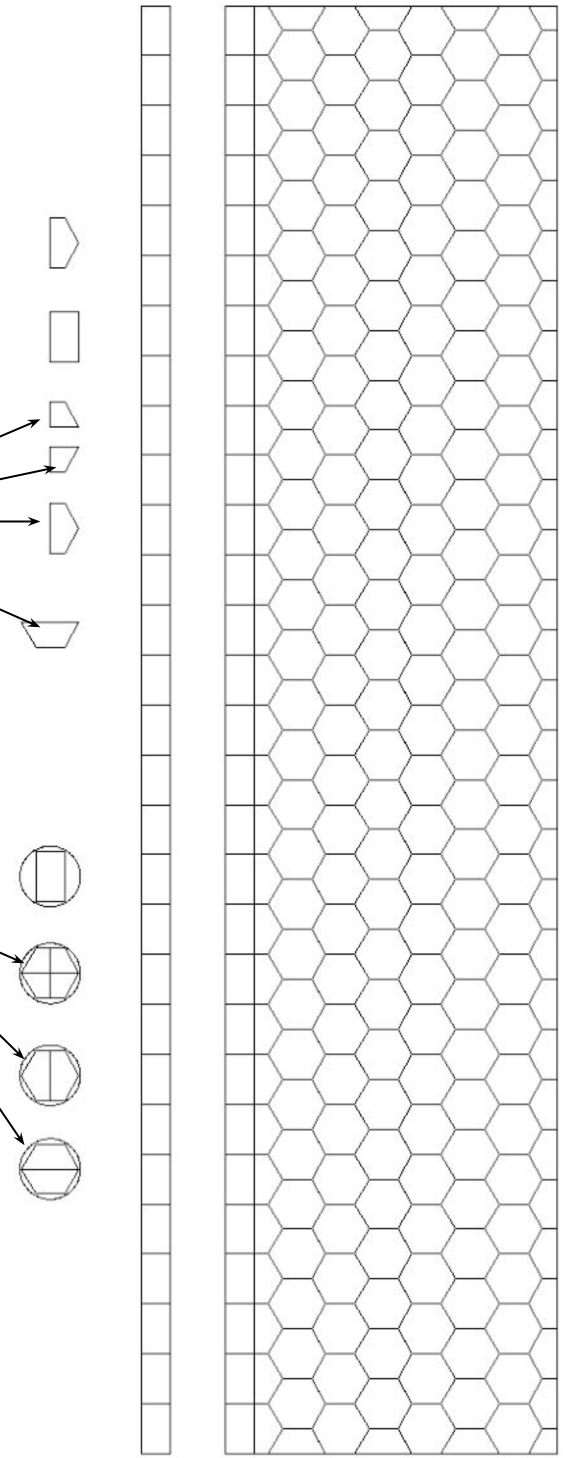
Tiling Issues

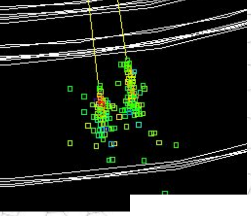
Beginning study of hybrid tiling:

Hexagons for the field, with standard elements to fill the hexagon tiling to a large rectangle.

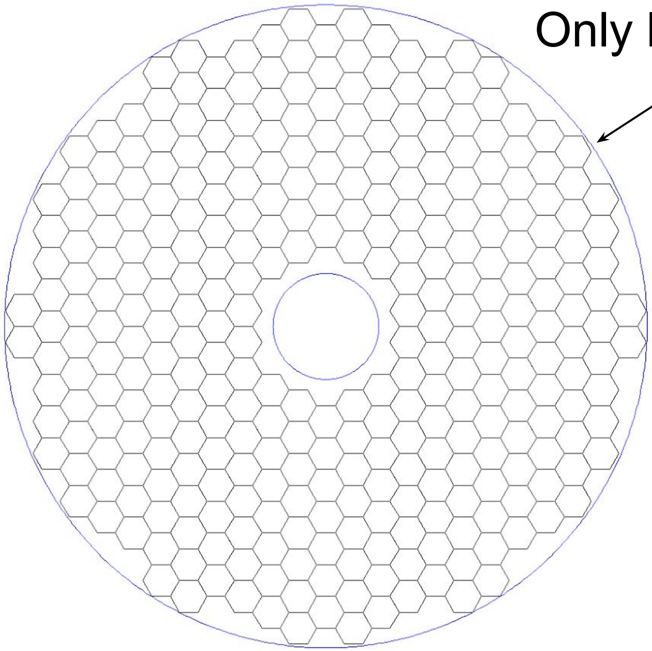
These elements efficiently fill a wafer.

Then fill to layer edge with rectangles.

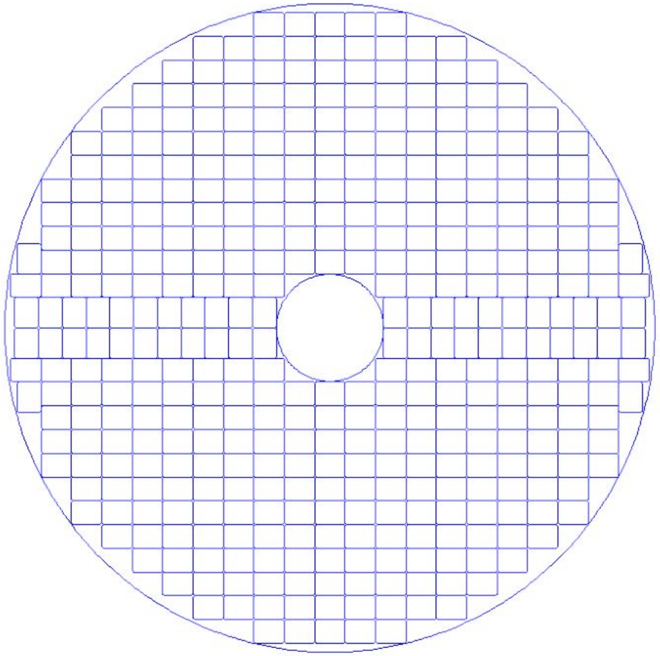




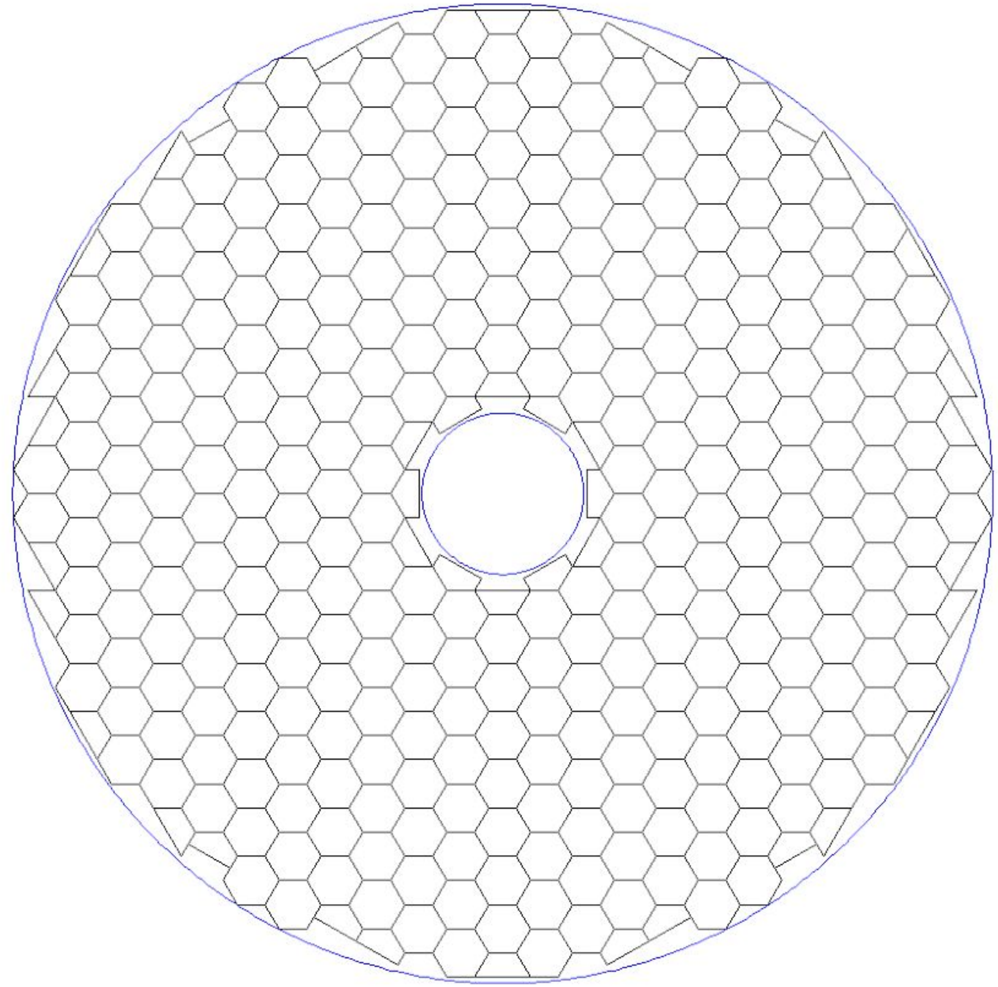
Endcap Tiling – first tries



Only hexagons



"Barrel" rectangles



Hexagons + Barrel hybrid elements