JAMMA_CONN

JM1

GND	1	A	GND
VSSA	2	B	VSS
VDDA	3	C	VCC
+5V	4	D	+5V
−5V	5	E	−5V
+12V	6	F	+12V
COIN_CNT_1	7	H	
	8	J	COIN_CNT_2
NC	9	K	NC
SPEAKER_(+)	10	L	SPEAKER_(−)
NC	11	M	NC
RED	12	N	GREEN
BLUE	13	P	SYNC
VIDEO_GND	14	R	SERVICE
NC	15	S	NC
COIN_1	16	T	COIN_2
1P_START	17	U	2P_START
1P_UP	18	V	2P_UP
1P_DOWN	19	W	2P_DOWN
1P_LEFT	20	X	2P_LEFT
1P_RIGHT	21	Y	2P_RIGHT
1P_BTN_1	22	Z	2P_BTN_1
1P_BTN_2	23	a	2P_BTN_2
1P_BTN_3	24	b	2P_BTN_3
1P_BTN_4	25	c	2P_BTN_4
1P_SELECT	26	d	2P_SELECT
	27	e	
GND	28	f	GND

PWR_FLAG VCC GND
PWR_FLAG
VCC
VSS
+12V
PWR_FLAG +5V
PWR_FLAG VSS

VSS

3P — CN6 Conn_01x15

1	COIN_3
2	3P_LEFT
3	
4	3P_RIGHT
5	3P_UP
6	3P_DOWN
7	3P_BTN_1
8	3P_BTN_2
9	3P_BTN_3
10	3P_START
11	3P_SERV
12	
13	
14	
15	

4P — CN7 Conn_01x15

1	COIN_4
2	4P_LEFT
3	
4	4P_RIGHT
5	4P_UP
6	4P_DOWN
7	4P_BTN_1
8	4P_BTN_2
9	4P_BTN_3
10	4P_START
11	4P_SERV
12	
13	
14	
15	VSS

NOT MOUNTED

VCC
RA22 4kX8 RA18 4kX8 RA17 4kX8 RA16 4kX8
YOBJROMD0 ... YOBJROMD31
YOBJROMD[31..0]

VCC
RA23 4kX8 RA21 4kX8 RA20 4kX8 RA19 4kX8
XOBJROMD0 ... XOBJROMD31
XOBJROMD[31..0]

OBJROMA[19..0]
VCC
CN1 Conn_02x32_Row_Letter_First
OBJROMA0 ... OBJROMA19
XOBJROMD0 ... XOBJROMD31
VSS

sound
PCM[2..0] → PCM[2..0]
SWAIT → SWAIT
SINT → SINT
SRST → SRST
BUSY → BUSY
SNDPAL5 → SNDPAL5
SNDPAL8 → SNDPAL8
SND_D[7..0] → SND_D[7..0]
SND_A[15..0] → SND_A[15..0]
SIC_CLK → SIC_CLK
SRD → SRD
SWR → SWR
SIORQ → SIORQ
SCLK → SCLK
MCLK → MCLK
Archivo: sound.kicad_sch

pcm
+12V → +12V
MYUT → MYUT
SND_A[15..0] → SND_A[1..0]
SNDPAL8 → SNDPAL8
SNDPAL5 → SNDPAL5
MAIN_A[23..0] → MAIN_A[4..0]
SDON → SDON
SRD → SRD
R/W → M_R/W
SWR → SWR
SIC_CLK → SIC_CLK
SIORQ → SIORQ
PAIRCS → PAIRCS
BUSY → BUSY
SCLK → SCLK
SND_D[7..0] → SND_D[7..0]
MAIN_D[7..0] → MAIN_D[15..0]
SPEAKER(+) → SPEAKER(+)
SPEAKER(−) → SPEAKER(−)
PCM[2..0] → PCM[2..0]
SWAIT → SWAIT
SRST → SRST
SINT → SINT
Archivo: pcm.kicad_sch

io_cabinet
IOCCS1 → IOCCS1
R/W → M_R/W
RESET → RESET
IOCCS2 → IOCCS2
MRD → MRD
UDS → UDS
PAS → PAS
MAIN_A[23..1] → MAIN_A[6..1]
1P_BTN_3 → 1P_BTN_3
2P_BTN_3 → 2P_BTN_3
2P_LEFT → 2P_LEFT
1P_DOWN → 1P_DOWN
1P_LEFT → 1P_LEFT
2P_DOWN → 2P_DOWN
1P_RIGHT → 1P_RIGHT
1P_BTN_2 → 1P_BTN_2
1P_BTN_1 → 1P_BTN_1
2P_RIGHT → 2P_RIGHT
2P_BTN_1 → 2P_BTN_1
2P_BTN_2 → 2P_BTN_2
TEST → TEST
2P_UP → 2P_UP
2P_START → 2P_START
1P_START → 1P_START
1P_UP → 1P_UP
COIN_1 → COIN_1
COIN_2 → COIN_2
SERVICE1 → SERVICE1
SERVICE2 → SERVICE2
3P_SERV → 3P_SERV
4P_SERV → 4P_SERV
3P_START → 3P_START
4P_START → 4P_START
3P_LEFT → 3P_LEFT
4P_LEFT → 4P_LEFT
3P_RIGHT → 3P_RIGHT
4P_RIGHT → 4P_RIGHT
3P_UP → 3P_UP
4P_UP → 4P_UP
3P_DOWN → 3P_DOWN
4P_DOWN → 4P_DOWN
COIN_3 → COIN_3
COIN_4 → COIN_4
3P_BTN_3 → 3P_BTN_3
4P_BTN_3 → 4P_BTN_3
3P_BTN_1 → 3P_BTN_1
4P_BTN_1 → 4P_BTN_1
3P_BTN_2 → 3P_BTN_2
4P_BTN_2 → 4P_BTN_2
COIN_CNT_1 → COIN_CNT_1
COIN_CNT_2 → COIN_CNT_2
MAIN_D[15..0] → MAIN_D[15..0]
VCHARA → VCHARA
OCHARA → OCHARA
SDON → SDON
INTDMAEN → INTDMAEN
MYUT → MYUT
OBJREG → OBJREG
PAIRCS → PAIRCS
PCUCS → PCUCS
CRCS → CRCS
+12V → +12V
SYSRES → SYSRES
SCRCLK → SCRCLK
Archivo: io_cabinet.kicad_sch

objects
OBJCS → OBJCS
UDS → UDS
LDS → LDS
HSYNC → HSYNC
VSYNC → VSYNC
ORAMWEH → ORAMWEH
ORAMWEL → ORAMWEL
RESET → RESET
OBJCLK6 → OBJCLK6
OCHARA → OCHARA
OBJREG → OBJREG
MAIN_A[23..0] → MAIN_A[13..1]
MRD → MRD
CRCS → CRCS
OBJCLK12 → OBJCLK12
MAIN_D[15..0] → MAIN_D[15..0]
OCOL[8..0] → OCOL[8..0]
PRI[4..0] → PRI[4..0]
OBJROMA[19..0] → OBJROMA[19..0]
XOBJROMD[31..0] → XOBJROMD[31..0]
YOBJROMD[31..0] → YOBJROMD[31..0]
OBJDMA → OBJDMA
SHD[1..0] → SHD[1..0]
Archivo: objects.kicad_sch

main
RESET → RESET
MAINIRQ → MAINIRQ
MCLK → MCLK
OBJDMA → OBJDMA
SCR_PQ → SCR_PQ
INTDMAEN → INTDMAEN
MCOWRL → MCOWRL
MCOWRH → MCOWRH
VCS → VCS
PAS → PAS
IOCCS1 → IOCCS1
IOCCS2 → IOCCS2
UDS → UDS
LDS → LDS
MRD → MRD
OBJCS → OBJCS
R/W → R/W
MAIN_A[23..0] → MAIN_A[23..0]
MAIN_D[15..0] → MAIN_D[15..0]
CRAMCS → CRAMCS
ORAMWEH → ORAMWEH
ORAMWEL → ORAMWEL
Archivo: main.kicad_sch

scroll
MAIN_A[23..0] → MAIN_A[16..1]
MRD → MRD
VCS → VCS
OBJCLK12 → OBJCLK12
OBJCLK6 → OBJCLK6
BCOL[3..0] → BCOL[3..0]
BPAL[4..0] → BPAL[4..0]
FCOL[3..0] → FCOL[3..0]
MAIN_D[7..0] → MAIN_D[15..0]
APAL[4..0] → APAL[4..0]
ACOL[3..0] → ACOL[3..0]
VCHARA → VCHARA
SCRCLK → SCRCLK
SYSRES → SYSRES
MAINIRQ → MAINIRQ
FPAL[3..0] → FPAL[3..0]
RESET → RESET
HBLANK → HBLANK
HSYNC → HSYNC
VSYNC → VSYNC
VBLANK → VBLANK
SCR_PQ → SCR_PQ
SYNC → SYNC
Archivo: scroll.kicad_sch

capacitors
Archivo: capacitors.kicad_sch

description
Archivo: description.kicad_sch

colmix
OBJCLK6 → OBJCLK6
SHD[1..0] → SHD[1..0]
FCOL[3..0] → FCOL[3..0]
FPAL[3..0] → FPAL[3..0]
BPAL[4..0] → BPAL[4..0]
BCOL[3..0] → BCOL[3..0]
PRI[4..0] → PRI[4..0]
APAL[4..0] → APAL[4..0]
ACOL[3..0] → ACOL[3..0]
OCOL[8..0] → OCOL[8..0]
MAIN_A[23..0] → MAIN_A[11..0]
MAIN_D[15..0] → MAIN_D[15..0]
MRD → MRD
PCUCS → PCUCS
MCOWRL → MCOWRL
MCOWRH → MCOWRH
HBLANK → HBLANK
VBLANK → VBLANK
RESET → RESET
CRAMCS → CRAMCS
RED → RED
GREEN → GREEN
BLUE → BLUE
Archivo: colmix.kicad_sch

JT

Konami schematic — input/data bus section

Left column switch blocks (KONAMI_005273):

S34
- 3P_BTN_3D → A0 Y0 → R3P_BTN_3
- 4P_BTN_3D → A1 Y1 → R4P_BTN_3
- COIN_3D → A2 Y2 → RCOIN_3
- COIN_4D → A3 Y3 → RCOIN_4

S33
- 3P_BTN_1D → A0 Y0 → R3P_BTN_1
- 4P_BTN_1D → A1 Y1 → R3P_BTN_1
- 3P_BTN_2D → A2 Y2 → R3P_BTN_2
- 4P_BTN_2D → A3 Y3 → R4P_BTN_2

S37
- 3P_LEFTD → A0 Y0 → R3P_LEFT
- 4P_LEFTD → A1 Y1 → R4P_LEFT
- 3P_RIGHTD → A2 Y2 → R3P_RIGHT
- 4P_RIGHTD → A3 Y3 → R4P_RIGHT

S36
- 3P_UPD → A0 Y0 → R3P_UP
- 4P_UPD → A1 Y1 → R4P_UP
- 3P_DOWND → A2 Y2 → R3P_DOWN
- 4P_DOWND → A3 Y3 → R4P_DOWN

S40
- 1P_BTN_3D → A0 Y0 → R1P_BTN_3
- 2P_BTN_3D → A1 Y1 → R2P_BTN_3
- COIN_1D → A2 Y2 → RCOIN_1
- COIN_2D → A3 Y3 → RCOIN_2

S39
- 1P_BTN_1D → A0 Y0 → R1P_BTN_1
- 2P_BTN_1D → A1 Y1 → R2P_BTN_1
- 1P_BTN_2D → A2 Y2 → R1P_BTN_2
- 2P_BTN_2D → A3 Y3 → R2P_BTN_2

S43
- 1P_LEFTD → A0 Y0 → R1P_LEFT
- 2P_LEFTD → A1 Y1 → R2P_LEFT
- 1P_RIGHTD → A2 Y2 → R1P_RIGHT
- 2P_RIGHTD → A3 Y3 → R2P_RIGHT

S42
- 1P_UPD → A0 Y0 → R1P_UP
- 2P_UPD → A1 Y1 → R2P_UP
- 1P_DOWND → A2 Y2 → R1P_DOWN
- 2P_DOWND → A3 Y3 → R2P_DOWN

74LS257 blocks:

C17 (74LS257)
- R3P_BTN_1 / R4P_BTN_1 → I0a/I1a → Za → MAIN_D12
- R3P_BTN_2 / R4P_BTN_2 → I0b/I1b → Zb → MAIN_D13
- RCOIN_3 / RCOIN_4 → I0c/I1c → Zc → MAIN_D15
- R3P_BTN_3 / R4P_BTN_3 → I0d/I1d → Zd → MAIN_D14
- PLAYER1 → S, MAIN_A1 → OE

C18 (74LS257)
- R3P_UP / R4P_UP → Za → MAIN_D8
- R3P_DOWN / R4P_DOWN → Zb → MAIN_D9
- R3P_RIGHT / R4P_RIGHT → Zc → MAIN_D11
- R3P_LEFT / R4P_LEFT → Zd → MAIN_D10
- PLAYER1 → S, MAIN_A1 → OE

C15 (74LS257)
- R1P_BTN_1 / R2P_BTN_1 → Za → MAIN_D4
- R1P_BTN_2 / R2P_BTN_2 → Zb → MAIN_D5
- RCOIN_1 / RCOIN_2 → Zc → MAIN_D7
- R1P_BTN_3 / R2P_BTN_3 → Zd → MAIN_D6
- PLAYER1 → S, MAIN_A1 → OE

CC15 (74LS257)
- R1P_UP / R2P_UP → Za → MAIN_D0
- R1P_DOWN / R2P_DOWN → Zb → MAIN_D1
- R1P_RIGHT / R2P_RIGHT → Zc → MAIN_D3
- R1P_LEFT / R2P_LEFT → Zd → MAIN_D2
- PLAYER1 → S, MAIN_A1 → OE

MAIN_D[15..0]

TESTD, SW17, EVQ-QS5-07K
- R13 220Ω, R14 3.3KΩ, VCC, B15
- CC3 104, VSS
- B[15..0]

S44 (KONAMI_005273)
- 1P_STARTD → A0 Y0 → B9
- 2P_STARTD → A1 Y1 → B10
- 3P_STARTD → A2 Y2 → B11
- 4P_STARTD → A3 Y3 → B12

S54 (KONAMI_005273)
- SERVICE1D → A0 Y0 → B1
- SERVICE2D → A1 Y1 → B2
- 3P_SERVD → A2 Y2 → B3
- 4P_SERVD → A3 Y3 → B4

R33 4.7KΩ, SW-B12, SLIDESW1P, OFF/ON, VSS, NOT MOUNTED

C16 3-StateHexBuffers (74LS367)
- B9 → I1 → O1a → MAIN_D8
- B10 → I2 → O2a → MAIN_D9
- B11 → I3 → O3a → MAIN_D10
- B12 → I4 → O4a → MAIN_D11
- B15 → I5 → O5b → MAIN_D14
- → I6 → O6b → MAIN_D15
- PLAYER2 → OEa / OEb

D16 3-StateHexBuffers (74LS367)
- B8 → I1 → O1a → MAIN_D0
- B7 → I2 → O2a → MAIN_D1
- B4 → I3 → O3a → MAIN_D2
- B3 → I4 → O4a → MAIN_D3
- B2 → I5 → O5b → MAIN_D6
- B1 → I6 → O6b → MAIN_D7
- PLAYER2 → OEa / OEb

D17 (74LS175) FOUR FLIP FLOP WITH DOUBLE RAIL OUTPUTS
- MAIN_D8 → D0, Q0, Q̄0 → OCHARA
- MAIN_D9 → D1, Q1, Q̄1 → VCHARA
- MAIN_D10 → D2, Q2, Q̄2 → SDON
- MAIN_D11 → D3, Q3, Q̄3 → MYUT
- Cp, Mr, RESETD

UDSD → 74LS32 F17D 11

CC13 (74LS174) hex flip flop
- MAIN_D0 → D0 Q0
- MAIN_D1 → D1 Q1
- MAIN_D2 → D2 Q2
- MAIN_D3 → D3 Q3
- MAIN_D4 → D4 Q4
- MAIN_D5 → D5 Q5
- Cp, Mr, RESET
- → INTDMAEN
- 74LS32 B14B

B13 ER5911 EEPROM
- CS, CLK, DI, RDY/BUSY, ORG, DO
- 128X8 or 64X16
- VSS, B7, B8

Decoder section:
- MAIN_A1 → E17A 74LS04 → MAIN_A1
- MAIN_A6, MAIN_A5 → A1 / A0, D15B → 74LS139 decoder → O0 O1 O2 O3 → PAIRCS, PCUCS
- IOCCS1D → E
- MAIN_A3, MAIN_A2 → A1 / A0, D15A → 74LS139 decoder → O0 O1 O2 O3 → PLAYER1, PLAYER2, CRCS
- MAIN_A[6..1]
- MROD → B14C 74LS32 9,10,8
- IOCCS2D → B14A 74LS32
- R/WD → 74LS32

F5B (74LS74)
- VSS → D, PASD → , VCC → Q̄ → AFE

FL-B12 VCC
- VSS, +12V
- AFE, JP-A12, SJ0

A11 (KONAMI 051550) Master/RESET generation for the whole system and the watchdog timer
- CLK, VREF, RES, CT, VS, OUT1, OUT2
- +5V, +12V
- RESET, CNT2, CNT2, CNT1, CNT1 → COIN_CNT_2, COIN_CNT_1
- N.C ×...

CP76 C_Small, VSS

G18A (74LS74)
- D, Q, Q̄ → SYSRES
- VCC

G12 XTAL_OSC 24MHz, VSS
- **H11C** 74LS04 → SCRCLK

JT

NOT MOUNTED

RA24 4.7kX8 RA25 4.7kX8 RA26 4.7kX8 RA27 4.7kX8

GFXROMA[18..0]

CN5 DIN64SS

J17 74LS373 — LATCHES AND FLIP FLOPS
H17 74LS373 — LATCHES AND FLIP FLOPS

OBJCLK12
G18B 74LS04
H18A 74LS74

L15 065A08 KONAMI MASK 8M – 16BIT — CMOS ROM — 054903
L16 065A08 KONAMI MASK 8M – 16BIT — CMOS ROM — 054903

GFXROMD[31..0]

J14 KONAMI 051962 TILE DRAWING

APAL[4..0]   SCRA   ACOL[3..0]
FIX   FCOL[3..0]
FPAL[3..0]
H11A 74LS04   VSYNC

OBJCLK6
MAIN_D[7..0]
BCOL[3..0] SCRB
BPAL[4..0]

LAYER A TRANSPARENCY
FIX LAYER TRANSPARENCY
CPU DATA TO READ GFX ROMS
LAYER B TRANSPARENCY
LAYER B COLOR INDEX
ATTRIBUTE CODE FROM 052109

G14 KONAMI 052109 TILE MAP GENERATOR

MAIN_A[16..1]

LAYER A SCROLL X
LAYER B SCROLL X
TILE ATTRIBUTES
GFX ROM ADDRESS
VRAM ADDRESS
GFX ROM read
VRAM DATA   CPU DATA

SCRAMA[12..0]

F13 CMOS Static RAM 8K x 8 BITS
F14 CMOS Static RAM 8K x 8 BITS
F15 CMOS Static RAM 8K x 8 BITS

VD[15..0]

D18 74LS367 3–State Hex Buffers
R7 470Ω
R5 100Ω
CSYNC
SYNC

JT

MAIN_A[11..0]
MAIN_D[15..0]
SHD[1..0]
PRI[4..0]
VCC
PRI4

K13
KONAMI
053251
PRIORITY CONTROL UNIT

PRIORITY
COLOR INPUTS

ACOL[3..0]
SCRA
APAL[4..0]
OCOL[8..0]

CHIP SELECT INPUT CS
COLOR OUTPUTS

10 74LS04 11
M11E
OBJCLK6

81 PCUCS

COL[10..0]
COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8
COL9
COL10

SDO1
SDO0
BRIT
NCOL

9
F18C
10 74LS32
8 SHAD

VCC
VSS

BCOL[3..0]
SCRB
BPAL[4..0]
FCOL[3..0]
FIX
FPAL[3..0]

Quad Mux J11
MAIN_A1
MAIN_A2
MAIN_A3
MAIN_A4
COL0
COL1
COL2
COL3
CRAMCS
VSS
74LS157
MCOL0
MCOL1
MCOL2
MCOL3

Quad Mux J10
MAIN_A5
MAIN_A6
MAIN_A7
MAIN_A8
COL4
COL5
COL6
COL7
CRAMCS
VSS
74LS157
MCOL4
MCOL5
MCOL6
MCOL7

Quad Mux J9
MAIN_A9
MAIN_A10
MAIN_A11
CRAMCS
COL8
COL9
COL10
VSS
CRAMCS
VSS
74LS157
MCOL8
MCOL9
MCOL10

MCOL[10..0]

HM6116P-3 H9 MCM2018 2kB RAM
MCOL0 A0 D0
MCOL1 A1 D1
MCOL2 A2 D2
MCOL3 A3 D3
MCOL4 A4 D4
MCOL5 A5 D5
MCOL6 A6 D6
MCOL7 A7 D7
MCOL8 A8
MCOL9 A9
MCOL10 A10
VSS CS
MCOOE OE
MCOWRLD WR

RGB0
RGB1
RGB2
RGB3
RGB4
RGB5
RGB6
RGB7

HM6116P-3 H10 MCM2018 2kB RAM
MCOL0 A0 D0
MCOL1 A1 D1
MCOL2 A2 D2
MCOL3 A3 D3
MCOL4 A4 D4
MCOL5 A5 D5
MCOL6 A6 D6
MCOL7 A7 D7
MCOL8 A8
MCOL9 A9
MCOL10 A10
VSS CS
MCOOE OE
MCOWRHD WR

RGBB
RGB9
RGB11
RGB12
RGB13
RGB14
RGB15

RGB[15..0]

rgb
CRAMCS CRAMCS REDD RED
RESETD RESET GREEND GREEN
HBLANKD HBLANK BLUED BLUE
VBLANKD VBLANK
MRDD MRD
OBJCLK6 OBJCLK6
RGB[15..0] RGB[15..0]
MAIN_D[15..0] MAIN_D[15..0]
SHAD SHAD
Archivo: rgb.kicad_sch

JT

Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

BHE = VIH; 16-bit (D15 to D0)
BHE = VIL; 8-bit (D7 to D0)

EQUATIONS TO REVIEW

SND PAL8 = A15 & A14 & A13 & $\overline{A12}$ & A9 & A10 +
SM1 & ($\overline{A15 \& A14 + A14}$)
SPAL8 = 0000-ECFF

SCEN' = $\overline{SRFSH}$ & $\overline{SMREQ}$ & A15 & A14 & A13 & A12 & A9 & $\overline{A10}$
SCEN' = F4XX*

SNDPAL5 = $\overline{SRFSH}$ & $\overline{SMREQ}$ & A15 & A14 & A13 & A12 & $\overline{A9}$
SNDPAL5 = F0XX*

YMCS = $\overline{SRFSH}$ & $\overline{SMREQ}$ & A15 & A14 & A13 & $\overline{A12}$ & A9
YMCS = E2XX*

SNDPAL3 = $\overline{SRFSH}$ & $\overline{SMREQ}$ & A15 & A14 & A13 & $\overline{A12}$ & $\overline{A9}$
SNDPAL3 = E0XX*

SRAMCS1 = $\overline{SRFSH}$ & $\overline{SMREQ}$ & A15 & A14 & $\overline{A13}$
SRAMCS1 = C000-DFFF

SROMCE = $\overline{SRD}$ & $\overline{SRFSH}$ & $\overline{SMREQ}$ & ($\overline{A15}$ & A14 + $\overline{A14}$)
SROMCE = 0000-BFFF

-- NOT CONNECTED --
/o13 = $\overline{SRFSH}$ & $\overline{SMREQ}$ & ($\overline{A15}$ & A14 + $\overline{A14}$)
O13 = 0000-BFFF

Sound communication latch/volume manager chip

THIS CONNECTOR REPLACES THE PINS OF THE KONAMI CI 054544

MAIN_D[7..0]

SND_A[1..0]

VCC

MAIN_A[4..0]

VCC
C4

SND_D[7..0]

SHORTED ON MOTHER PCB

1.54-1.53MHz

8MHz

C4-1
KONAMI
054321
PCM

* Channel Latch Enable
*AD1868R * Left Channel Data Output
*Right Channel Data Output
AND Z80 SOUND *
*Z80 SOUND *

054539 SND IC *

+12V
R31
4.7kΩ

R30
10kΩ

MYUTD C1C4
74LS07

MYUTB

CP9
1µF

CP12   CP3
1µF   1µF

C4-2

SIC_CLK

P40
P36

VOR
VOL

P32
P33

CP6   CP7
4.7µF 4.7µF

VSS

Pins 8 and 16 of the AD1868R are connected to pins 40 and 36 of the 054544 respectively.
but these pins (40 and 36) are floating.

WAIT

74LS08
F16C

BUSYD   SWAIT

SRST
SINT

C4-3A
MC3320

RR1
310Ω

RR3 310Ω

CP13 1µF

MC3320
C4-3B

RR2
310Ω

R4   310Ω

CP14 1µF

RR5
310Ω

CP20 1µF

RR7
310Ω

VSS

R6
310Ω

CP15 1µF

R8
310Ω

VSS

KONAMI 054544
Audio module

SOUND AMPLIFIER MOTHER PCB

+12V

CC2
104

CP38
330µF

R26
10kΩ

VSS

CP132
10µF

VSS

VOR CP127
4.7M16T

R20
3.9KΩ

R22
10kΩ

A4B
LM358

R19
3.3KΩ

+12V

R25
4.7kΩ

R29
1kΩ

CP131
4.7M16T

VSS

+12V

R18
3.3KΩ

A4A
LM358

R24
4.7kΩ

CP130
4.7M16T

R28
1kΩ

CP133
2.2nF

VSS   VSS

R27
10kΩ

VSS

VOL CP126
4.7M16T

R21
3.9KΩ

R23
10kΩ

A1

IN-A
NFBA
BYPASS
NFBB
IN-B
VSS
VSS
OUT-B
BSB
BSA
OUT-A
MB3722

NFBA
NFBA
MYUTB
NFBB

+12V
VCC

CP114
1000µF

A,G-JP1
JPB

CC1
104

VSS

CN8
SOUND OUT

CP115
1000µF

CP128
0.1µF

VSS

LS1
Speaker

SPEAKER(+)

SPEAKER(−)

VSS

CP16
470µF

CP134   CP17 CP2   CP1
2.2nF   470µF 470µF 470µF

CP11
1µF

OUT-B
BSB
BSA

CP18 CP4
4.7µF 4.7µF

CP5   CP19
4.7µF 4.7µF

CP116
1000µF

CP129
0.1µF

VSS

JT

VCC

CP77	C78	C79	C80	C81	C82	C83	C84	C85	C86	C91	C99	C100	C101	C102	C103	C104	C105	C106	C118	C120	C121	C124
104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104

4 — F17B 74LS32 — 6
5 —

4 — F16B 74LS08 — 6
5 —

| F5C 74LS74 | B14E 74LS32 | F17E 74LS32 | E17G 74LS04 | B11G 74LS07 | C12G 74LS07 | CC11G 74LS07 | C11G 74LS07 | F16E 74LS08 | E16E 74LS00 | E18C 74LS74 | D15C 74LS139 decoder | H11G 74LS04 | F18E 74LS32 | G18C 74LS74 | C13E 74LS32 | F4E 74LS32 | A4C LM358 | C4-3C MC33202 |

14 VCC 14 VCC 14 VCC 14 VCC
7 GND 7 GND 7 GND 7 GND

8 V+ 8 V+
4 V− 4 V−

VSS

X-Men (1992 video game)

X-Men (エックス・メン) is a side-scrolling beat 'em up game produced and released by Konami for arcades in 1992, based on the Marvel Comics superhero team of the same name. The character designs of the characters in the game are based on the 1989 cartoon X-Men: Pryde of the X-Men. In the game, up to six players control the X-Men to defeat their archenemy Magneto. The six-player version of the game utilizes two screens housed in a deluxe cabinet. It was one of the top five highest-grossing dedicated arcade games of 1992 in the United States, while the Amusement & Music Operators Association (AMOA) nominated it for the "most innovative new technology" award.

An arcade exclusive for many years, a home version of the game developed by Backbone Entertainment was released by Konami digitally on the PlayStation 3 and Xbox 360 in 2010, followed by mobile versions for iOS and Android devices.
This version is no longer available for purchase as of 2013.

HARDWARE DESCRIPTION

Video Chips : 052109 051962 053247 053246 053251

CPU : 68000 ($\overline{RESET}$ generator 051550)

Sound : Z80 YM2151 054539 054544 (PCM054321 AD1868R)