

These schematics cover the missing pages in the original ones published by the maker. Signal names existing in the original pages have been preserved. New signal names try to follow the maker style or are taken from similar schematics of the same maker.

The schematic shows a complex interconnection of components. Key components include:

- 74LS244** (D29): A hex inverter/driver.
- 74LS257** (A26, B26): 4-to-1 multiplexers.
- 74LS253** (C24, C25, D24, D25): 4-bit binary counters.
- 74LS174** (B22): A hex flip-flop.
- 74LS04** (F15A, F15B): Hex inverters.
- 74LS00** (U1): A hex NAND gate.
- 74LS08** (U2): A hex AND gate.
- 74LS00** (U3): A hex NAND gate.
- 74LS08** (U4): A hex AND gate.
- 74LS00** (U5): A hex NAND gate.
- 74LS08** (U6): A hex AND gate.
- 74LS00** (U7): A hex NAND gate.
- 74LS08** (U8): A hex AND gate.
- 74LS00** (U9): A hex NAND gate.
- 74LS08** (U10): A hex AND gate.
- 74LS00** (U11): A hex NAND gate.
- 74LS08** (U12): A hex AND gate.
- 74LS00** (U13): A hex NAND gate.
- 74LS08** (U14): A hex AND gate.
- 74LS00** (U15): A hex NAND gate.
- 74LS08** (U16): A hex AND gate.
- 74LS00** (U17): A hex NAND gate.
- 74LS08** (U18): A hex AND gate.
- 74LS00** (U19): A hex NAND gate.
- 74LS08** (U20): A hex AND gate.
- 74LS00** (U21): A hex NAND gate.
- 74LS08** (U22): A hex AND gate.
- 74LS00** (U23): A hex NAND gate.
- 74LS08** (U24): A hex AND gate.
- 74LS00** (U25): A hex NAND gate.
- 74LS08** (U26): A hex AND gate.
- 74LS00** (U27): A hex NAND gate.
- 74LS08** (U28): A hex AND gate.
- 74LS00** (U29): A hex NAND gate.
- 74LS08** (U30): A hex AND gate.
- 74LS00** (U31): A hex NAND gate.
- 74LS08** (U32): A hex AND gate.
- 74LS00** (U33): A hex NAND gate.
- 74LS08** (U34): A hex AND gate.
- 74LS00** (U35): A hex NAND gate.
- 74LS08** (U36): A hex AND gate.
- 74LS00** (U37): A hex NAND gate.
- 74LS08** (U38): A hex AND gate.
- 74LS00** (U39): A hex NAND gate.
- 74LS08** (U40): A hex AND gate.
- 74LS00** (U41): A hex NAND gate.
- 74LS08** (U42): A hex AND gate.
- 74LS00** (U43): A hex NAND gate.
- 74LS08** (U44): A hex AND gate.
- 74LS00** (U45): A hex NAND gate.
- 74LS08** (U46): A hex AND gate.
- 74LS00** (U47): A hex NAND gate.
- 74LS08** (U48): A hex AND gate.
- 74LS00** (U49): A hex NAND gate.
- 74LS08** (U50): A hex AND gate.
- 74LS00** (U51): A hex NAND gate.
- 74LS08** (U52): A hex AND gate.
- 74LS00** (U53): A hex NAND gate.
- 74LS08** (U54): A hex AND gate.
- 74LS00** (U55): A hex NAND gate.
- 74LS08** (U56): A hex AND gate.
- 74LS00** (U57): A hex NAND gate.
- 74LS08** (U58): A hex AND gate.
- 74LS00** (U59): A hex NAND gate.
- 74LS08** (U60): A hex AND gate.
- 74LS00** (U61): A hex NAND gate.
- 74LS08** (U62): A hex AND gate.
- 74LS00** (U63): A hex NAND gate.
- 74LS08** (U64): A hex AND gate.
- 74LS00** (U65): A hex NAND gate.
- 74LS08** (U66): A hex AND gate.
- 74LS00** (U67): A hex NAND gate.
- 74LS08** (U68): A hex AND gate.
- 74LS00** (U69): A hex NAND gate.
- 74LS08** (U70): A hex AND gate.
- 74LS00** (U71): A hex NAND gate.
- 74LS08** (U72): A hex AND gate.
- 74LS00** (U73): A hex NAND gate.
- 74LS08** (U74): A hex AND gate.
- 74LS00** (U75): A hex NAND gate.
- 74LS08** (U76): A hex AND gate.
- 74LS00** (U77): A hex NAND gate.
- 74LS08** (U78): A hex AND gate.
- 74LS00** (U79): A hex NAND gate.
- 74LS08** (U80): A hex AND gate.
- 74LS00** (U81): A hex NAND gate.
- 74LS08** (U82): A hex AND gate.
- 74LS00** (U83): A hex NAND gate.
- 74LS08** (U84): A hex AND gate.
- 74LS00** (U85): A hex NAND gate.
- 74LS08** (U86): A hex AND gate.
- 74LS00** (U87): A hex NAND gate.
- 74LS08** (U88): A hex AND gate.
- 74LS00** (U89): A hex NAND gate.
- 74LS08** (U90): A hex AND gate.
- 74LS00** (U91): A hex NAND gate.
- 74LS08** (U92): A hex AND gate.
- 74LS00** (U93): A hex NAND gate.
- 74LS08** (U94): A hex AND gate.
- 74LS00** (U95): A hex NAND gate.
- 74LS08** (U96): A hex AND gate.
- 74LS00** (U97): A hex NAND gate.
- 74LS08** (U98): A hex AND gate.
- 74LS00** (U99): A hex NAND gate.
- 74LS08** (U100): A hex AND gate.

The schematic is a single-page layout with a title block at the bottom right containing project information and a logo.