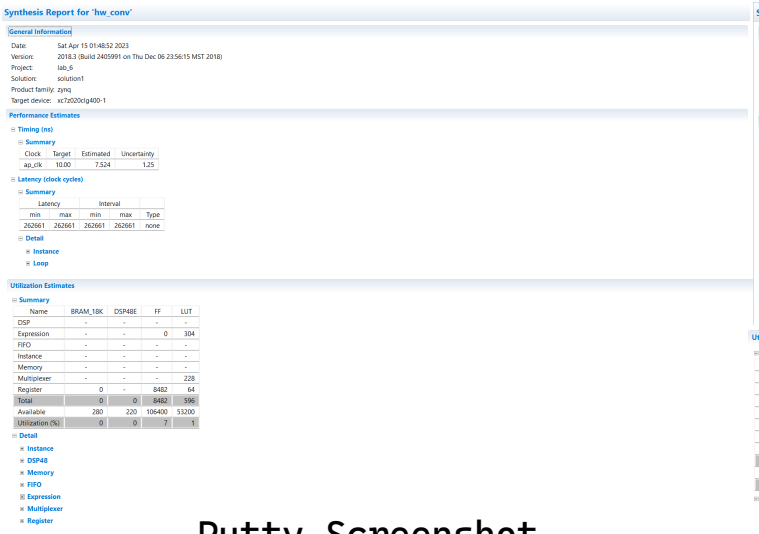
Justin Pacella 04/16/2023

Lab 6 Report
Hardware Acceleration for 2d Convolution

Shift Register Implementation



Synthesis Report for 'hw_conv'

General Information

Date: Sat Apr 15 01:48:52 2023
Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project: lab_6
Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.524	1.25

Latency (clock cycles)

Summary

Latency		Interval	
min	max	min	max	Type
262661	262661	262661	262661	none

Detail

Instance

Loop

Utilization Estimates

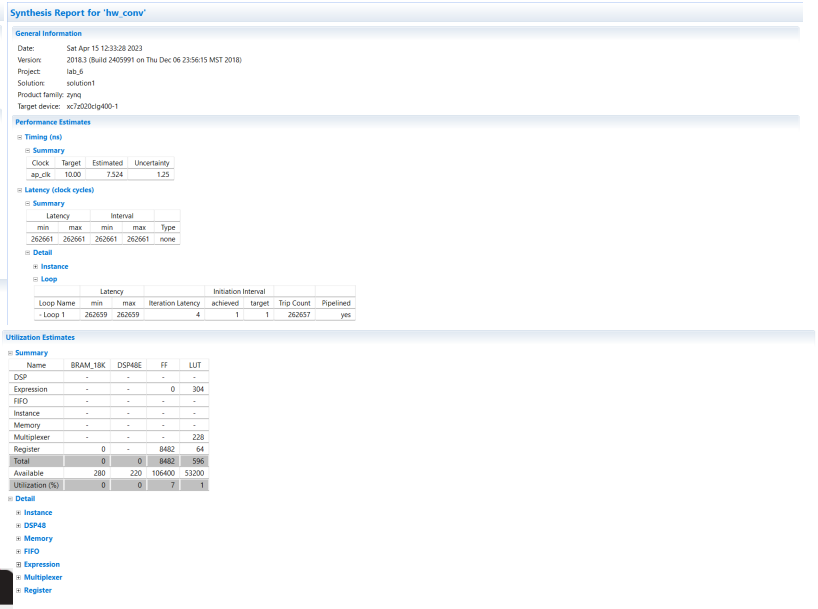
Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	304
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	228
Register	0	-	8482	64
Total	0	0	8482	596
Available	280	220	106400	53200
Utilization (%)	0	0	7	1

Detail

Instance
DSP48
Memory
FIFO
Expression
Multiplexer
Register

Ring Buffer Implementation



Synthesis Report for 'hw_conv'

General Information

Date: Sat Apr 15 12:33:28 2023
Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project: lab_6
Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.524	1.25

Latency (clock cycles)

Summary

Latency		Interval	
min	max	min	max	Type
262661	262661	262661	262661	none

Detail

Instance

Loop

Loop Name	Latency min	Latency max	Iteration Latency	Initiation Interval achieved	Initiation Interval target	Trip Count	Pipelined
- Loop 1	262659	262659	4	1	1	262657	yes

Utilization Estimates

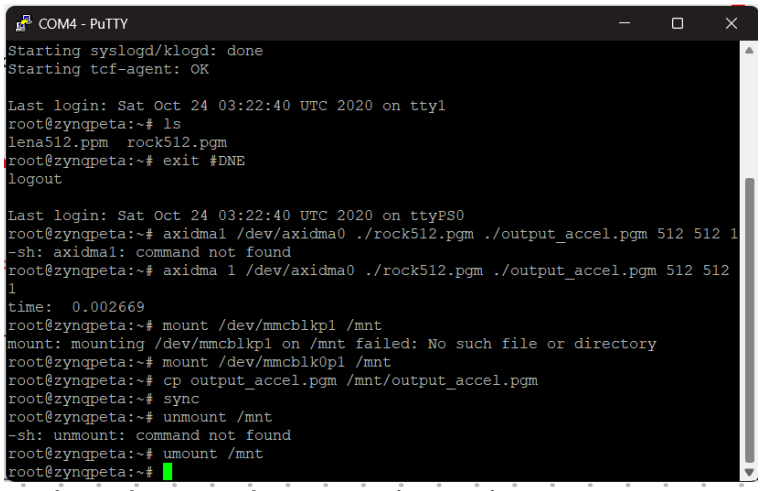
Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	304
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	228
Register	0	-	8482	64
Total	0	0	8482	596
Available	280	220	106400	53200
Utilization (%)	0	0	7	1

Detail

Instance
DSP48
Memory
FIFO
Expression
Multiplexer
Register

Putty Screenshot



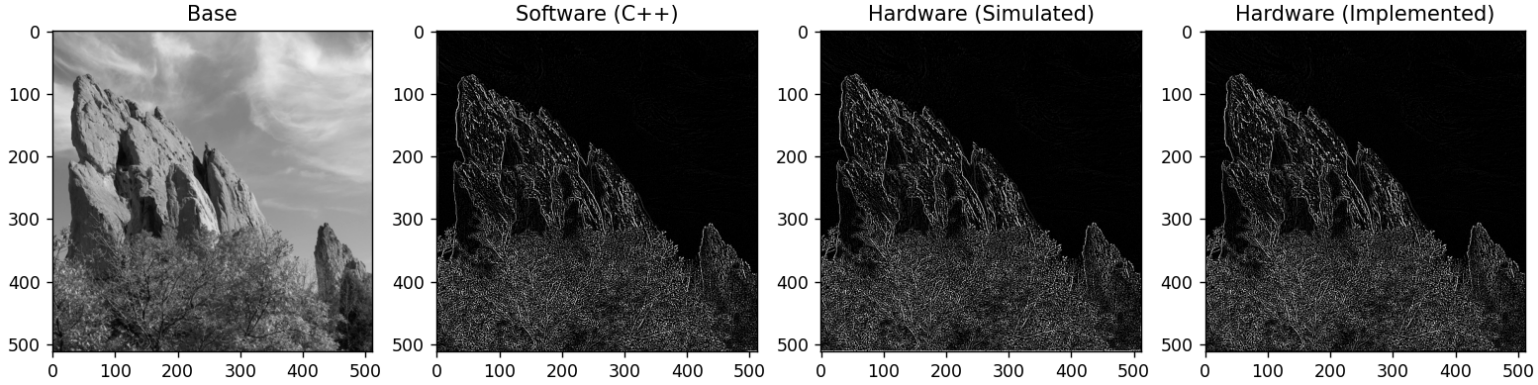
```
COM4 - PuTTY
Starting syslogd/klogd: done
Starting tcf-agent: OK

Last login: Sat Oct 24 03:22:40 UTC 2020 on tty1
root@zynqpeta:~# ls
lena512.ppm  rock512.pgm
root@zynqpeta:~# exit #DNE
logout

Last login: Sat Oct 24 03:22:40 UTC 2020 on ttyPS0
root@zynqpeta:~# axidma1 /dev/axidma0 ./rock512.pgm ./output_accel.pgm 512 512 1
-sh: axidma1: command not found
root@zynqpeta:~# axidma 1 /dev/axidma0 ./rock512.pgm ./output_accel.pgm 512 512
1
time:  0.002669
root@zynqpeta:~# mount /dev/mmcblkp1 /mnt
mount: mounting /dev/mmcblkp1 on /mnt failed: No such file or directory
root@zynqpeta:~# mount /dev/mmcblk0p1 /mnt
root@zynqpeta:~# cp output_accel.pgm /mnt/output_accel.pgm
root@zynqpeta:~# sync
root@zynqpeta:~# unmount /mnt
-sh: unmount: command not found
root@zynqpeta:~# umount /mnt
root@zynqpeta:~#
```

The observed execution time was 2.669 milliseconds. This roughly corresponds to the predicted 2.627 milliseconds (clock_prd * latency = 10ns * 262661).

Output Images



The images resulting from each implementation seem to be identical. However, the simulated hardware output has a small (1 pixel) bright strip along the bottom. The explanation for this likely resides in how Vivado HLS simulates hardware on a CPU.