Name: _____

Lab 1: Zynq-SoC Design Flow

____/10 VHDL for Full adder

____/10 VHDL for 32-bit adder/sub (using generic and for-generate)

____/10 VHDL testbench (corner cases & random testing)

____/10 VHDL testbench simulation (running correctly, assert report (if any))

____/15 Generating bitstream successfully

____/10 C\C++ testbench (corner cases & random testing)

____/15 C\C++ testbench simulation (running correctly)