2110352 Computer System Architecture
1st semester/2016
Assignment II

In this exercise, we will create and use the cache simulator for studying the factors that affects the performance of cache accesses. The cache simulator will read an address trace file from *gcc_ld_trace.txt* or *go_ld_trace.txt* . The simulator will show us a number of cache hit, a number of cache miss, miss rate, and access time. Please form a group of 2 students and follow the instruction.

Instruction

1. Please create the cache simulator which can simulate scenarios in the following table.
   a. Block Size Tradeoff on direct mapped cache

	Direct mapped			
Block Size (Bytes)	*Cache Size(KB)*			
	4	8	16	32
4				
8				
16				
32				

   b. N-way associativity cache with replacement algorithms: Least recently used (LRU), and Round Robin (RR).

	Associativity			
Cache Size (KB)	*Two-way*		*Four-Way*	
	LRU	RR	LRU	RR
1				
4				
8				
32				
512				
1024				

2. Please use one address trace and simulate result.
3. Please fill miss rate and plot graph for each table.

Hint

You can check Simulator.c for an example. It is a simple direct mapped cache simulator.

*Simulator.c need file path as parameter