Pune Institute of Computer Technology, Pune-43
DEPARTMENT OF INFORMATION TECHNOLOGY
(Academic Year – 2023-24 Sem-II)
UNIT TEST - I

Subject: Processor Architecture — Subject Code: 214451
Class: SE — Div.: IX, X, XI — [Max. Marks: 30]
Date: 20 /02/2024 — Day: Tuesday — Duration: 1 Hour

Instructions to the candidate:

1. All questions are compulsory
2. Draw a neat diagram wherever necessary.

Que. No.	Questions	Max Marks	CO Mapped	Bloom's Learning Level
1-a	Draw and explain the architecture of PIC18F4550 Microcontroller.	05	CO-I	L2
1-b	Draw and explain Data memory organization of PIC18F4550 Microcontroller.	05	CO-I	L2
2-a	Write an embedded C program to add an array of n numbers.	05	CO-II	L3
2-b	Write an embedded C menu driven program for a) Multiply 8-bit no. by 8-bit no. b) Divide 8-bit no. by 8-bit no.	05	CO-II	L3
3-a	Explain with neat diagram Timer0, 16-bit mode operation.	05	CO-III	L2
3-b	What value is required to load in the timer0 register to generate square wave of 10Hz. (Assume that XTAL = 20 MHz and Prescaler value=1:16)	05	CO-III	L3

Course Outcomes (CO Mapped):

CO-I	**Apprehend** architecture and memory organization of PIC 18 microcontroller. Compare and contrast MP and MC.
CO-II	**Implement** embedded C programming for PIC 18. Demonstrate with MPLAB.
CO-III	**Use** concepts of timers and interrupts of PIC 18. Programming the timer for a given delay.

Bloom's Taxonomy (Bloom's Learning Level):

L1	Remembering	Recall specific facts
L2	Understanding	Grasp meaning of materials
L3	Applying	Use information in a new situation
L4	Analyzing	Identify schemas or relationships
L5	Evaluating	Use information to make judgments
L6	Creating	Create or develop something new

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