Total No. of Questions : 4]

SEAT No. :

**PA-4980**

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# S.E. (Information Technology) (Insem)

## PROCESSOR ARCHITECTURE

## (2019 Pattern) (Semester - II) (214451)

*Time : 1 Hour]* *[Max. Marks : 30*

*Instructions to the candidates:*

1) *Answer Q1 or Q2, Q3 or Q4.*
2) *Neat diagrams must be drawn whenever necessary.*
3) *Figures to the right side indicate full marks.*
4) *Assume suitable data if necessary.*

*Q1)* a) Explain program memory organization of PIC18 micro controller with suitable diagram. [6]

b) Draw and explain status register of PIC18 microcontroller. [5]

c) Explain watchdog timer used in PIC18 microcontroller. [4]

OR

*Q2)* a) With a neat diagram discuss in detail about the architecture of PIC18 micro controller. [6]

b) Write short note on Brownout Reset. [5]

c) Differentiate between RISC and CISC. [4]

*Q3)* a) Name the SFRs associated with each I/O port of PIC18F. What is the role of PORTx SFR? [4]

b) Calculate total delay generated by Timer 0 if (FFF1) H is loaded into it.

Assume Crystal frequency =10 MHz [4]

c) Explain working of PIC18F Timer1 with the help of suitable diagram. [7]

OR

*P.T.O.*

*Q4)* a) Find the value to be loaded in TRISD and TRISC resister for the following : [4]

RD0,RD1,RD2,RD3 as input port

RD4,RD5,RD6,RD7, as output port

RC0,RC2,RC4,RC6,RC7 as output port

RC1,RC3,RC5 as input port

b) Explain in detail Prescaling and Postscaleing of PIC18 Timers. [4]

c) Explain Timer0 Control Register T0CON in detail. [7]

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