CPU
Consists of: (Neumann Arch)
- ALU
- instruction register / program counter
- access to memory
- external storage
- I/O mechanisms

- some memory now stored inside cpu to reduce latency

CPU Caches
- L3 - shared between all cores (largest)
- L2 - internal in core but shared
- L1 - closest cache split in 2 - data and instructions

Registers -
- hold data being used for computations in CPU
  1. data fetched from memory
  2. operation performed
  3. repeat until final result
  4. result moved back from register to memory

x86 Registers: rax, rbx, rcx, ...
rsi - source index
rdi - destination index

Carry Flags - Indicate result of an operation i.e.:
CF: carry (overflow)
ZF: zero flag
SF: negative (sign) flag

Assembly
Instruction commands used to perform operations on the CPU