

Topic 0

Course Introduction

Instructional Support

- **Instructor:** Gang Zheng, Ph.D.
- **Office:** JI New Building 400E
- **Contact:** (021) 3420-6765 x4005, gzheng@sjtu.edu.cn
- **Office Hours:** W 4:00-6:00pm / Th 10:00am-12:00pm, or by appointment
- **TAs:** Mr. CHEN Rui, 2016jichenrui@sjtu.edu.cn
Ms. LI Yushan, littleantuanzi@sjtu.edu.cn
- **TA Office Hours:** TBD

What will be taught?

- How computers execute programs?
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How to design a processor (datapath and controller) as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

What you are expected to obtain

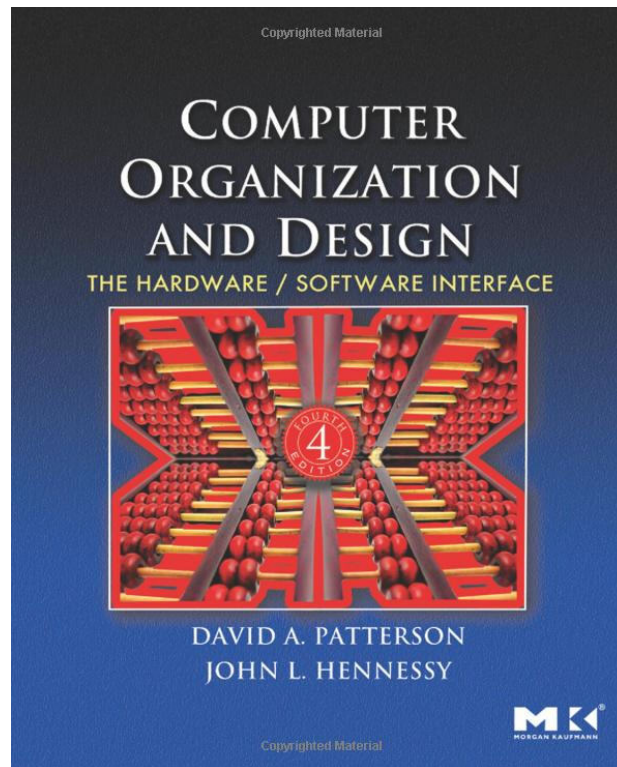
- Write an assembly language program that implements a task, translate the program into machine-level instructions, and trace the execution of the program.
- Model the computer hardware including datapath and control logic for a given instruction-set architecture by using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface the CPU
- Be able to use library and internet resources for literature search to learn the contemporary issues, technologies, and future development trends in computing

Topics to Cover

- Introduction to computer
- Software
 - MIPS instruction set, operands, operations, assembly programming
 - Instruction encoding, addressing mode
 - Procedures, memory usage, procedure calling conventions
- Hardware – CPU
 - Single cycle processor implementation
 - Pipelined datapath and control
 - Data hazards, control hazards, exceptions
- Hardware – Memory and other peripherals
 - Cache, virtual memory, virtual machine
 - I/Os devices and interfaces
- *Advanced topics*
 - *Parallelism, Multicores, multiprocessors, clusters*

Textbook

- David Patterson and John Hennessy, *Computer Organization and Design - Hardware/Software Interface*, 4th edition, Morgan Kaufmann, 2008, ISBN 978-0-12-374493-7



Course Policies

■ Honor Code

- All students in the class are bound by the Honor Code of the Joint Institute (see the related sections in *Jl Student Handbook* for details).
- You may not seek to gain an unfair advantage over your fellow students
- You may not consult, look at, or possess the unpublished work of another without their permission
- You must appropriately acknowledge your use of another's work
- Anyone violating Honor Code in an assignment/exam will receive 0 point for that assignment/exam

■ Attendance

- Attendance will be recorded randomly
- 5% will be deducted from the final grade for each absence starting from the 4th one.

Course Policies

■ Evaluation methods

- About 9 homework assignments, will not be graded, will be discussed in the classes, will be helpful for exams
- 4 projects (on software, hardware modeling, memory modeling, literature review), reports and demonstration
- 2 exams (paper based)

■ Submission

- project reports are due on a specified date and should be submitted electronically on Canvas.
- No late submission will be accepted.

Course Policies

■ Individual Assignments

- Project 1 and 4
- Literature search homework
- Students are encouraged to discuss course topics and assignments with each other
- However, all submissions must represent your own work. Duplicated submission is absolutely not allowed and will trigger an honor code violation investigation.

■ Group Assignments

- Project 2 and 3
- Team of 3 students
- The work submitted must reflect the work of the team.
- The grade for a group assignment will be shared among the entire team equally, unless specified differently.

Grading Policy

■ Homework	0%
■ Literature search homework*	2%
■ Midterm Exam 1	30%
■ Final Exam	30%
■ Project 1*	5%
■ Project 2**	25%
■ Project 3**	5%
■ Project 4*	3%
■ Total	100%

*Individual assignments

**Group assignments

Note: final letter grades may be curved