**State your assumptions and show all of your reasoning and all computations. All work must be done on this sheet.**

1. (8 pts) IF TIMER\_A1->CCR[0] =1000 (MCLK= 3 MHZ, compare mode, continuous mode), what is the period of Timer A1?

**ANSWER\_\_21.8 ms (max)\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

1. (5 pts) How many TIMER\_A modules are there in the MSP432?
   1. 1
   2. 2
   3. 4
   4. 16
   5. 32
2. (8 pts) IF TIMER\_A2 is used At 3 MHz, INPUT divider = /4, what is the time between counts?

ANSWER\_\_\_333ns\*4 = 1.332 uS\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. (8 pts) What value should you load into the CCR0 register if you wanted TimerA to count to 23 msec before rolling over? (Assume a 3 MHz clock)

ANSWER\_\_\_\_NOT POSSIBLE\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. (8 pts) Calculate the duty cycle of the following periodic waveform

3.3V

150 ms

200ms

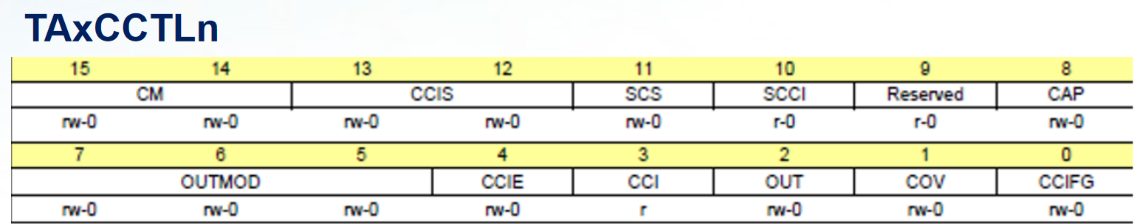
0V

ANSWER \_\_\_\_150/350=42%\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. (5 pts) Which of the following may be used to extend the time before 16-bit Timer A overflows:
   1. **Add more bits**
   2. **Use a different clock source**
   3. **Use a voltage divider**
   4. **Use a clock divider**
   5. **Travel faster (relativity thing…)**
2. (8 pts) Using only the register chart, determine the purpose of the following command: (looking for specifics- NOT just sets bit ‘x” of CCTL[1] to a “one”).

**TIMER\_A1->CCTL[1]= 0x0100;**

**ANSWER:\_\_\_\_\_\_Put into CAPTURE MODE\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**



Calendar

Description automatically generated