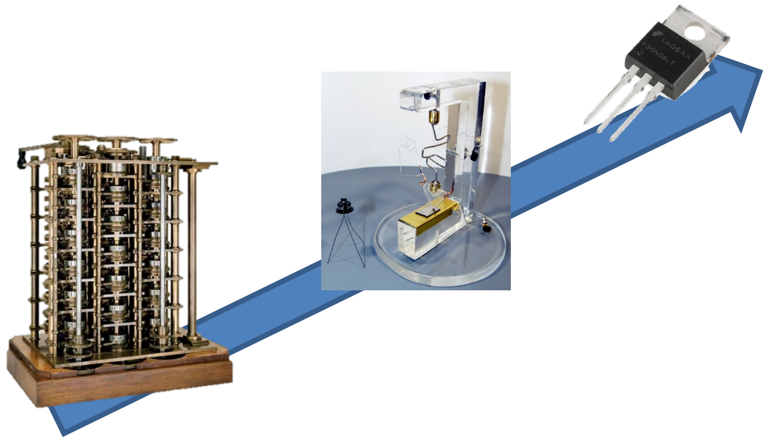
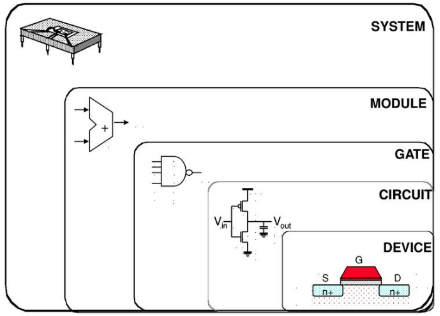
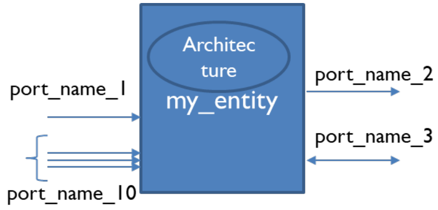
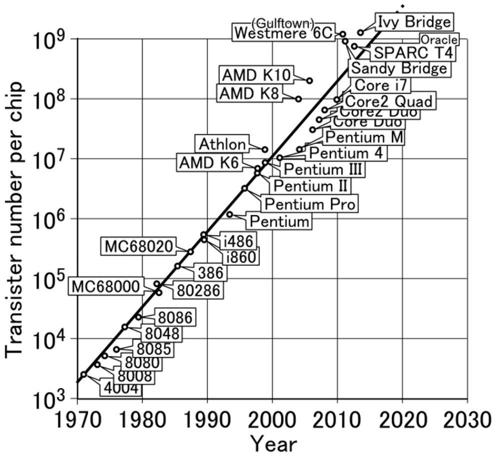
Summary of Lecture 1



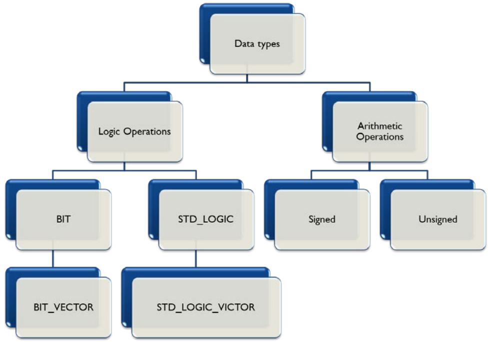




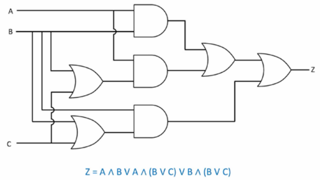

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity AND_Gate is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C : out STD_LOGIC);
end AND_Gate;

architecture Behavioral of AND_Gate is

begin
C <= A and B;

end Behavioral;
```

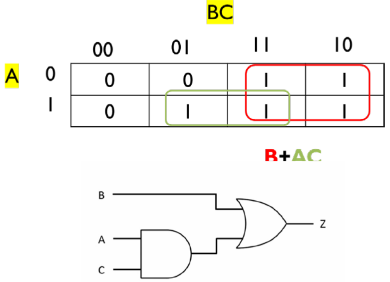


VHDL

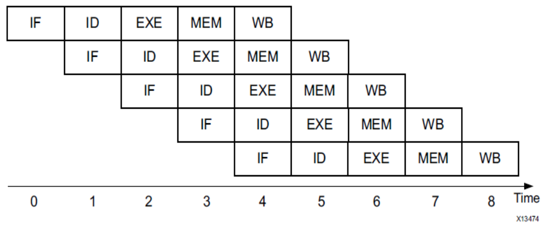


Character	Value
'U'	uninitialized
'X'	strong drive, unknown logic value
'0'	strong drive, logic zero
'1'	strong drive, logic one
'Z'	high impedance
'W'	weak drive, unknown logic value
'L'	weak drive, logic zero
'H'	weak drive, logic one
'-'	don't care





Summary of lecture 2



Processor with Multiple Instruction Execution Units

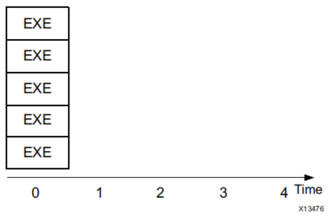
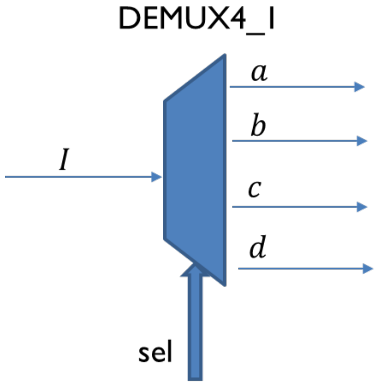
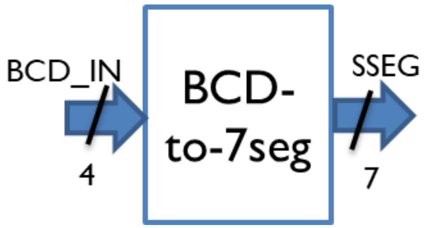
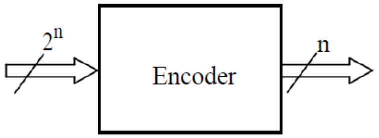
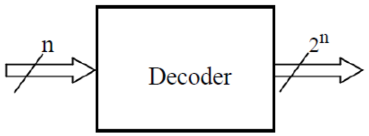


Figure 3-4: **FPGA with Multiple Instruction Execution Units**





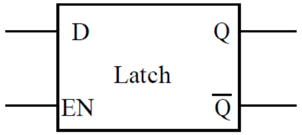


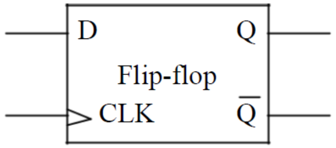


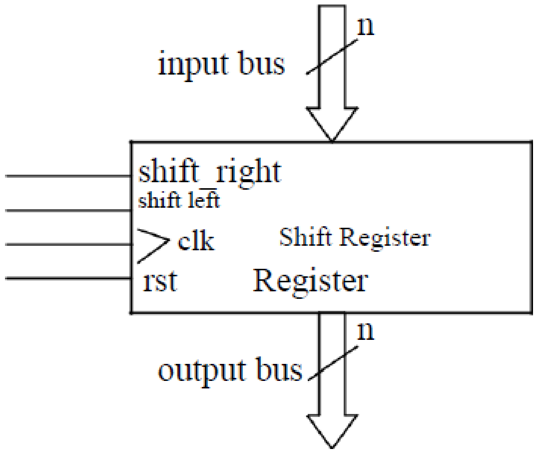
- Concurrent and Sequential statements
  - Conditional signal assignment (when)
  - Selected Signal Assignment (with select)
  - Process statement (if/else)
  - Process statement (case)

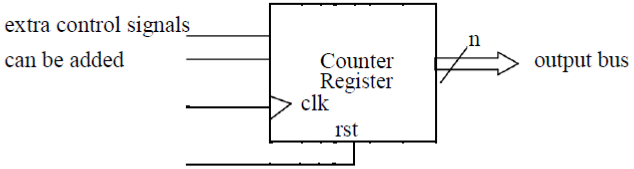
Summary of lecture 3

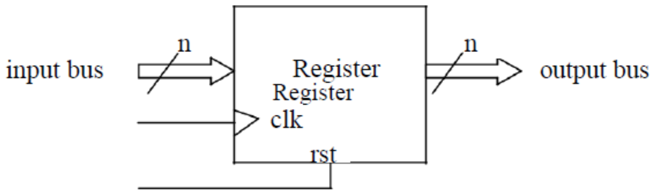
Signal and Variables

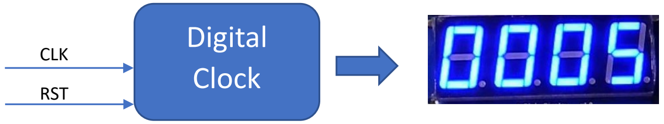






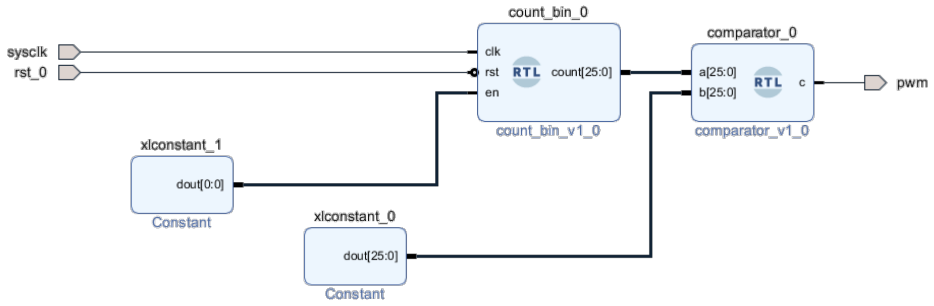


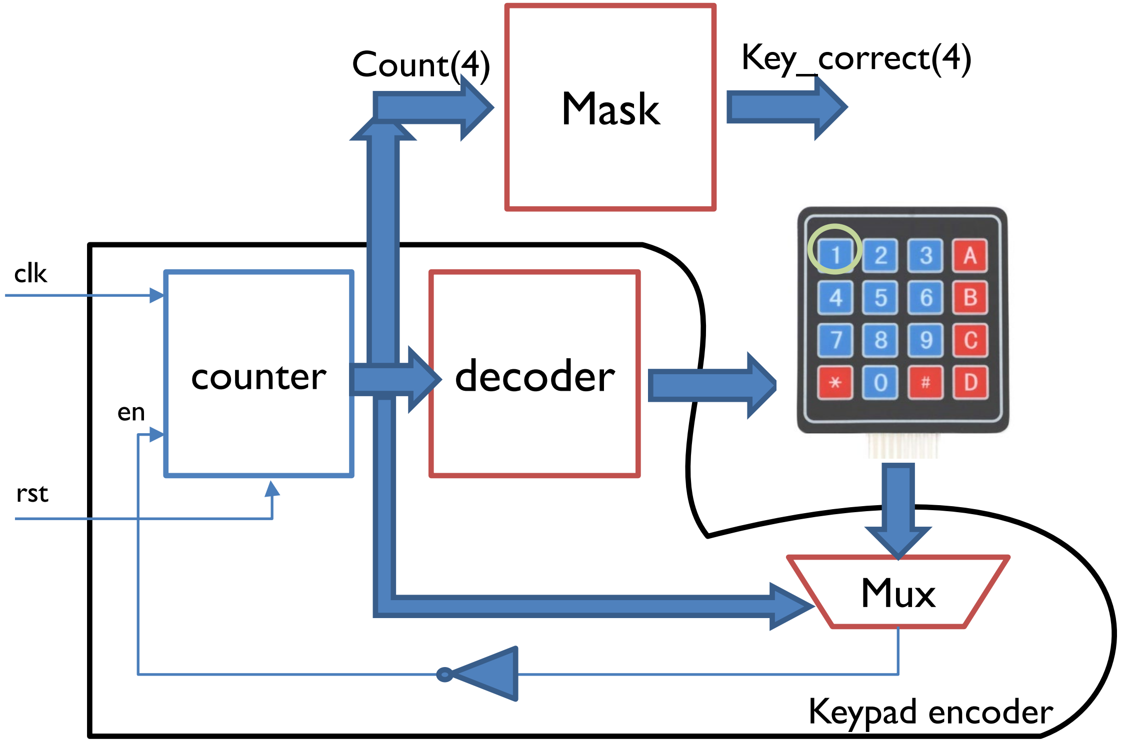




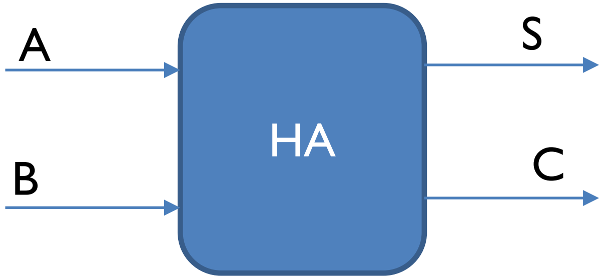
Summary of lecture 4

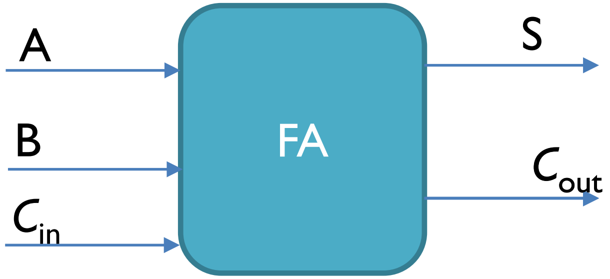
Operators	VHDL
Equality & Relational	= /= < <= > >=
Logical	not and or



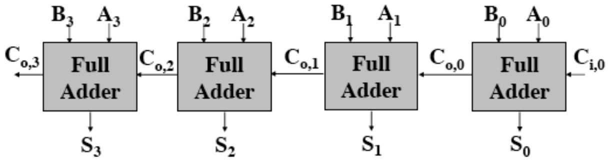


Summary of lecture 5

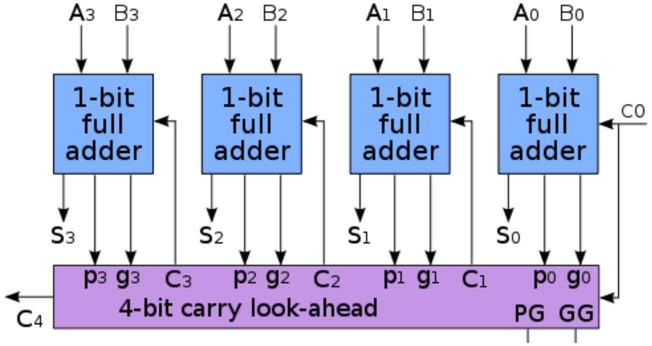




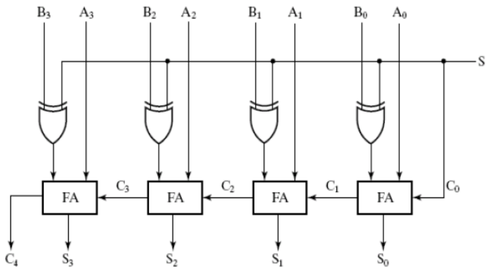
- **Ripple-carry adder**



- **Carry-look-ahead adder**

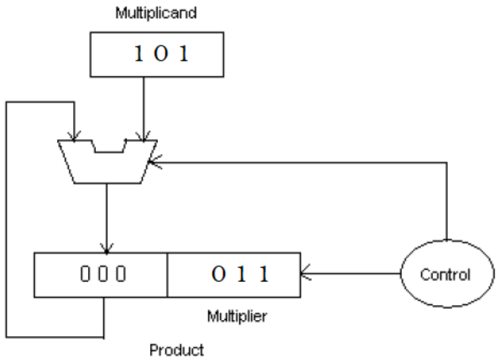


- Full Adder/Subtractors

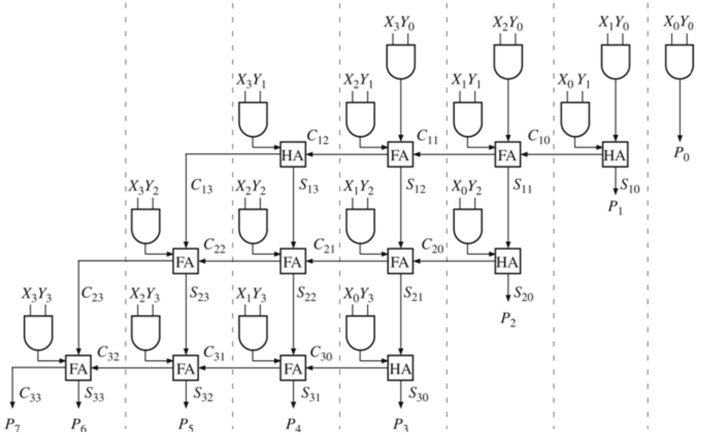


Summary of lecture 5

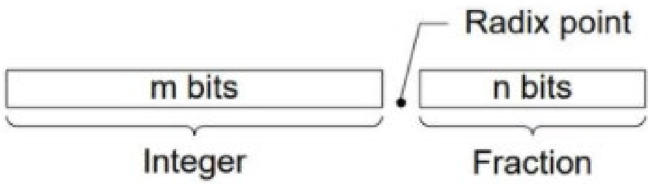
- Multiplier



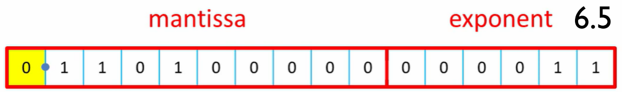
- Array Multiplier



- Dividers
  - Clk divider
  - Division by subtraction
  - Division by multiplication
- Fixed point

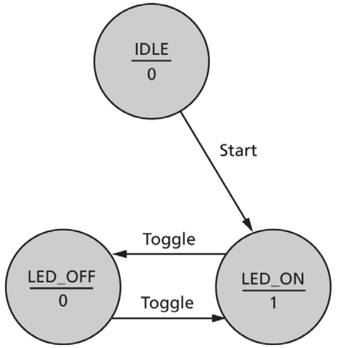


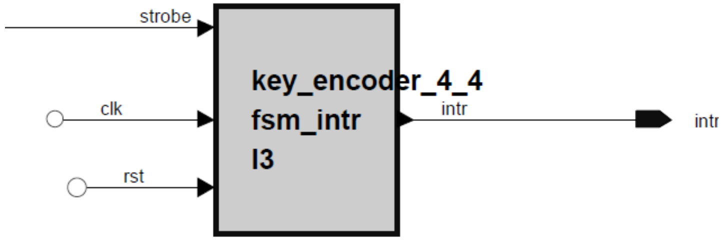
- Floating point

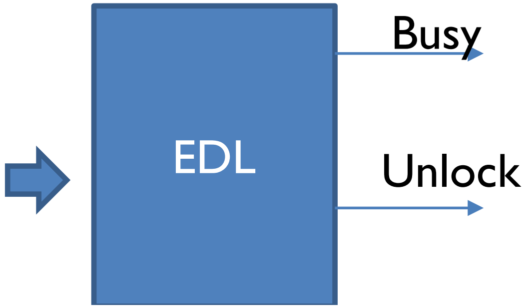


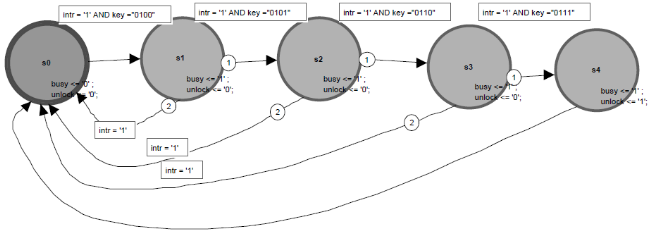
Summary of lecture 6

- Moore

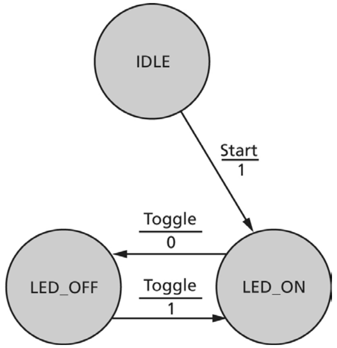


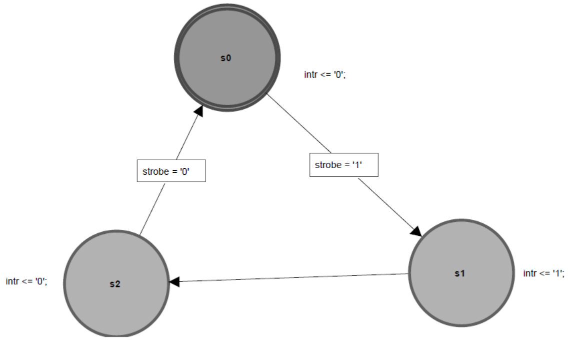


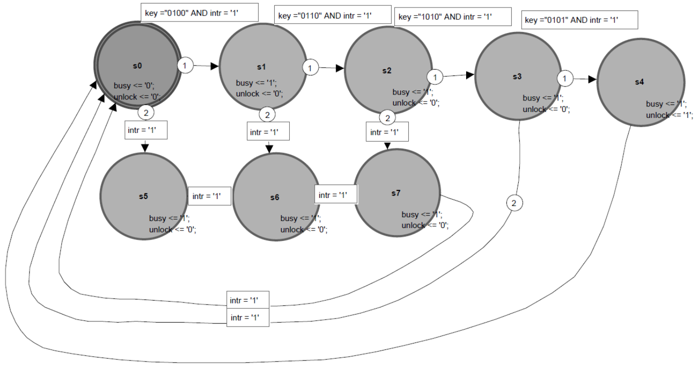




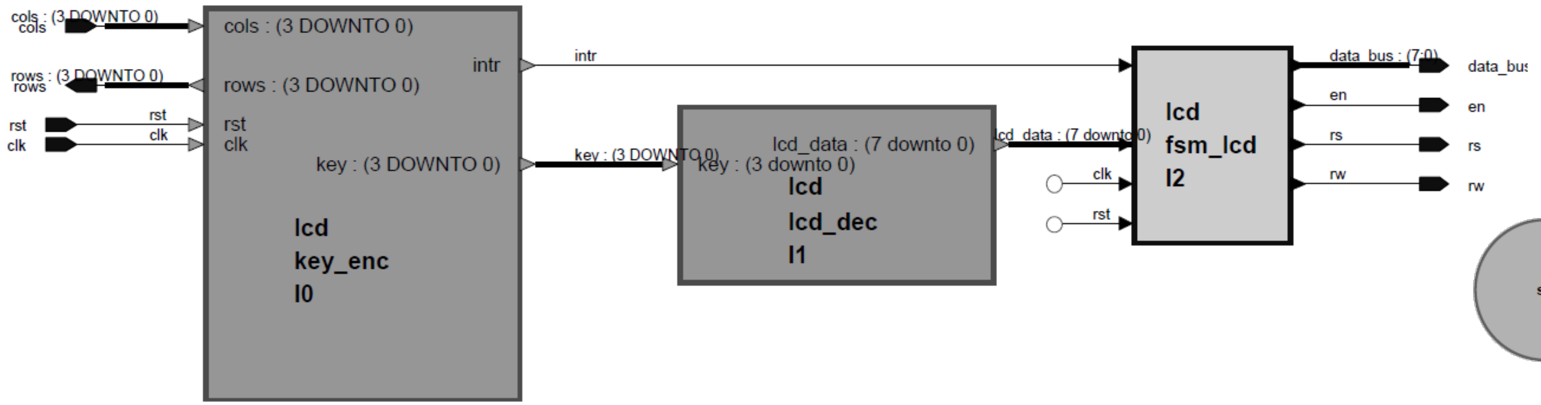
- Mealy

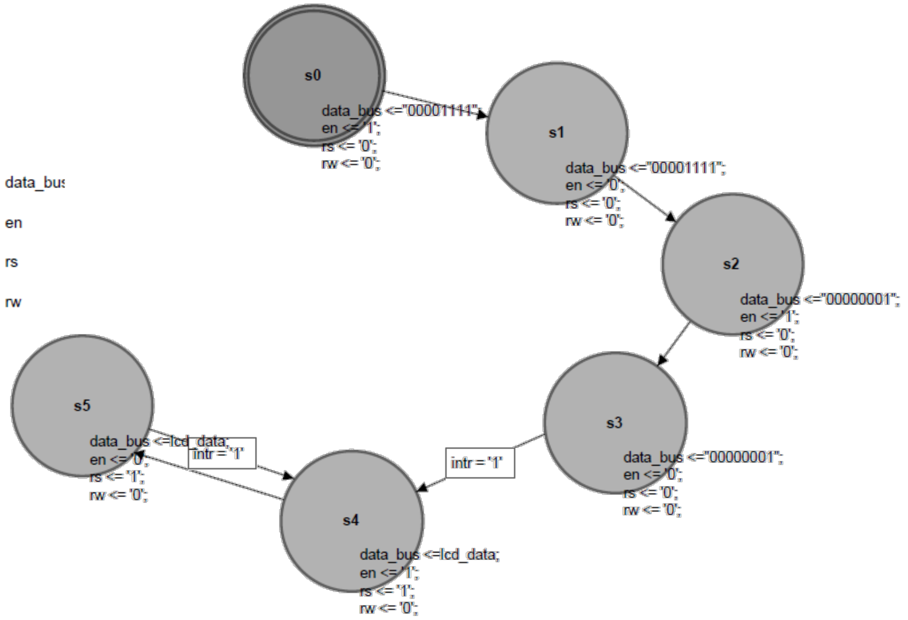




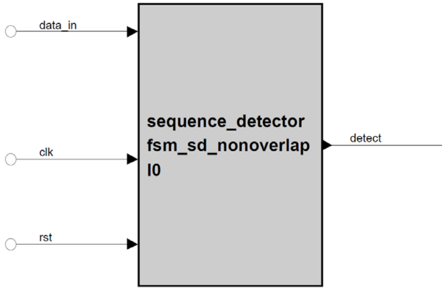


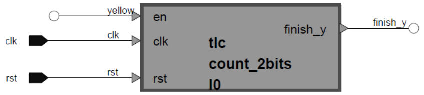
Summary of lecture 6

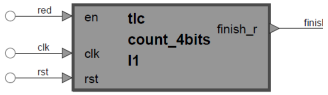


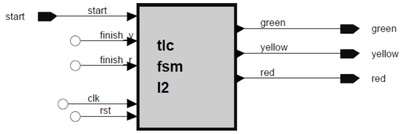


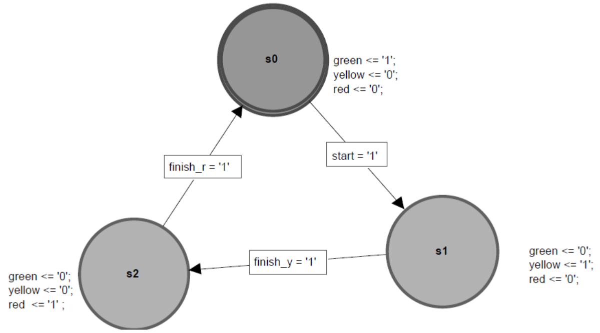
Summary of lecture 7

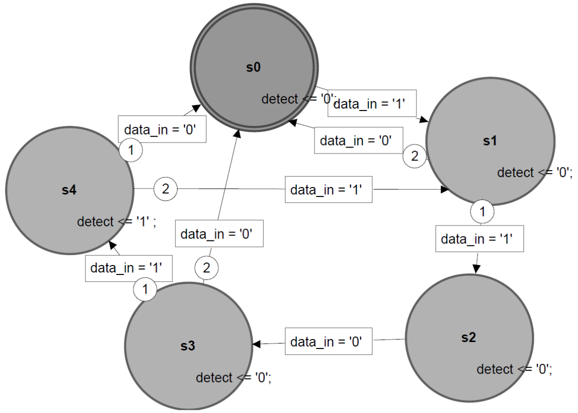


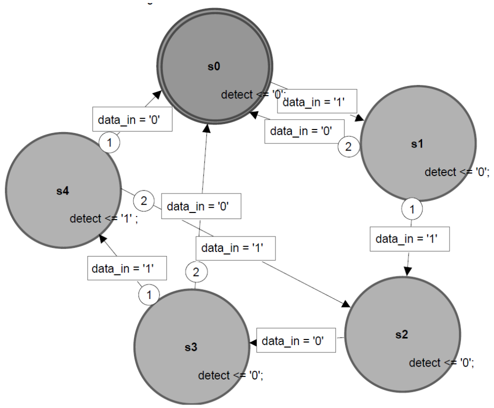


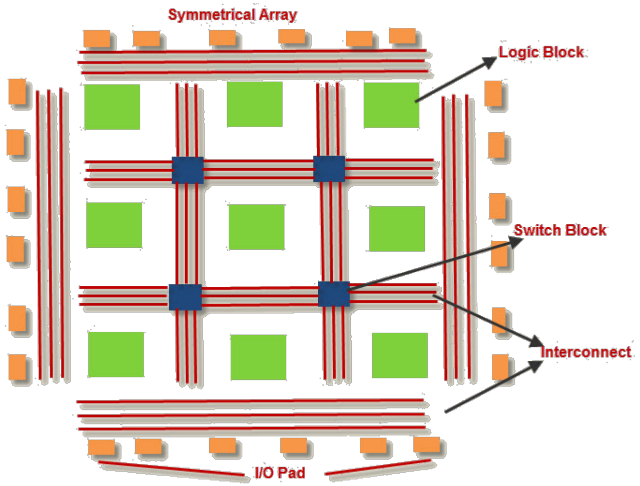






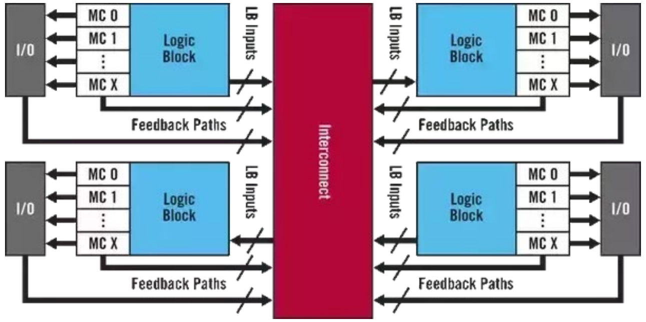


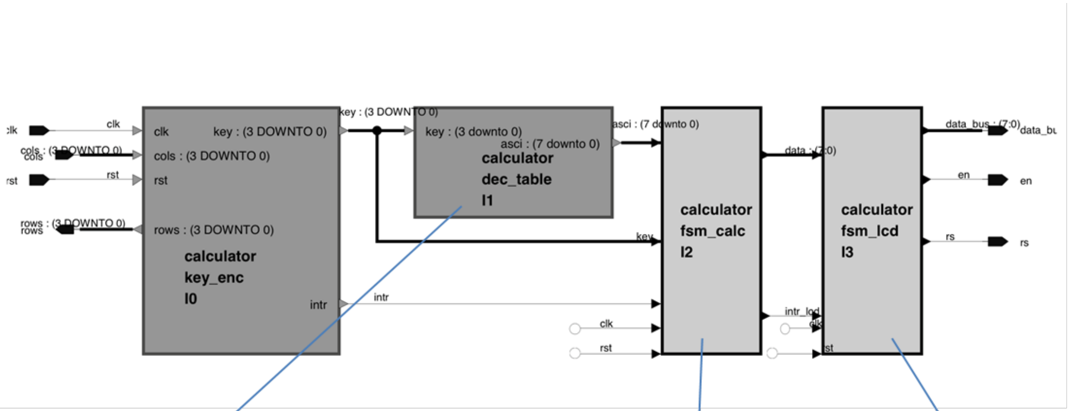




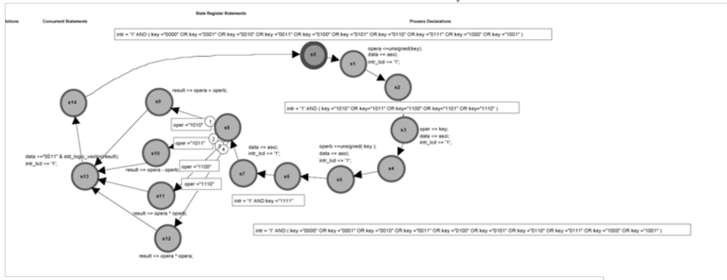
Summary of Lecture 8

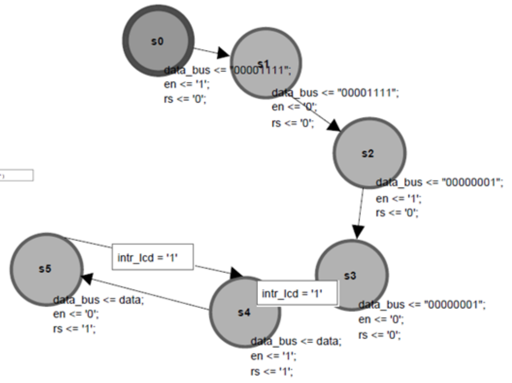
- CPLD



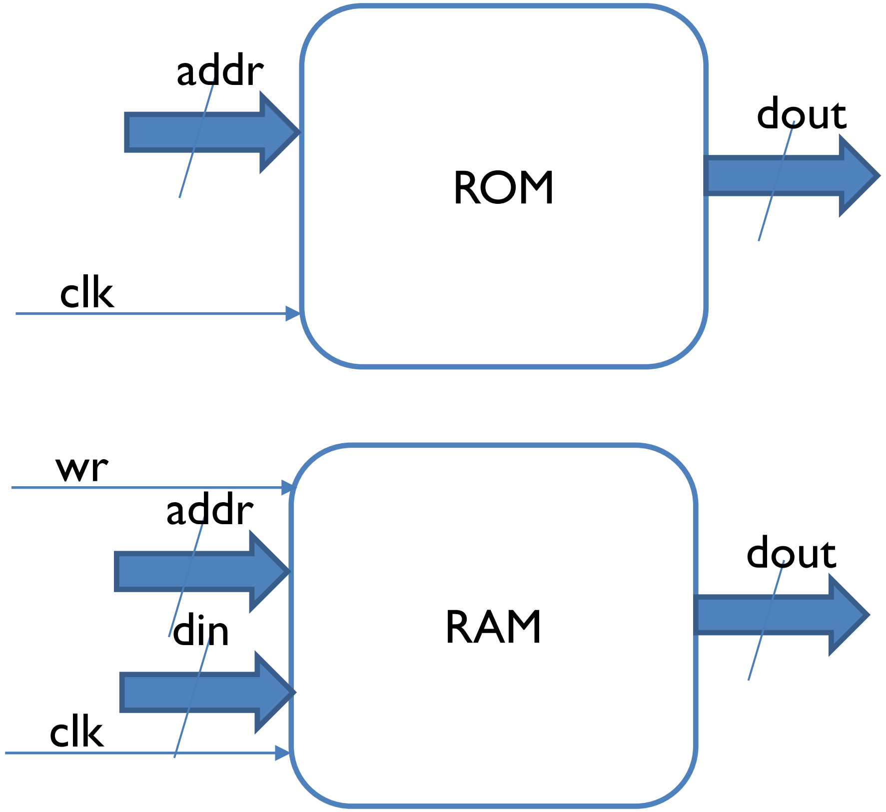


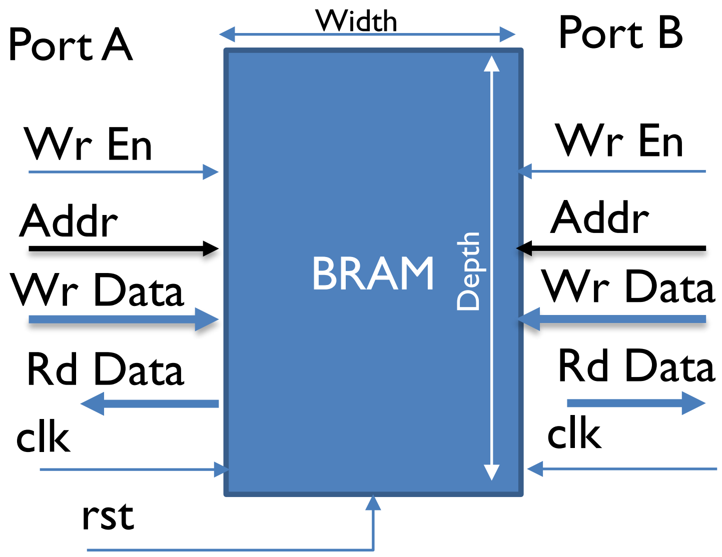

```
ENTITY dec_table IS
-- Declarations
   port(key: in std_logic_vector(3 downto 0);
        asci : out std_logic_vector(7 downto 0));
END dec_table ;

-- hds interface_end
ARCHITECTURE rtl OF dec_table IS
BEGIN
  process(key)
   begin
    if(key="0000")then asci<="00110000";
    elsif(key="0001")then asci<="00110001";--0
    elsif(key="0010")then asci<="00110010";
    elsif(key="0011")then asci<="00110011";
    elsif(key="0100")then asci<="00110100";
    elsif(key="0101")then asci<="00110101";
    elsif(key="0110")then asci<="00110110";
    elsif(key="0111")then asci<="00110111";
    elsif(key="1000")then asci<="00111000";
    elsif(key="1001")then asci<="00111001";--9
    elsif(key="1010")then asci<="00101011";--+
    elsif(key="1011")then asci<="00101101";-- -
    elsif(key="1100")then asci<="00101010";-- *
    elsif(key="1101")then asci<="00101111";--^2
    elsif(key="1110")then asci<="00101110";--.
    else asci<="00111101"; --=
   end if;
  end process;

END rtl;
```





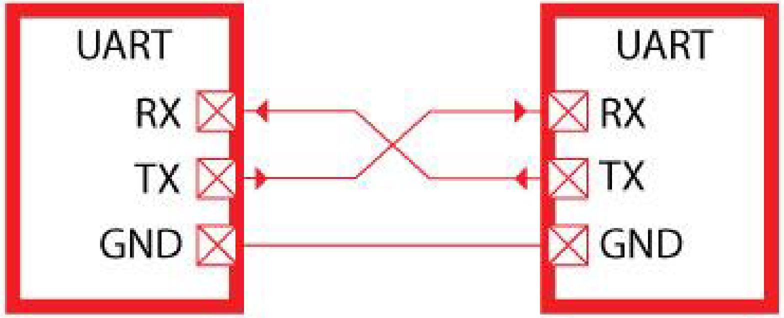
Summary of lecture 9



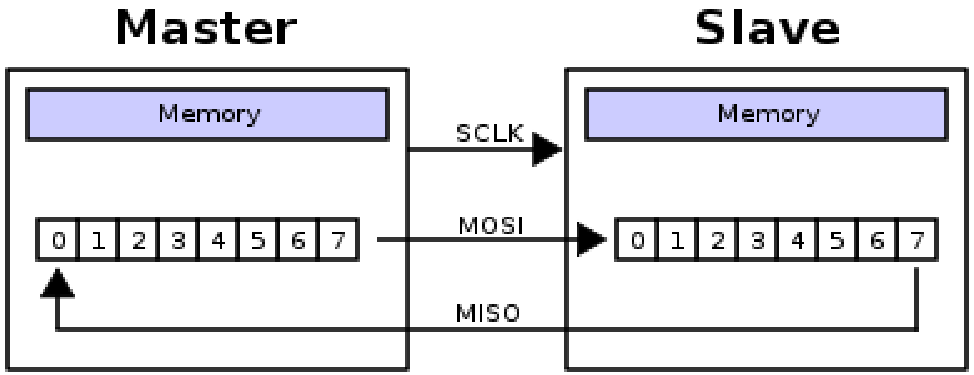


Summary of lecture 10

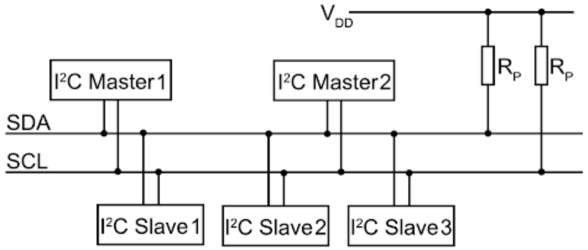
UART

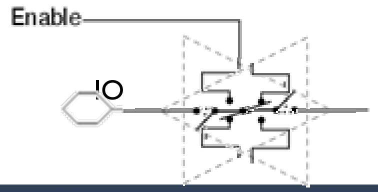


SPI



I2C

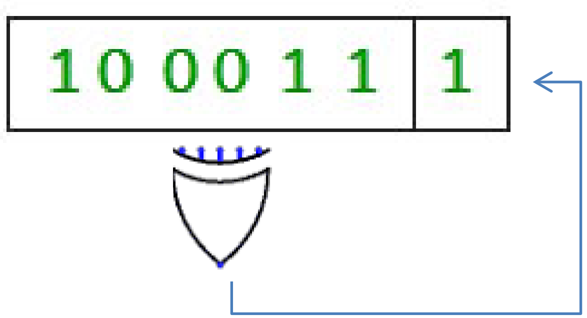




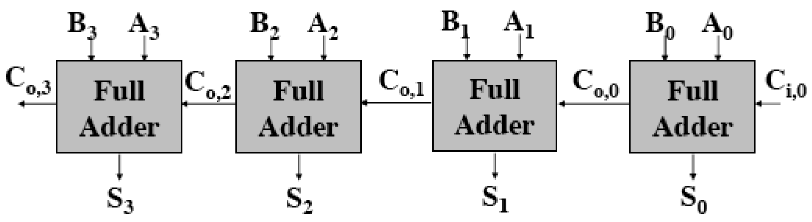
Summary of lecture 11

Error detection:

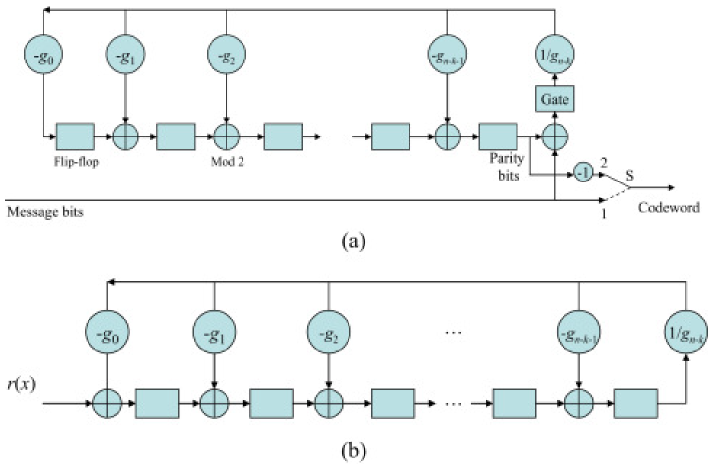
- Parity check



Checksum

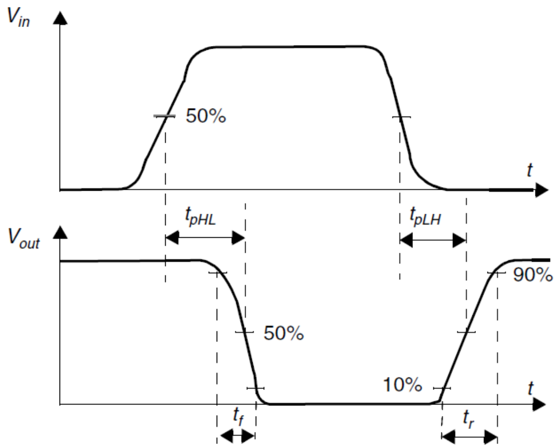


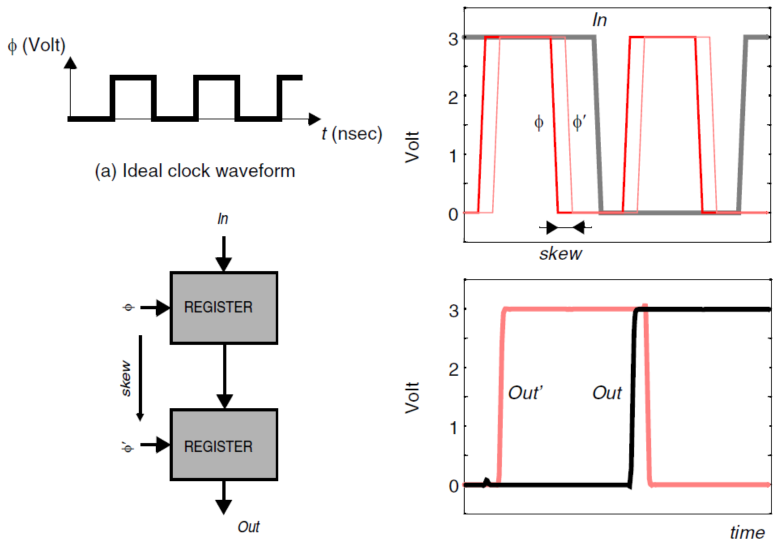
CRC



Summary of lecture 11

- Quality Metrics of a Digital Design
- Performance
- Propagation delay
- Metastable
- Clock Skew





(a) Ideal clock waveform
(b) Two cascaded registers
(c) Simulated waveforms