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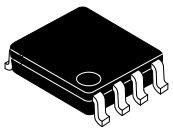
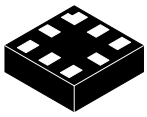
TinyLogic UHS D-Type, Flip-Flop with Preset and Clear

NC7SZ74



US8
CASE 846AN



UQFN8
1.6X1.6, 0.5P
CASE 523AY

Description

The NC7SZ74 is a single, D−type, CMOS flip−flop with preset and clear from **onsemi** ultra high−speed series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad V_{CC} operating range of 1.65 V to 5.5 V V_{CC}. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V_{CC} operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive−going transition of the CLK pulse.

Features

- Ultra−High Speed: t_{PD} 2.6 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High−Impedance Inputs/Outputs
- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry

CONNECTION DIAGRAM

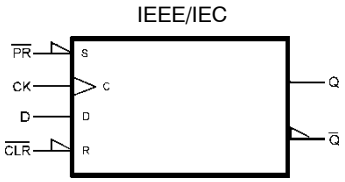
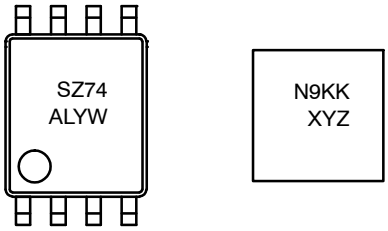


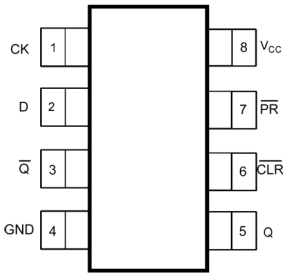
Figure 1. Logic Symbol

MARKING DIAGRAMS

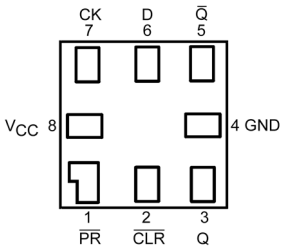


SZ74, N9	= Specific Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Wee
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code Format
Z	= Assembly Plant Code

PIN CONFIGURATIONS



USB (Top View)



MicroPak™ (Top Through View)

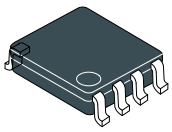
ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

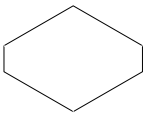
NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

TinyLogic UHS D型，带预置和清除功能的

NC7SZ74触发器



US8
案例 846AN



UQFN8
1.6X1.6, 0.5P
案例 523AY

描述

NC7SZ74是一种单D型CMOS触发器，具有来自onsemi超高速TinyLogic系列的预置和清除功能。该器件采用先进的CMOS技术制造，以实现超高速和高输出驱动，同时在1.65 V至5.5 V的广泛VCC工作范围内保持低静态功耗。当V_{CC}为0 V时，输入和输出为高阻抗。输入电压可承受高达5.5 V的电压，与V_{CC}工作电压无关。

施加到 D 输入的信号电平在 CLK 脉冲的正向过渡期间被传输到 Q 输出。

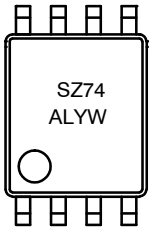
特点

- 超高速：t_{PD}2.6 ns（典型）在 5 V V_{CC} 下对 50 pF
- 高输出驱动：±24 mA 在 3 V V_{CC} 下
- 宽 V_{CC}工作范围：1.65 V 到 5.5 V
- 断电高阻抗输入/输出
- 过电压容忍输入便于 5 V 到 3 V 的转换
- 专有噪声/电磁干扰减少电路

连接图

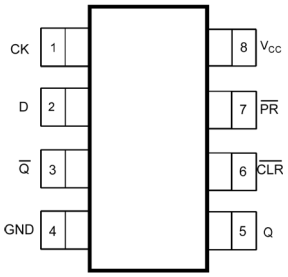
图 1. 逻辑符号

标记图

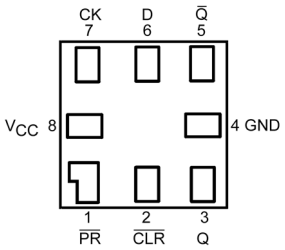


SZ74, N9 = 特定设备代码
A = 装配地点
L = 晶圆批号
YW = 装配开始周
KK = 2位数字批次追溯代码
XY = 2位数字日期代码格式
Z = 装配工厂代码

引脚配置



USB（顶部视图）



MicroPak™ （顶部透视图）

订购信息

请参阅本数据表第 6 页的详细订购和运输信息。

注意：本数据表中的某些设备已停产。请参阅第6页的表格。

PIN DEFINITIONS

Pin # US8	Pin # MicroPak	Name	Description
1	7	CK	Clock Pulse Input
2	6	D	Data Input
3	5	$\overline{Q}$	Flip−Flop Output
4	4	GND	Ground
5	3	Q	Flip−Flop Output
6	2	$\overline{CLR}$	Direct Clear Input
7	1	$\overline{PR}$	Direct Preset Input
8	8	VCC	Supply Voltage

FUNCTION TABLE

Inputs				Output		
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	Function
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

H = HIGH Logic Level Qn = No change in data X = Immaterial ↓= Falling Edge

L = LOW Logic Level Z = High Impedance ↑ = Rising Edge

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
I_{OUT}	DC Output Source/Sink Current		−	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		−	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		−	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
P_D	Power Dissipation in Still Air	US8 MicroPak−8	− −	500 539	mW
ESD	Human Body Model: JEDEC:JESD22−A114		−	4000	V
	Charge Device Model: JEDEC:JESD22−C101		−	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

引脚定义

引脚 # US8	引脚 # MicroPak	名称	描述
1	7	CK	时钟脉冲输入
2	6	D	数据输入
3	5	$\overline{Q}$	翻转−翻转输出
4	4	GND	接地
5	3	Q	翻转−翻转输出
6	2	$\overline{CLR}$	直接清除输入
7	1	$\overline{PR}$	直接预设输入
8	8	V_{CC}	供电电压

功能表

输入				输出		
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	功能
L	高	无	无	L	高	清除
高	L	无	无	高	L	预设
L	L	无	无	高	高	
高	高	L	↑	L	高	
高	高	高	↑	高	L	
高	高	无	↓	Q_n	$\overline{Q}_n$	无变化

H = 高逻辑电平　　Qn = 数据无变化　　X = 无关　　↓= 下降沿

L = 低逻辑电平　　Z = 高阻抗　　↑ = 上升沿

绝对最大额定值

符号	参数		最小值	最大值	单位
V_{CC}	供电电压		−0.5	6.5	伏特
$V_{输入}$	直流输入电压		−0.5	6.5	伏特
$V_{输出}$	直流输出电压		−0.5	6.5	伏特
I_{IK}	直流输入二极管电流	V输入< 0 V	−	−50	毫安
I_{OK}	直流输出二极管电流	V_{OUT} < 0 V	−	−50	毫安
我输出	直流输出源/吸收电流		−	±50	毫安
I_{CC} 或 IGND	直流 V_{CC} 或接地电流		−	±50	毫安
T_{STG}	存储温度范围		−65	+150	°C
T_J	偏置下的结温		−	+150	°C
T_L	焊接时的结引脚温度（10秒）		−	+260	°C
P_D	静止空气中的功耗	US8 MicroPak−8	− −	500 539	毫瓦
静电放电	人体模型：JEDEC:JESD22 −A114		−	4000	伏特
	充电设备模型：JEDEC:JESD22 −C101		−	2000	

超过最大额定值表中列出的应力可能会损坏设备。如果超过这些限制，则不应假定设备功能，可能会发生损坏并影响可靠性。

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active State	0	V_{CC}	V
		3−State	0	5.5	
t_r, t_f	Input Rise and Fall Times	V_{CC} = 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} = 3.3 V ±0.3 V	0	10	
		V_{CC} = 5.0 V ±0.5 V	0	5	
T_A	Operating Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	US8		250	°C/W
		MicroPak−8		232	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Vcc	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Control Input Voltage	1.65 to 1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.30 to 5.50		0.70 V_{CC}			0.70 V_{CC}		
V_{IL}	LOW Level Control Input Voltage	1.65 to 1.95				0.35 V_{CC}		0.35 V_{CC}	V
		2.30 to 5.50				0.30 V_{CC}		0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH}, I_{OH} = −100 μA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH} = −4 mA	1.29	1.52		1.29		
		2.30	I_{OH} = −8 mA	1.90	2.15		1.90		
		3.00	I_{OH} = −16 mA	2.40	2.80		2.40		
		3.00	I_{OH} = −24 mA	2.30	2.68		2.30		
		4.50	I_{OH} = −32 mA	3.80	4.20		3.80		
V_{OL}	LOW Level Control Output Voltage	1.65	V_{IN} = V_{IH}, I_{OL} = 100 μA			0.10		0.10	V
		2.30				0.10		0.10	
		3.00				0.10		0.10	
		4.50				0.10		0.10	
		1.65	I_{OL} = 4 mA		0.10	0.24		0.24	
		2.30	I_{OL} = 8 mA		0.10	0.30		0.30	
		3.00	I_{OL} = 16 mA		0.15	0.40		0.40	
		3.00	I_{OL} = 24 mA		0.22	0.55		0.55	
		4.50	I_{OL} = 32 mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	0 ≤ V_{IN} ≤ 5.5 V			±0.1		±1.0	μA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT} = 5.5 V			1		10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN} = 5.5 V, GND			1		10	μA

推荐操作条件

符号	参数	条件	最小值	最大值	单位
V_{CC}	供电电压操作		1.65	5.50	伏特
	供电电压数据保持		1.50	5.50	
$V_{输入}$	输入电压		0	5.5	伏特
$V_{输出}$	输出电压	活动状态	0	V_{CC}	伏特
		三态	0	5.5	
t_r, t_f	输入上升和下降时间	V_{CC} = 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} = 3.3 V ±0.3 V	0	10	
		V_{CC} = 5.0 V ±0.5 V	0	5	
T_A	工作温度		−40	+85	°C
θ_{JA}	热阻	US8		250	°C/W
		MicroPak−8		232	

在推荐工作范围内列出的应力下的功能操作并不意味着被暗示。长时间暴露于超出推荐工作范围限制的应力可能会影响设备的可靠性。

注意：未使用的输入必须保持在高电平或低电平。它们不能悬空。

直流电气特性

符号	参数	Vcc	条件	T_A = +25°C			T_A = −40 到 +85°C		单位
				最小值	典型值	最大值	最小值	最大值	
V_{IH}	高电平控制输入电压	1.65 到 1.95		0.65 V_{CC}			0.65 V_{CC}		伏特
		2.30 到 5.50		0.70 V_{CC}			0.70 V_{CC}		
V_{IL}	低电平控制输入电压	1.65 到 1.95				0.35 V_{CC}		0.35 V_{CC}	伏特
		2.30 到 5.50				0.30 V_{CC}		0.30 V_{CC}	
V_{OH}	高电平输出电压	1.65	V_{IN} = V_{IH}, I_{OH} = −100 μA	1.55	1.65		1.55		伏特
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH} = −4 mA	1.29	1.52		1.29		
		2.30	I_{OH} = −8 mA	1.90	2.15		1.90		
		3.00	I_{OH} = −16 mA	2.40	2.80		2.40		
		3.00	I_{OH} = −24 mA	2.30	2.68		2.30		
		4.50	I_{OH} = −32 mA	3.80	4.20		3.80		
V_{OL}	低电平控制输出电压	1.65	V_{IN} = V_{IH}, I_{OL} = 100 μA			0.10		0.10	伏特
		2.30				0.10		0.10	
		3.00				0.10		0.10	
		4.50				0.10		0.10	
		1.65	I_{OL} = 4 mA		0.10	0.24		0.24	
		2.30	I_{OL} = 8 mA		0.10	0.30		0.30	
		3.00	I_{OL} = 16 mA		0.15	0.40		0.40	
		3.00	I_{OL} = 24 mA		0.22	0.55		0.55	
		4.50	I_{OL} = 32 mA		0.22	0.55		0.55	
I_{IN}	输入泄漏电流	1.65 到 5.5	0 ≤ V_{IN} ≤ 5.5 V			±0.1		±1.0	μA
I_{OFF}	关机泄漏电流	0	V_{IN} 或 V_{OUT}= 5.5 V			1		10	μA
I_{CC}	静态供电电流	1.65 到 5.50	V_{IN} = 5.5 V, GND			1		10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units	Figure
				Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	1.80 ±0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	75			75		MHz	Figure 4 Figure 8
		2.50 ±0.20		150			150			
		3.30 ±0.30		200			200			
		5.00 ±0.50		250			250			
		3.30 ±0.50	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	175			175			
		5.00 ±0.50		200			200			
t_{PLH}, t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	1.80 ±0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open		6.5	12.5		13.0	ns	Figure 4 Figure 6
		2.50 ±0.20			3.8	7.5		8.0		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	4.5		5.0		
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t_{PLH}, t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$ to Q, $\overline{Q}$	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open		6.5	14.0		14.5	ns	Figure 4 Figure 6
		2.50 ±0.20			3.8	9.0		9.5		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	5.0		5.5		
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t_S	Setup Time CK to D	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	6.5			6.5		ns	Figure 4 Figure 7
		2.50 ±0.20		3.5			3.5			
		3.30 ±0.30		2.0			2.0			
		5.00 ±0.50		1.5			1.5			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	2.0			2.0			
		5.00 ±0.50		1.5			1.5			
t_H	Hold Time, CK to D	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	0.5			0.5		ns	Figure 4 Figure 7
		2.50 ±0.20		0.5			0.5			
		3.30 ±0.30		0.5			0.5			
		5.00 ±0.50		0.5			0.5			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	0.5			0.5			
		5.00 ±0.50		0.5			0.5			
t_W	Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	6.0			6.0		ns	Figure 4 Figure 8
		2.50 ±0.20		4.0			4.0			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		2.0			2.0			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	3.0			3.0			
		5.00 ±0.50		2.0			2.0			
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	8.0			8.0		ns	Figure 7
		2.50 ±0.20		4.5			4.5			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		3.0			3.0			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	3.0			3.0			
		5.00 ±0.50		3.0			3.0			

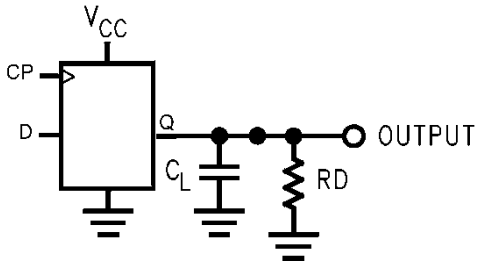
交流电气特性

符号	参数	V_{CC}	条件	T_A = +25°C			T_A = −40 到 +85°C		单位	图
				最小值	典型值	最大值	最小值	最大值		
$f_{最大值}$	最大时钟频率	1.80 ±0.15	C_L = 15 pF, R_D = 1 M Ω, S_1 = 开放	75			75		MHz	图 4 图 8
		2.50 ±0.20		150			150			
		3.30 ±0.30		200			200			
		5.00 ±0.50		250			250			
		3.30 ±0.50	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放	175			175			
		5.00 ±0.50		200			200			
t_{PLH}, t_{PHL}	传播延迟 CK 到 Q, $\overline{Q}$	1.80 ±0.15	C_L = 15 pF, R_D = 1 M Ω, S_1 = 开放		6.5	12.5		13.0	ns	图 4 图 6
		2.50 ±0.20			3.8	7.5		8.0		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	4.5		5.0		
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t_{PLH}, t_{PHL}	传播延迟 $\overline{CLR}$, $\overline{PR}$ 到 Q, $\overline{Q}$	1.80 ±0.15	C_L = 15 pF, R_L = 1 M Ω, S_1 = 开放		6.5	14.0		14.5	ns	图 4 图 6
		2.50 ±0.20			3.8	9.0		9.5		
		3.30 ±0.30			2.8	6.5		7.0		
		5.00 ±0.50			2.2	5.0		5.5		
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放		3.4	7.0		7.5		
		5.00 ±0.50			2.6	5.0		5.5		
t_S	设置时间 CK 到 D	1.80 ±0.15	C_L = 15 pF, R_L = 1 M Ω, S_1 = 开放	6.5			6.5		ns	图 4 图 7
		2.50 ±0.20		3.5			3.5			
		3.30 ±0.30		2.0			2.0			
		5.00 ±0.50		1.5			1.5			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放	2.0			2.0			
		5.00 ±0.50		1.5			1.5			
t_H	保持时间，CK到D	1.80 ±0.15	C_L = 15 pF, R_L = 1 M Ω, S_1 = 开放	0.5			0.5		ns	图 4 图 7
		2.50 ±0.20		0.5			0.5			
		3.30 ±0.30		0.5			0.5			
		5.00 ±0.50		0.5			0.5			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放	0.5			0.5			
		5.00 ±0.50		0.5			0.5			
t_W	脉冲宽度，CK, $\overline{PR}$, $\overline{CLR}$	1.80 ±0.15	C_L = 15 pF, R_L = 1 M Ω, S_1 = 开放	6.0			6.0		ns	图 4 图 8
		2.50 ±0.20		4.0			4.0			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		2.0			2.0			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放	3.0			3.0			
		5.00 ±0.50		2.0			2.0			
t_{REC}	恢复时间 CLR, $\overline{PR}$到CK	1.80 ±0.15	C_L = 15 pF, R_L = 1 M Ω, S_1 = 开放	8.0			8.0		ns	图 7
		2.50 ±0.20		4.5			4.5			
		3.30 ±0.30		3.0			3.0			
		5.00 ±0.50		3.0			3.0			
		3.30 ±0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = 开放	3.0			3.0			
		5.00 ±0.50		3.0			3.0			

AC ELECTRICAL CHARACTERISTICS (continued)

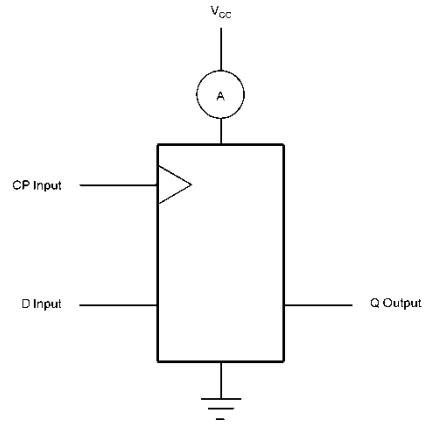
Symbol	Parameter	V_{CC}	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units	Figure
				Min	Typ	Max	Min	Max		
C_{IN}	Input Capacitance	0			3				pF	
C_{OUT}	Output Capacitance	0			4				pF	
C_{PD}	Power Dissipation Capacitance (Note 1)	3.30			10				pF	
		5.00			12					

1. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.



2. C_L includes load and stray capacitance. Input PRR = 1.0 MHz t_w = 500 ns.

Figure 2. AC Test Circuit



3. CP input = AC Waveforms $t_r = t_f$ = 2.5 ns.
4. CP input PRR = 10 MHz; Duty Cycle = 50%.
5. D input PRR = 5 MHz; Duty Cycle = 50%.

Figure 3. AC Test Circuit

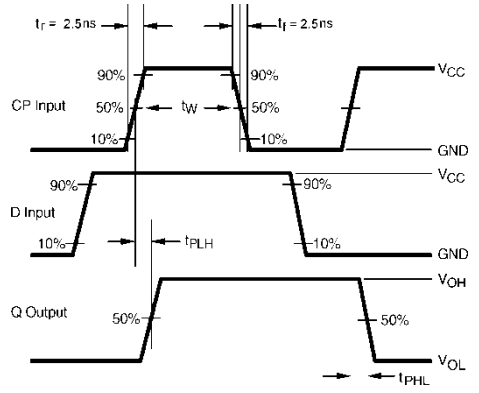


Figure 4. AC Waveforms

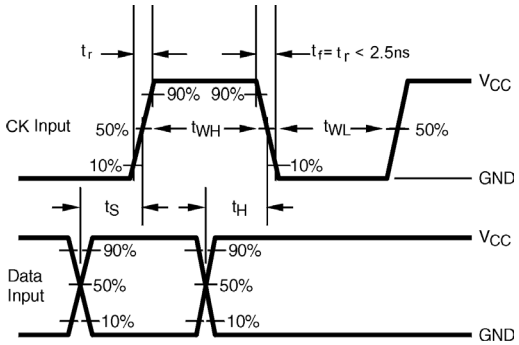


Figure 5. AC Waveforms

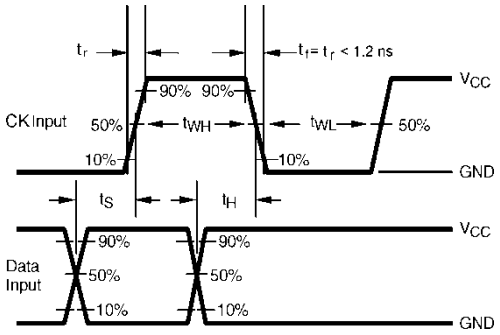


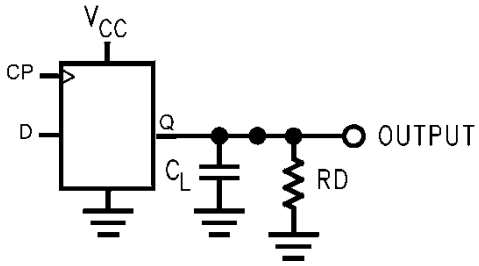
Figure 6. AC Waveforms

交流电气特性（续）

符号	参数	V_{CC}	条件	T_A = +25°C			T_A = −40 到 +85°C		单位	图
				最小值	典型值	最大值	最小值	最大值		
C_{IN}	输入电容	0			3				皮法	
C_{OUT}	输出电容	0			4				皮法	
C_{PD}	功耗 电容（注1）	3.30			10				皮法	
		5.00			12					

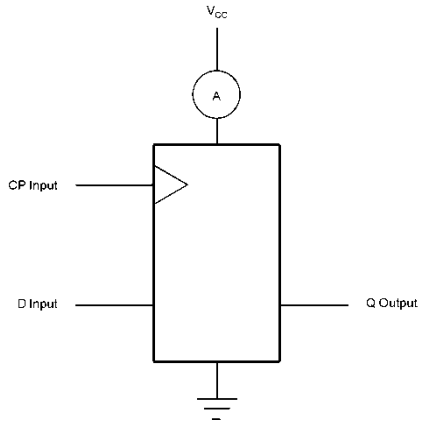
1.C_{PD}定义为从动态工作电流消耗（I_{CCD}）在无输出负载和以50%占空比工作时得出的内部等效电容值。C_{PD}与I_{CCD}dynamic工作电流的关系由以下表达式给出：

I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}静态)。



2. C_L 包括负载和杂散电容。
输入 PRR = 1.0 MHz t_W= 500 ns。

图2. 交流测试电路



3.CP 输入 = AC 波形 t_r = t_f = 2.5 ns。
4. CP 输入 PRR = 10 MHz；占空比 = 50%。
5. D 输入 PRR = 5 MHz；占空比 = 50%。

图 3. AC 测试电路

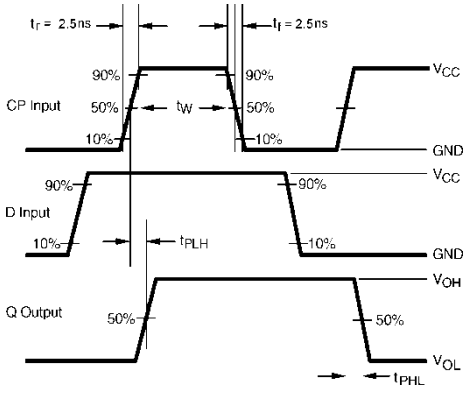


图 4. AC 波形

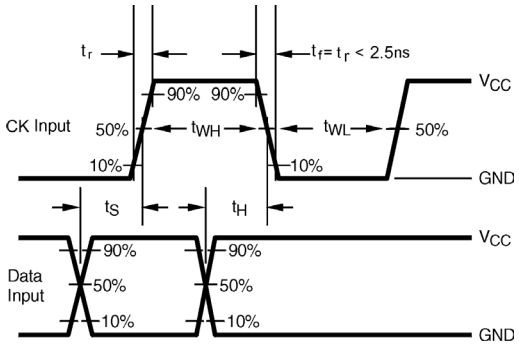


图 5. AC 波形

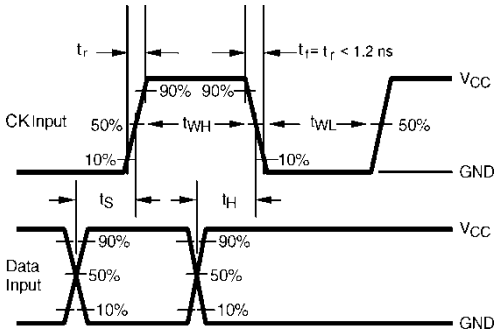


图 6. AC 波形

ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method†
NC7SZ74K8X	SZ74	8−Lead US8, JEDEC MO−187, Variation CA 3.1mm Wide	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8−Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

DISCONTINUED (Note 6)

NC7SZ74K8X−L22236	SZ74	8−Lead US8, JEDEC MO−187, Variation CA 3.1mm Wide	3000 Units on Tape & Reel
NC7SZ74L8X−L22185	N9	8−Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

订购信息

部件编号	顶部标记	封装	包装方式†
NC7SZ74K8X	SZ74	8 引脚 US8，JEDEC MO−187，变体 CA 3.1mm 宽	3000 单位在带和卷上
NC7SZ74L8X	N9	8−引脚MicroPak，宽1.6毫米	5000个单位在卷带和卷轴上

已停产（注6）

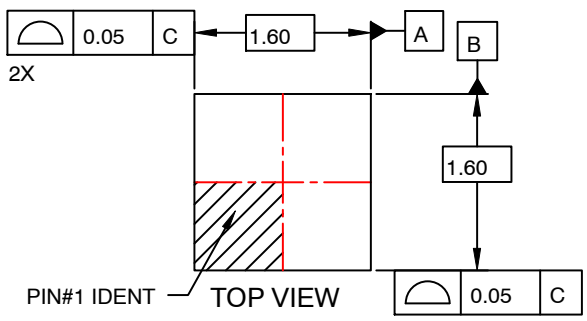
NC7SZ74K8X−L22236	SZ74	8 引脚 US8，JEDEC MO−187，变体 CA 3.1mm 宽	3000 单位在带和卷上
NC7SZ74L8X−L22185	N9	8−引脚MicroPak，宽1.6毫米	5000个单位在卷带和卷轴上

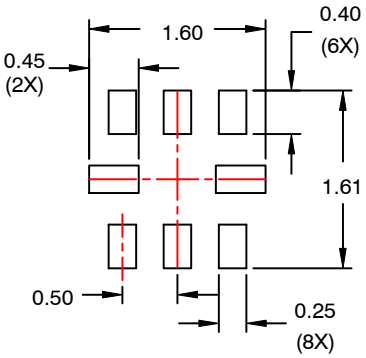
†有关卷带和卷轴规格的信息，包括零件方向和卷带尺寸，请参阅我们的卷带和卷轴包装规格手册，BRD8011/D

6.**已停产：**这些设备不推荐用于新设计。请联系您的 **onsemi**representative以获取信息。关于这些设备的最新信息可能在www.onsemi.com上可用。

UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016





RECOMMENDED
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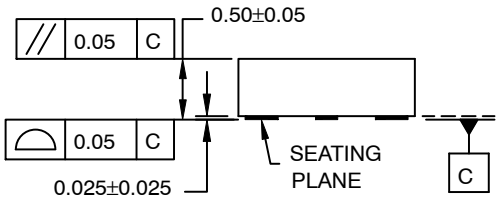


SIDE VIEW

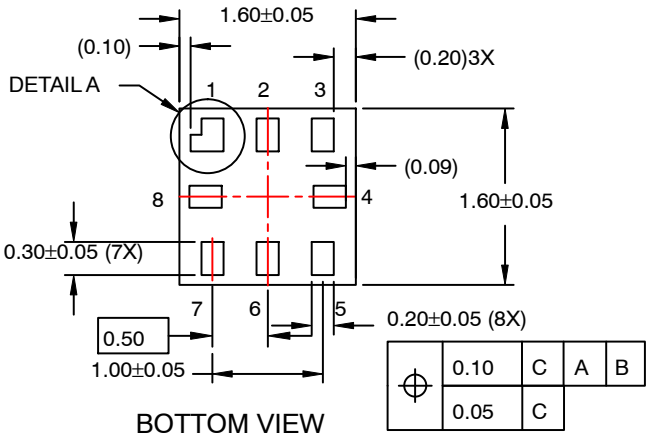
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

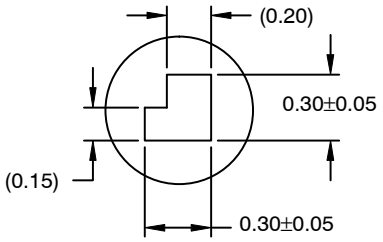
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



DETAIL A
SCALE : 2X

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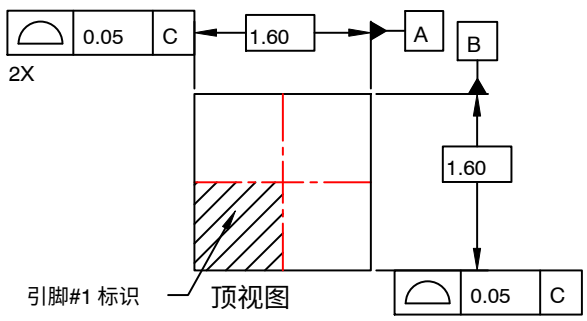
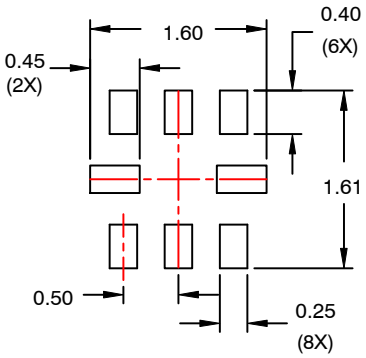
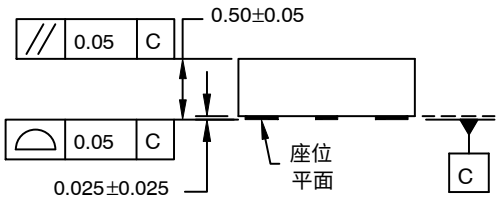
UQFN8 1.6X1.6, 0.5P
外壳 523AY
问题 O

日期 2016年8月31日





推荐
土地图案



侧视图

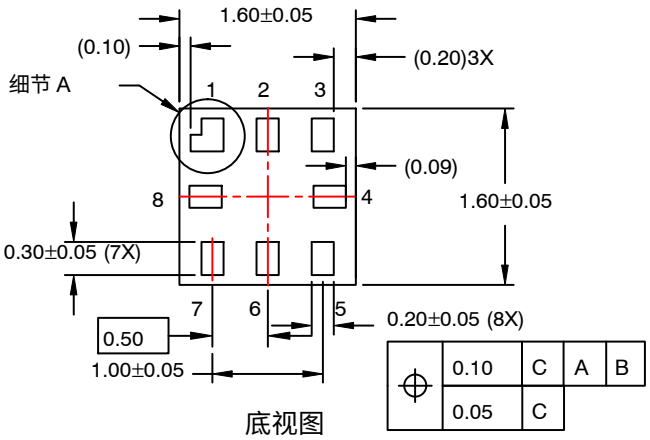
备注：

A.封装符合JEDEC MO−255
变体UAAD。

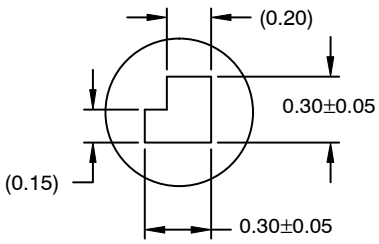
B.尺寸以毫米为单位。

C. 尺寸和公差按
ASME Y14.5M, 2009。

D.土地图案推荐为
现有行业土地图案。



底视图



细节 A
比例 : 2X

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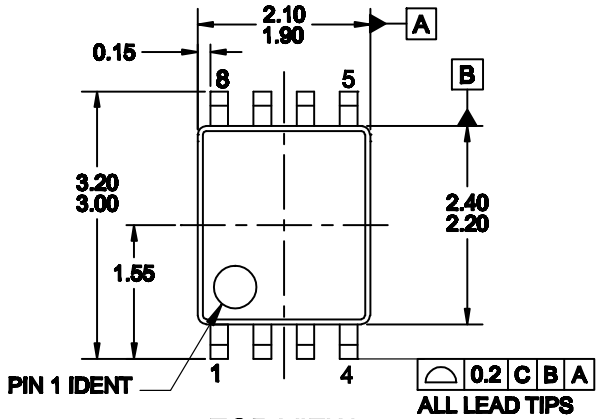
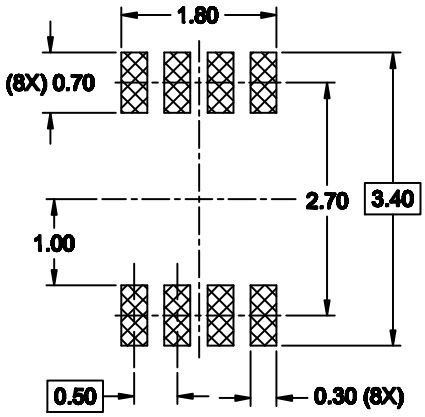
US8
CASE 846AN
ISSUE O

DATE 31 DEC 2016



TOP VIEW



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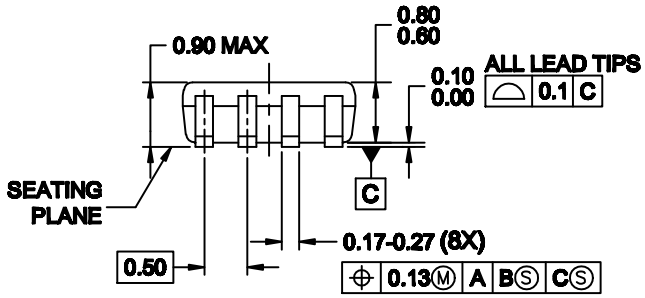


SIDE VIEW

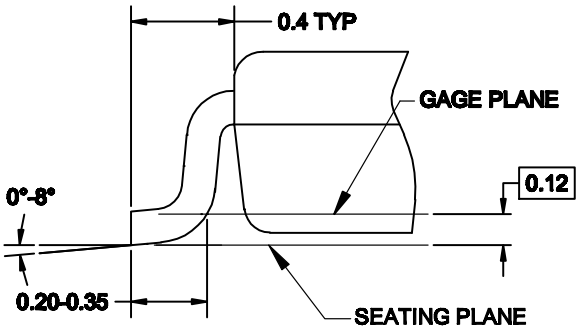
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187

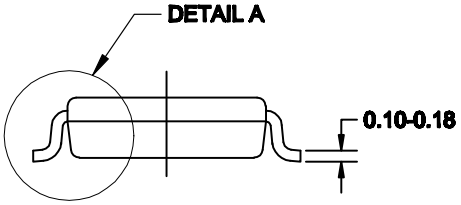
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



DETAIL A



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案例 846AN
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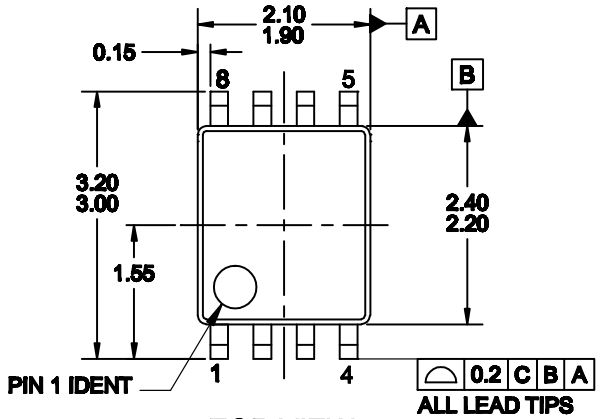
日期 2016 年 12 月 31 日



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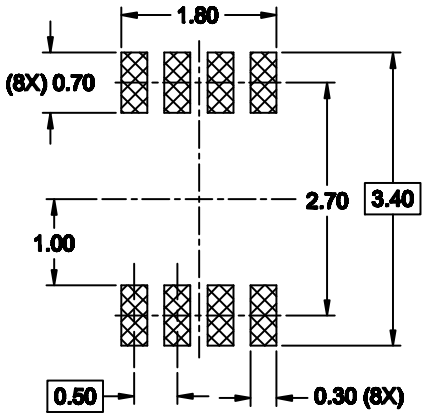

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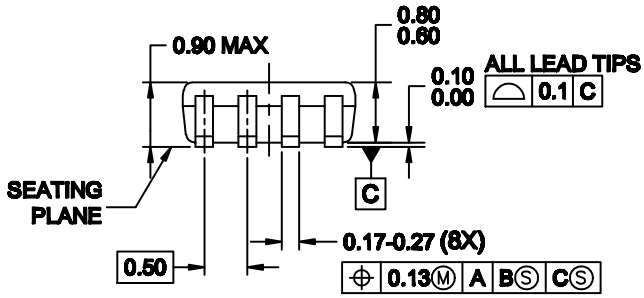


SIDE VIEW

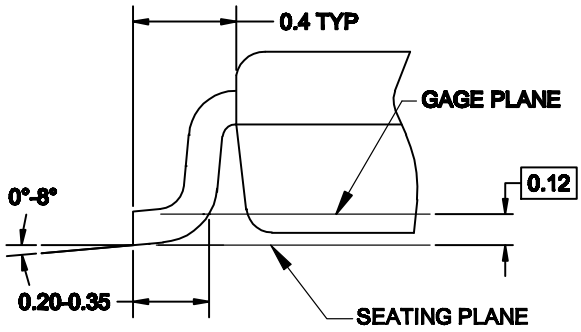
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187

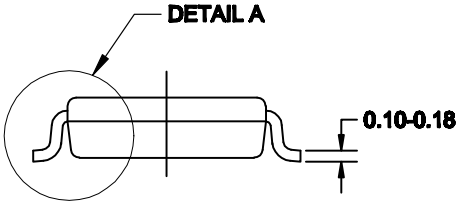
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



DETAIL A



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