Digital Signal Processing with Field Programmable Gate Arrays

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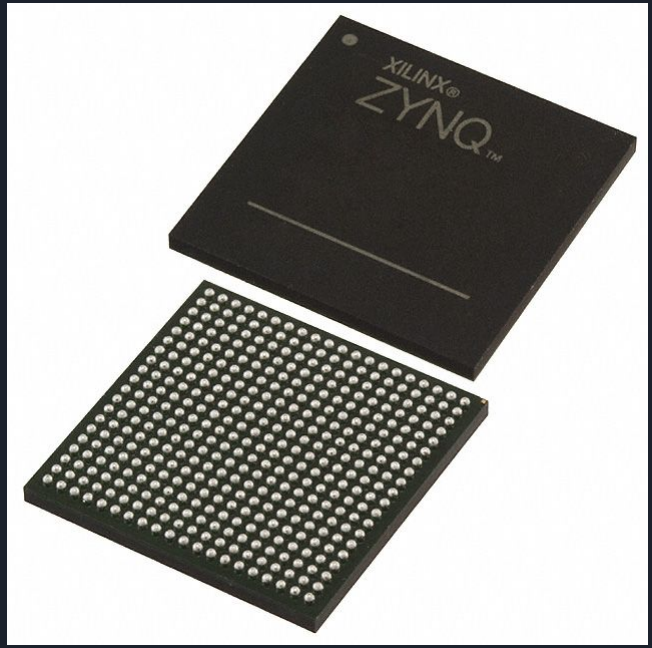
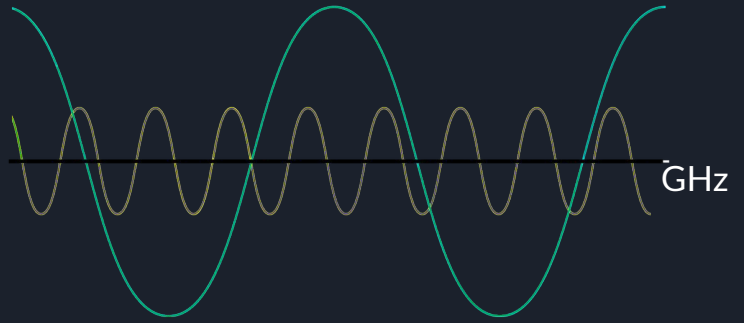
What is an FPGA?

(Field Programmable Gate Array)

- Array of configurable logic blocks
- Programmable with VHDL, Verilog
- Programmed to implement custom hardware
- Can outperform processors due to
  - application specific logic
  - parallel nature
- Complex hardware like ALUs, filters, and processors can even be implemented



Project Goals



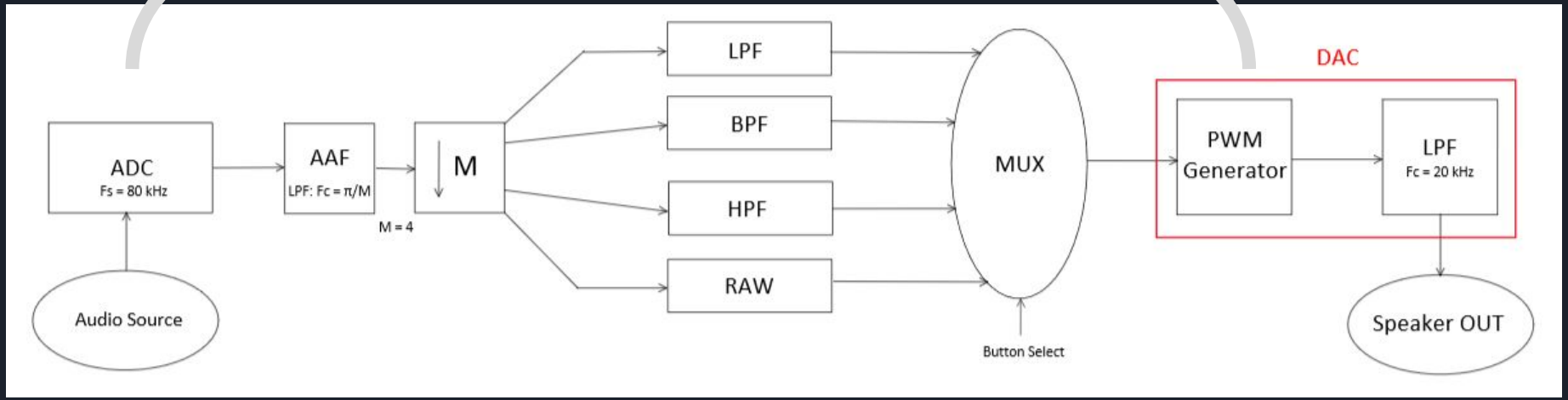
- Develop computer engineering abilities
- Gain understanding of FPGA uses and system design
- Fast, **real-time processing**
- High-performance capabilities
- Intelligible I/O

Our Implementation

15 vhdl files
- 11 unique components
- 4 test benches

15 IPs
21/100 DSP Slices
4 tcl files - configures simulations
1 xdc file - maps pins

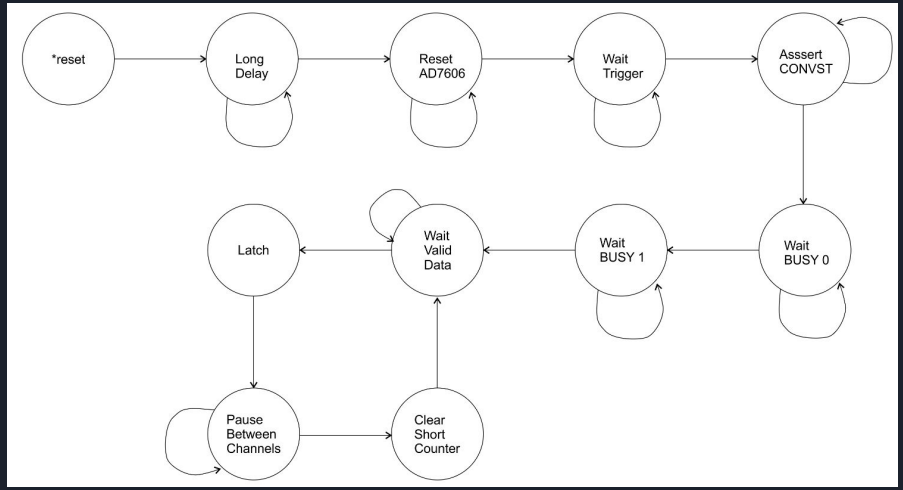
FPGA Operations

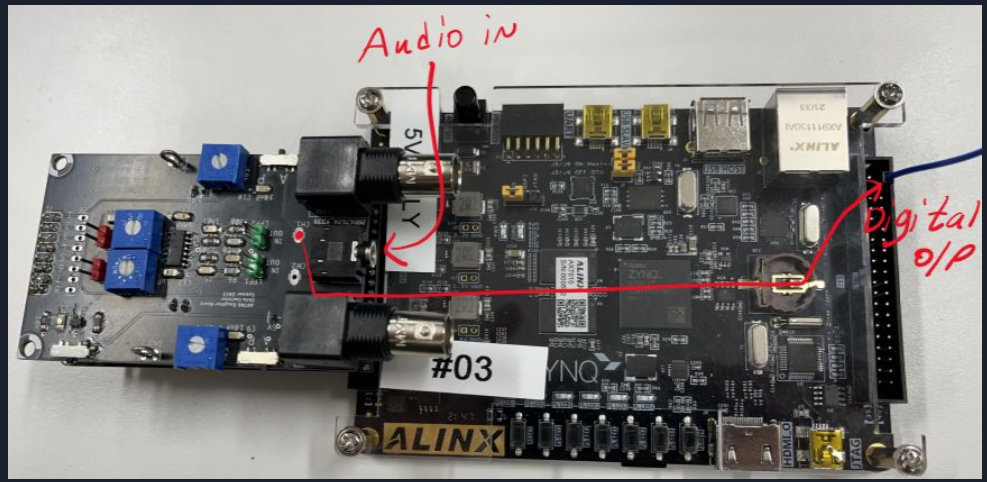


Analog To Digital Converter

- Programmed a counter/comparator pair to FPGA

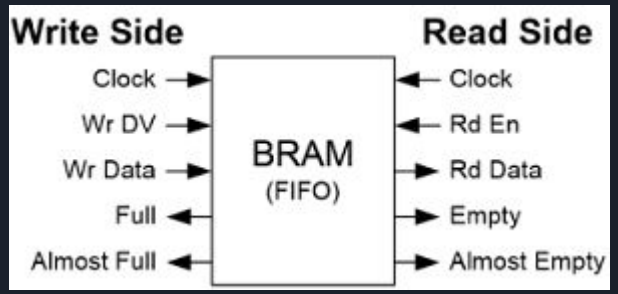
- Activates trigger
  - Tells ADC when to take samples (20 kHz)





Filter Implementation

- Filters have 16 bit input and output data
- FPGA Block Ram to store filter coefficients and data inputs
- DSP Slices to do intricate multiplication and addition
- 3 1000 Order filters, each with a 48 bit coefficient width
- Total of 21 DSP Slices and 9 blocks of Bram



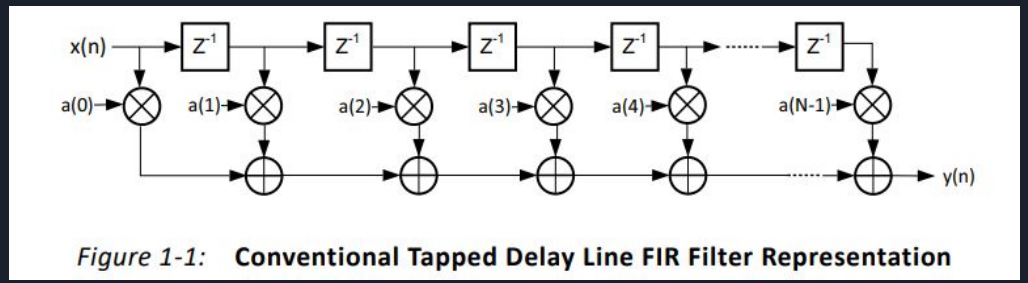
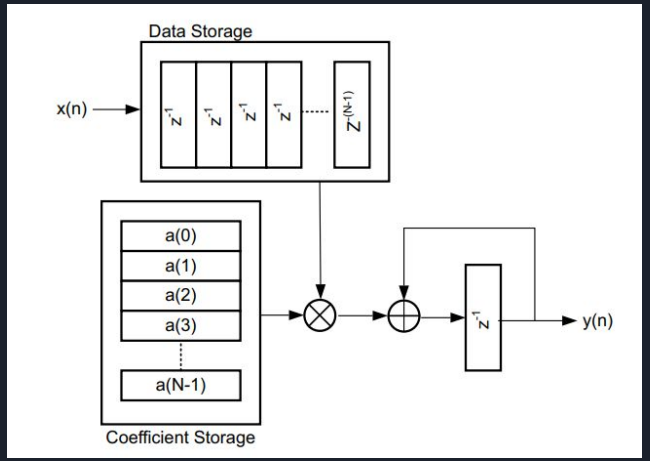
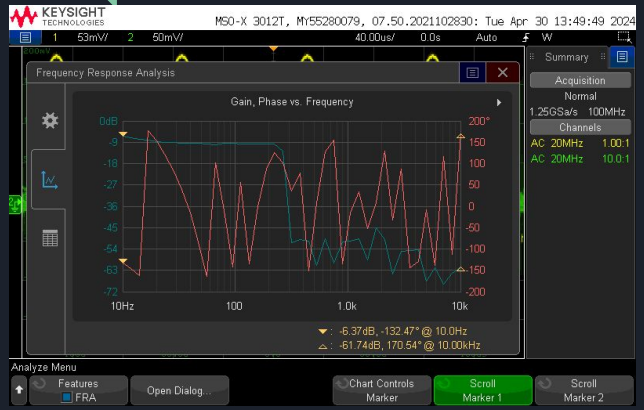
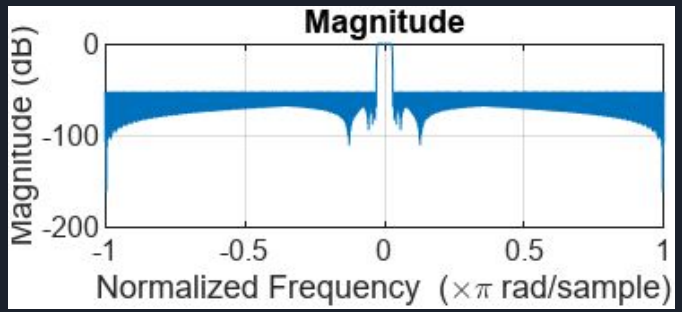


Figure 1-1: **Conventional Tapped Delay Line FIR Filter Representation**

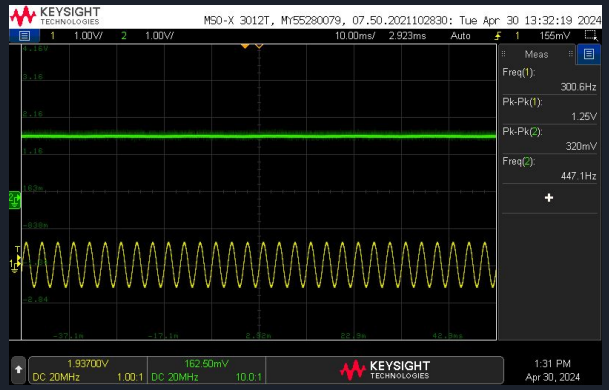


Low Pass Filter: f < 250 Hz

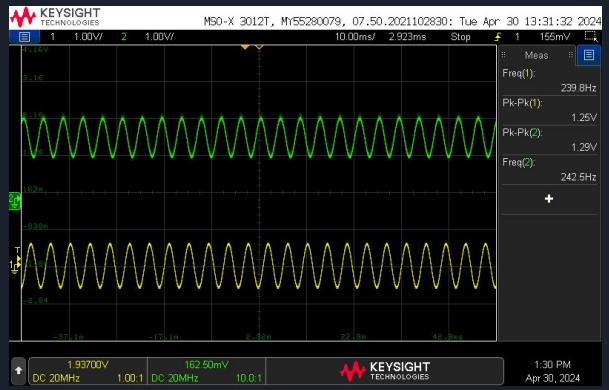




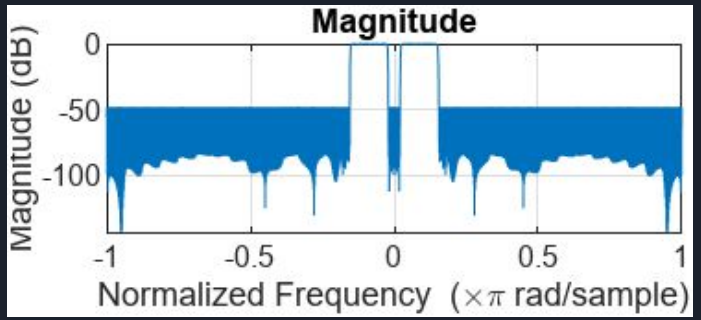
300 Hz



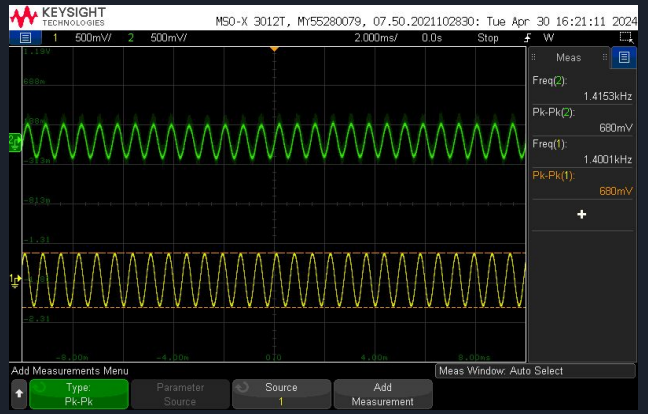
240 Hz



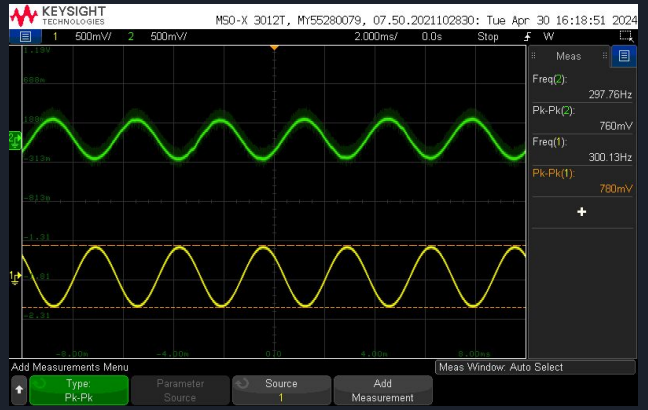
Bandpass Filter:
250 Hz < f < 1500 Hz



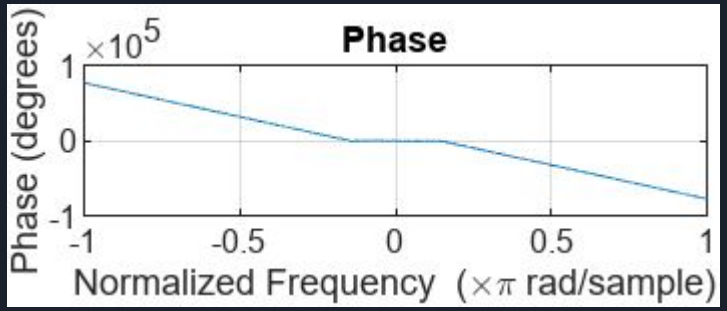
1400 Hz

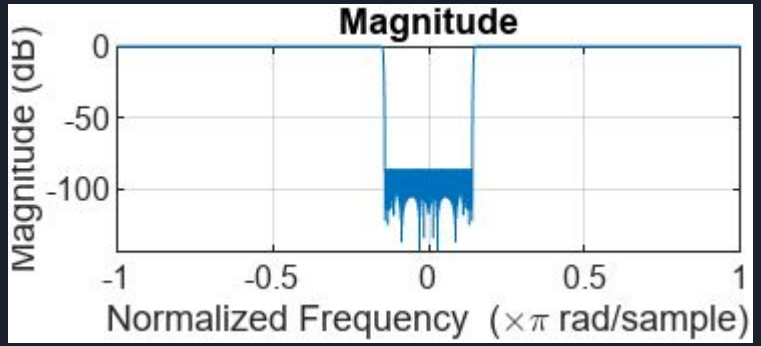


300 Hz

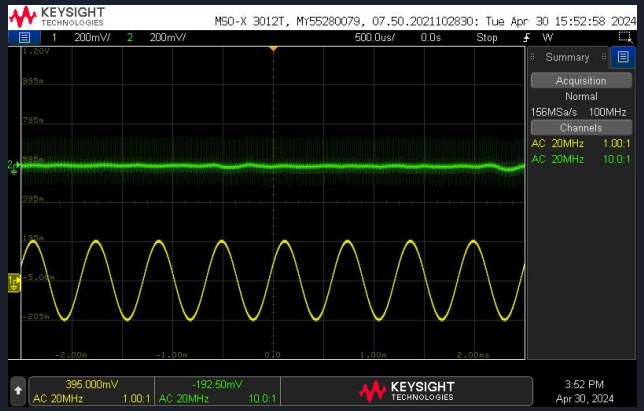


High Pass Filter: f > 1500 Hz

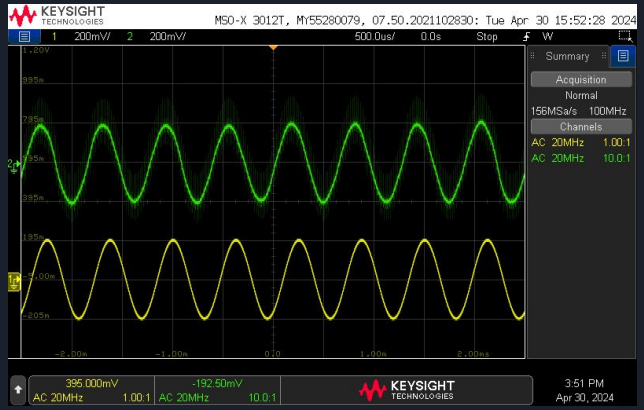




1400 Hz

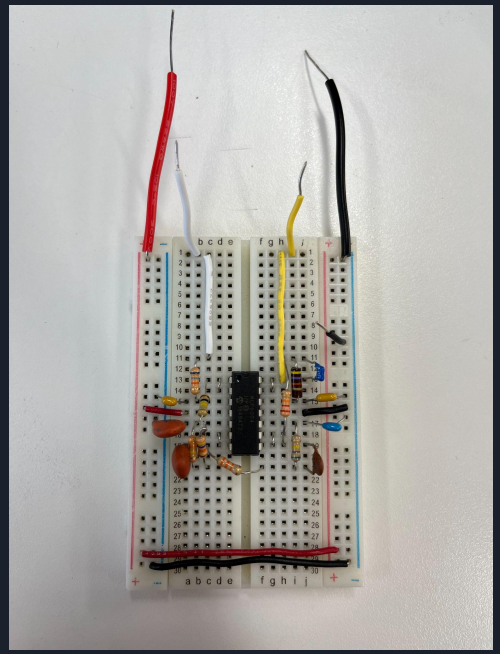


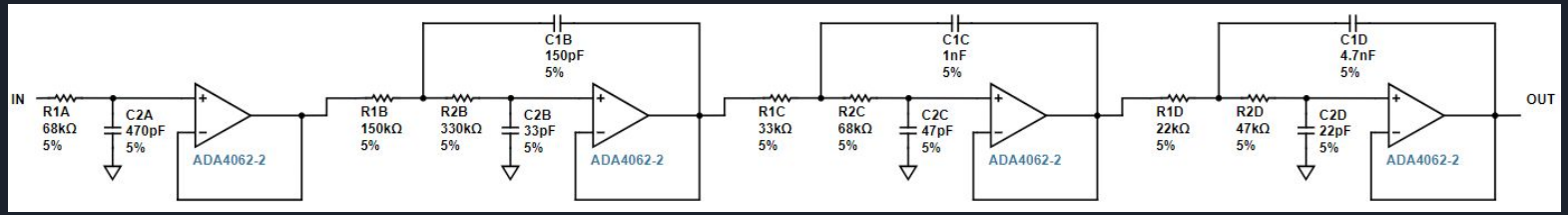
1800 Hz



Digital to Analog Converter

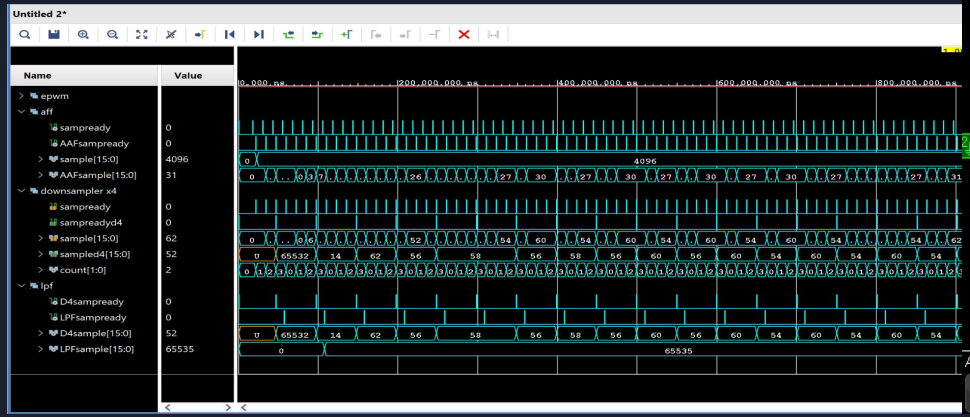
- Digital Values to PWM waveform
  - 50 MHz clock rate
  - Max 10-bit resolution
    - ~50 kHz PWM frequency
- LPF to cut out PWM frequency
  - Analog Filter
  - 7th Order Chebyshev

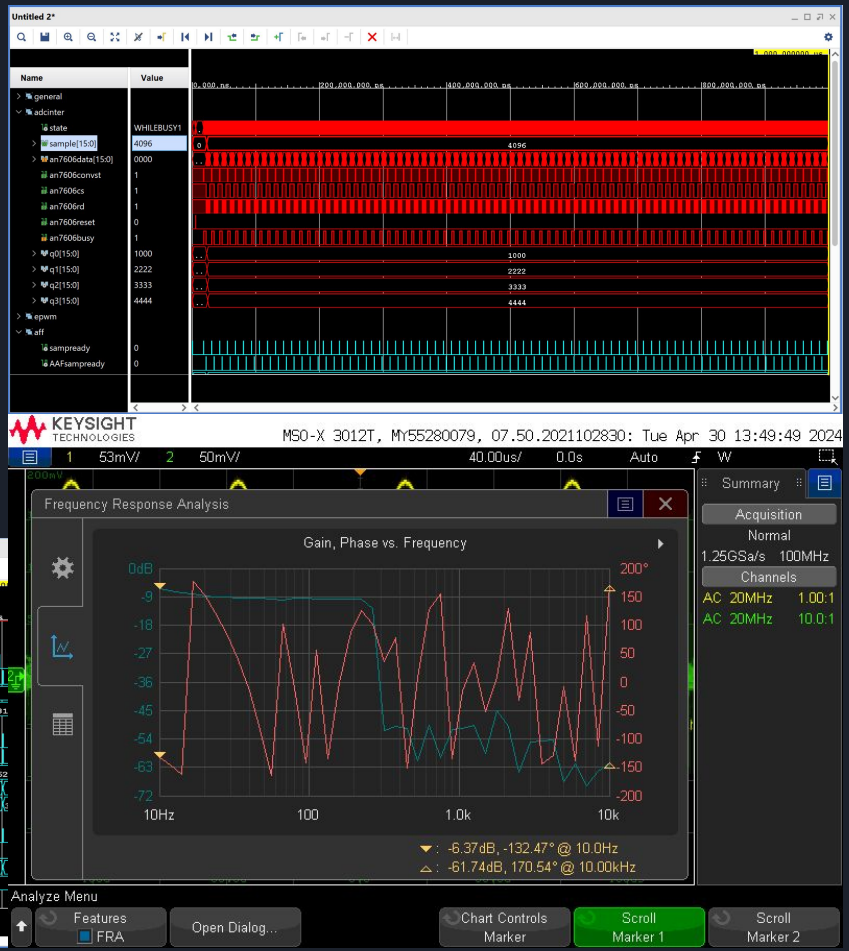




Debugging

- Used simulation to debug code
- Used an oscilloscope to verify output after programing
- Datasheets





Live Demo

60 Hz tone: https://www.youtube.com/watch?v=GqwFimG3X3w

1 kHz tone: https://www.youtube.com/watch?v=PyD9cMarVJk

2 kHz tone: https://www.youtube.com/watch?v=0voTVFmpVjY

Bohemian Rhapsody: https://www.youtube.com/watch?v=fJ9rUzIMcZQ

Mo Bamba: https://www.youtube.com/watch?v=cf45ZeUe2vg

Timmy Trumpet: https://www.youtube.com/watch?v=r1dquH_KOQc

Sidewalks and Skeletons: https://www.youtube.com/watch?v=EVLaJtg8xIU 1:20

Questions?

Sources

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