
NSLS-II CSX Beamline Docs Documentation

Release 0.1

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CSX-1 (23-ID-1) BEAMLINE DOCUMENTATION

Contents:

1.1 Fast CCD Detector

1.1.1 Introduction

The FastCCD installed in the endstation at CSX-1 is of the LBNL Fast CCD design. The sensor contains 1920 x 960 pixels of 30 μm x 30 μm and is arranged into two halves of 960 rows by 960 columns with the columns parallel to the long CCD axis. There is one output for each 10 columns (a “super column”) which results in 192 individual outputs and analogue to digital converters (ADC). The CCD camera can either be used in a traditional CCD with an x-ray shutter exposing the full chip, or in a framestore (frame transfer) mode by covering two quarters of the CCD with a light (x-ray) block effectively exposing half the chip along the column direction.

The analogue CCD signal is digitized by a custom designed fCRIC. Each fCRIC has 16 analogue inputs and digitizes with 13 bit precision and had 16 bit dynamic range. This is accomplished by having 3 gain ranges of 8x, 4x and 1x with an auto gain feature. In order to allow negative charge injection. The ADC is biased at a value of approximately 0x1000 with the exact value dependent on the ADC channel. The gain settings are stored in the two most significant bits of each ADC reading. The schematic of a single fCRIC channel is shown in Figure _fig_fcric

1.1.2 Specifications

- Pixel Size: 30 μm x 30 μm
- Active Area: 1920 pixels (column) x 960 pixels (row)
- 192 super columns = 192 outputs (480 rows x 10 columns)
- Pixel readout time: 500 μs
- Digitization time: 2 μs at 120 Hz
- 100 Hz maximum data collection

Table 1.1: Data Format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
G1	G0	ERR	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

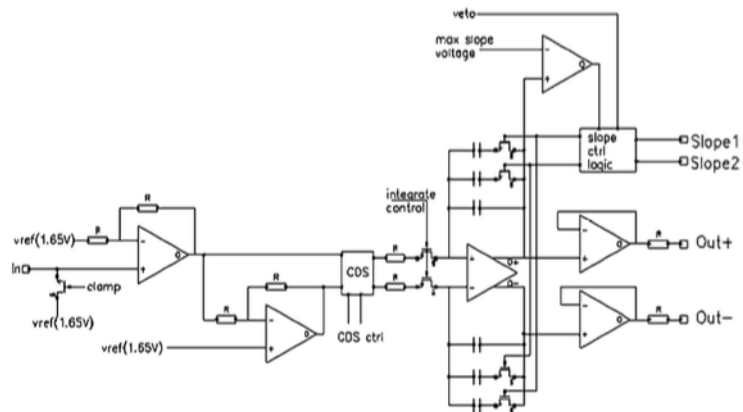


Table 1.2: Gain Setting

G1	G0	Gain	Pre-factor
0	0	x8	x1
1	0	x2	x4
1	1	x1	x8

$$I_{corr} = (I_{meas} * G) - BG$$

1.1.3 Useful Links

- [LBNL Fast CCD Site](#)
- [csxtools python analysis routines](#)
- [libcin low level c driver](#)
- [areaDetector Driver](#)

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