# Project: Traffic Lights Controller

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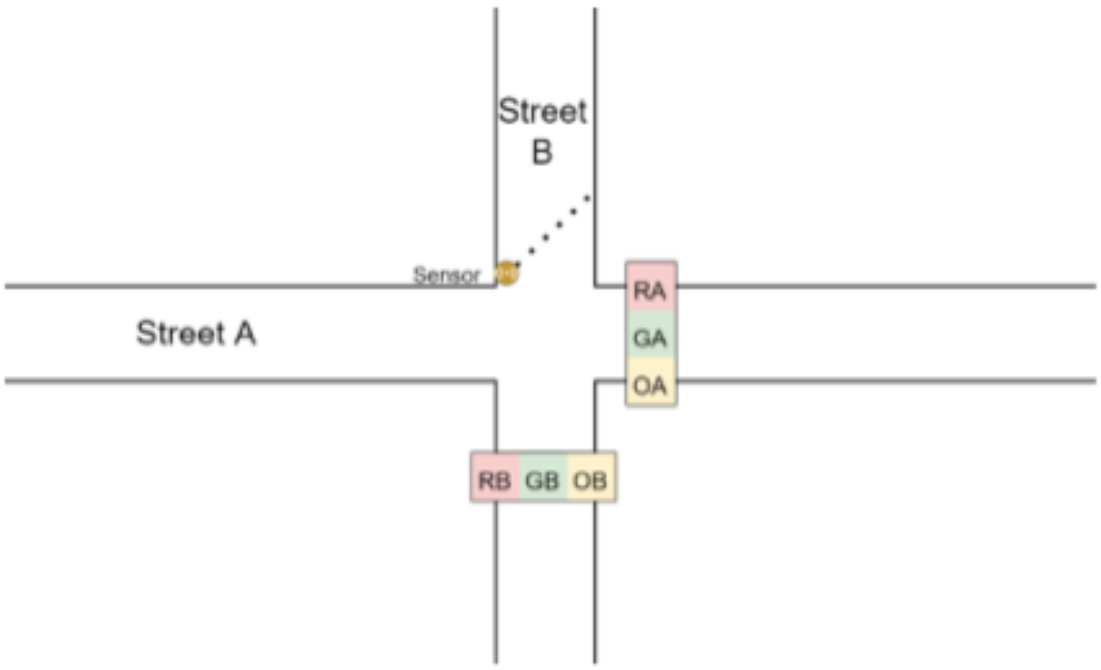
CS 2204

## *Objective:*

The goal of this project is to create Verilog code that embeds a finite state machine that regulates traffic lights at an intersection.

## *Introduction:*

The following intersection has two streets labeled street A and street B. For both streets A and B there is a traffic light directing traffic. The signal {RA, RB} is short for red which means stop, the {GA, GB} is green which means go, and {OA, OB} is orange which means slow down. In addition, street A is primary street and has a higher precedence over street B.

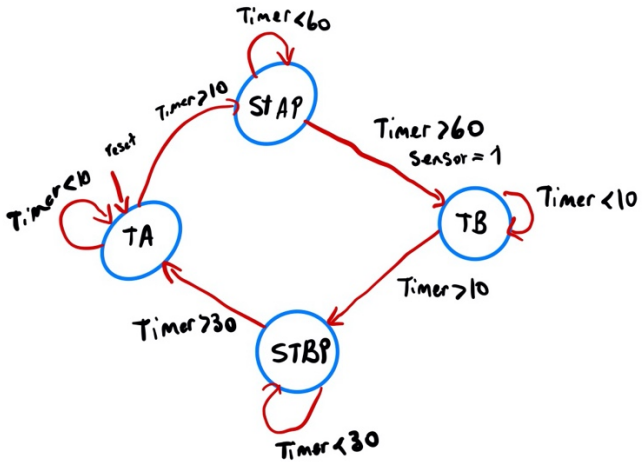


The Instructions:

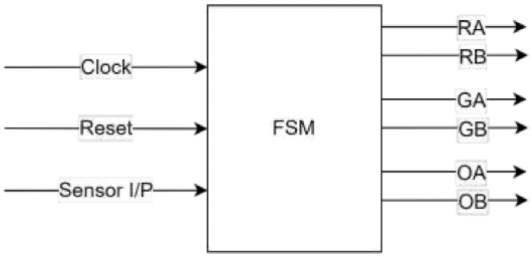
- There is a sensor placed on street B which detects any cars waiting on street B. This sensor outputs a 1 with value “High” if there is a car on street B and a “Low” if there is no car on street B.
- Once street A gets a green signal, it stays on for at least 60 seconds.
- If there is no car on street B, the signal A stays Green always.
- If the sensor detects a car on street B, the signal A turns orange for a duration of 10 seconds and then signal B turns Green with signal A turning Red.
- If the sensor detects a car on street B, the signal A turns orange for a duration of 10 seconds and then signal B turns Green with signal A turning Red.
- Once signal B turns red, signal A turns to green again.

**State Diagram:**

- **STAP:** Street A Pass
- **STBP:** Street B Pass
- **TA:** Traffic light A
- **TB:** Traffic light B




**Finite State Machine Circuit:**



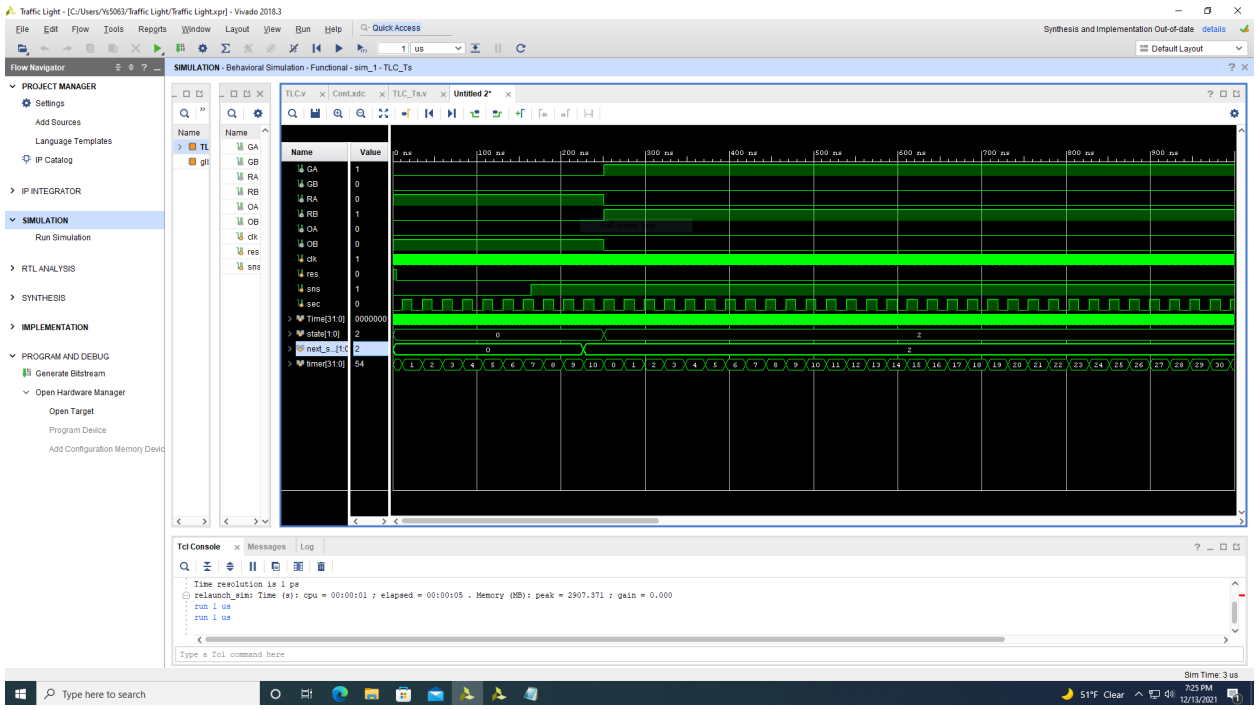
1. GA: Green for traffic light A
2. GB: Green for traffic light B
3. RA: Red for traffic light A
4. RB: Red for traffic light B
5. OA: Orange for traffic light A
6. OB: Orange for traffic light B

**Table:**

| Output | STAP | STBP | TA | TB |
|---|---|---|---|---|
| GA | 1 | 0 | 0 | 0 |
| GB | 0 | 1 | 0 | 0 |
| RA | 0 | 1 | 1 | 0 |
| RB | 1 | 0 | 0 | 1 |
| OA | 0 | 0 | 0 | 1 |
| OB | 0 | 0 | 1 | 0 |

**Simulation:**

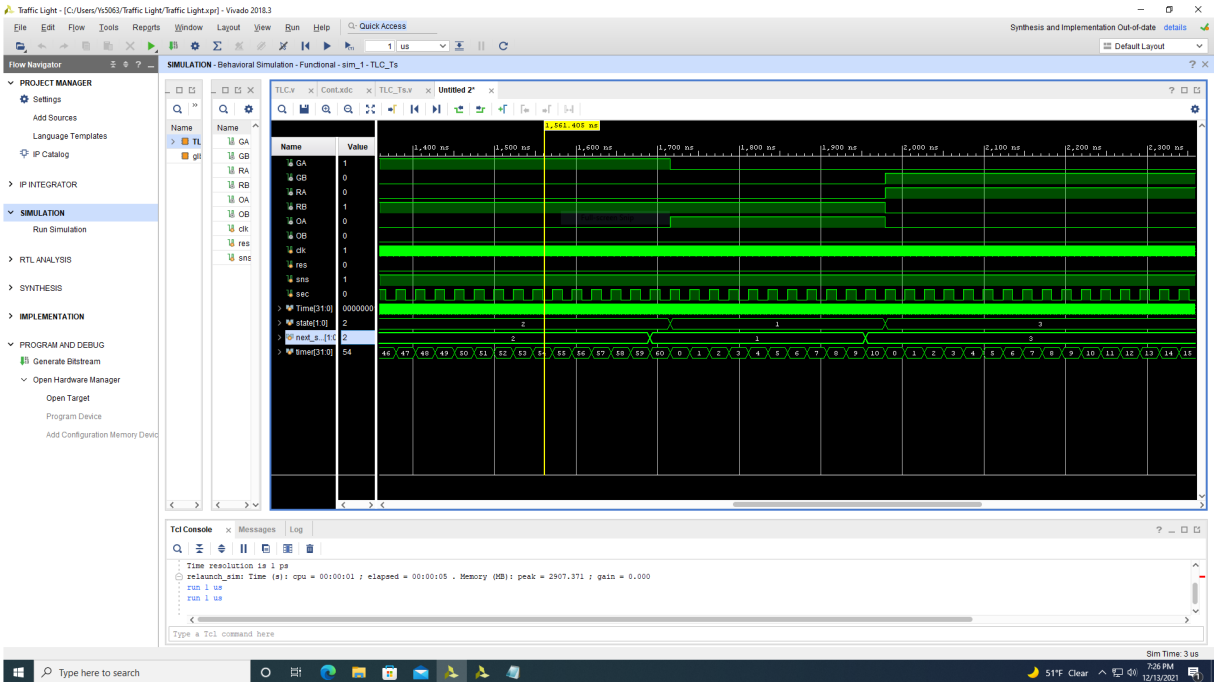
**States: TA & STAP**




We begin in state TA, which is our reset state. That instance, traffic light B will be orange for 10 seconds before turning red, while traffic light A will become red. After 10 seconds, we switch to STAP mode, where traffic light B is red and traffic light A is green for 60 seconds. As

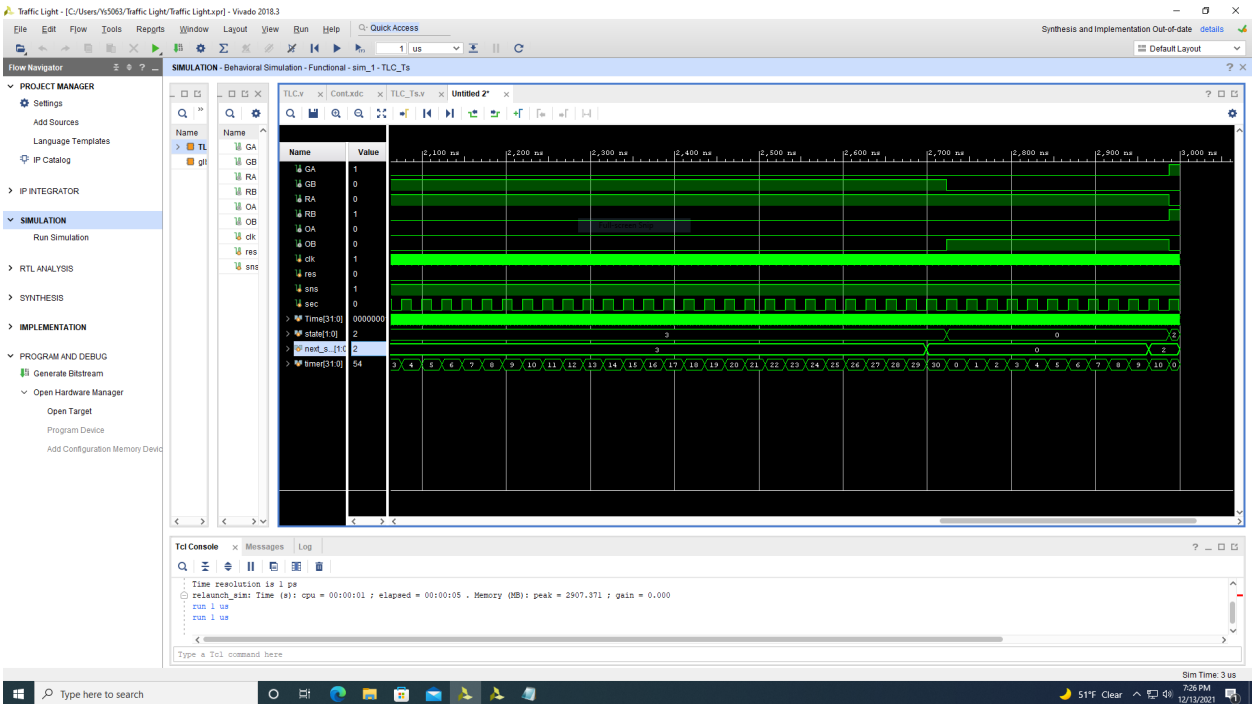
demonstrated in the waveform above, we were in state "0" for 10 seconds before transitioning to state "2," where "0" is TA and "2" is STAP. (Can be verified by looking at the Verilog code). In addition, by analyzing the waveform we can see that TA is RA=1 and OB=1 while everything else remains at zero as instructed (Traffic light A is Red and Traffic light B is orange). After transitioning to state STAP we see that GA=1 and RB=1 and senser=1. This means that the traffic light A is now green and traffic light at B is now red while there is a car detected by the sensor at street B.

## States: TB & STBP



After 60 seconds, will transition to state TB due to the sensor detecting a car at street B. Will stay at TB for 10 seconds before switching to state STBP. This indicates that traffic light at street A will be Orange for 10 seconds before turning Red. Once, the 10 seconds are up will go to state STBP. At STBP the traffic light at street B will turn green and red for traffic light at A for a duration of 30 seconds. As shown in the waveform above we have at state “1” (TB) where OA=1 and RB=1 which means that traffic light at street A is now orange and red for street light at B as stated above. Then we have at state “3” (STBP) GB=1 and RA=1 this shows that traffic light at B is now green and traffic light at A is now red.

## State: STEP & TA



After 30 seconds will go from STEP back again to TA, as shown in the waveform above which demonstrates a full cycle.

In conclusion, in this lab we were able to construct a simple finite state machine that can safely direct traffic at an intersection using traffic lights. This demonstrates the significance of finite state machines in real-world applications. I know that as my engineering education progresses, finite state machines will be fundamental to designing more complex innovations in the future.