This folder contains:

1. **Zipped folder** containing **a library which has four cells**.
2. **Two individual files (A spice file and a testbench)**

Please follow the steps below carefully to integrate and understand each component.

🔹 **1. ece_482_pdn_v2 – Unzip this. Add this library to your gpdk045_new folder. Add the name to cds.lib file as well.**

Included Cells in the library:

1. **Decoupling Capacitor (Unit Cell):**
   A single decap unit cell.
2. **Decoupling Capacitor (Double Cell):**
   Two unit cells combined into one structure for higher capacitance density.
3. **Decap Tile:**
   A larger decap array design placed between the **VDDIO** and **VSSIO** rails at the **bottom-left corner** of the design.
   - Only **one instance** of this tile has been included for demonstration.
   - You should add **multiple tiles** across your layout to effectively mitigate supply noise.

Important:
The provided decaps are designed for the **VDDIO (1.8 V)** rail.
If you wish to add decaps for the **VDD (1.1 V)** rail, you must create new decap cells using **1.1 V transistors**.

4. **PDN Cell:**
   This is the **top-level power delivery network and pad ring** designed for you.
   - Power routing for **VDDIO**, **VDD**, and **VSS** is implemented on the **top two metal layers (M11 and M10)**.
   - The **VSS** and **VSSIO** rails have been **shorted** on-chip for a unified ground reference.
   - To power your own devices, you must **connect power and ground through vias** to the corresponding rails.

Pad and Pin Naming

- **VDD pads:** VDD1, VDD2, VDD3
- **VDDIO pads:** VDDIO1, VDDIO2, VDDIO3
- **VSS pads:** VSS1, VSS2, VSS3, VSS4
- **VSSIO pads:** VSSIO1, VSSIO2, VSSIO3

Note: Since **VSS** and **VSSIO** are shorted on-chip, all these pins belong to the **same net**.

All **input**, **clock**, and **output** signals have names ending with the suffix **_oc** (meaning *on-chip*).
Explore the **top-level PDN cell** to understand the pin connections and overall hierarchy.

🔹 2. Testbench File

This file contains the testbench setup and is fully commented.
Please **read through the comments** to understand how the testbench connects to the PDN and how to perform simulations.

🔹 3. SPICE File

This SPICE file models the **dummy M11 resistors** used in the PDN design.
Save this file in the **same directory** as your testbench file so it can be correctly referenced during simulation.

⚠️ Notes and Known Issues

- When performing **LVS**, you may see a warning similar to the following image even though the comparison result is a match:


```
Warnings and errors of connectivity for cell "resm11_CDNS_762391755460"

  [WARN] Unattached port label:
      Label "PLUS" on layer 1063(ind11_text) at (3.000, -0.110)

  [WARN] Unattached port label:
      Label "MINUS" on layer 1063(ind11_text) at (3.000, 1.110)
```

This is a **known bug** related to the dummy **resm11** resistors and can be safely **ignored**.

- When running **DRC**, **LVS**, and **extraction**, you should not encounter any other errors or warnings besides the one mentioned above.