UNIVERSIDAD DE COSTA RICA

IE-0624 Laboratorio de Microcontroladores

Laboratorio # 1

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1 Introducción

En el presente trabajo se creo un circuito capaz de emular el comportamiento de una tómbola de un bingo sencillo, para ello se utilizaron una serie de componentes electrónicos, donde el más importante de ellos es el microcontrolador PIC12F683.

El circuito final se compone de tres partes fundamentales, el circuito de entrada, creado para evitar picos de tensión propios de los interruptores, el microcontrolador que lleva cargado un programa desarrollado en C para controlar 3 pines de salida que serán usados para implementar un simple protocolo de comunicación serial y finalmente el circuito de salida que se compone de compuertas lógicas, flip flops, demultiplexores, decodificadores y displays de 7 segmentos.

Con la implementación propuesta se logró hacer funcionar el circuito cumpliendo casi todas las especificaciones, pero debido a la falta de memoria no se pudo implementar una de ellas, que posteriormente se comentará con detalle, por otro lado los valores calculados teóricamente fueron alcanzados según como se muestra en los resultados finales.

El repositorio de Github se puede consultar en la siguiente dirección:

https://github.com/JackTheKnife16/IE-0624_Laboratorio_de_Microcontroladores_I_2023

2 Nota Teórica

En este apartado se mostrarán algunas características del microcontrolador así como la justificación de la utilización de los componentes externos y el diagrama de flujo del firmware creado para el microcontrolador.

2.1 Microcontrolador PIC12F683

2.1.1 Características Generales

El microcontrolador PIC15F683 cuenta con una memoria de programa flash de 1024 words, un Data Memory de 64 Bytes SRAM y 128 Bytes EEPROM, con 8 Pines, 6 de ellos I/O configurables, 1 comparador y 1 timer de 8 y otro de 16 bits.

2.1.2 Diagrama de Bloques

En la Figura 1 se muestra en detalle el diagrama de bloques del microcontrolador.

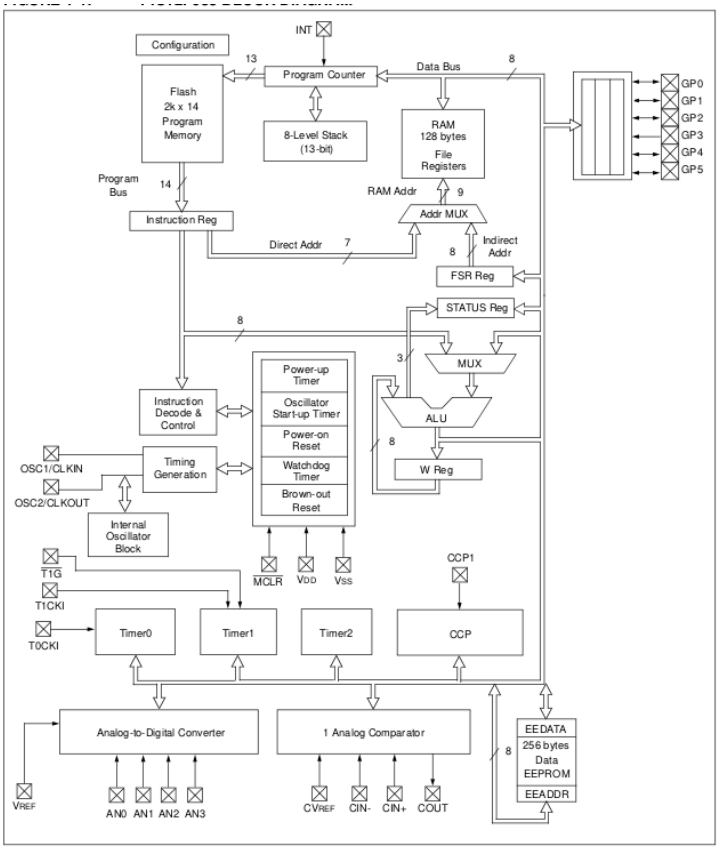


Figura 1: Diagrama de Bloques del PIC12F683 [1]

2.1.3 Diagrama de Pines

En la Figura 2 se muestra el diagrama de pines del microcontrolador.

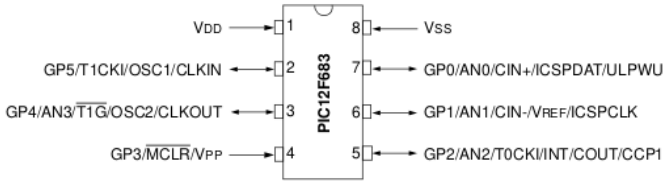


Figura 2: Diagrama de Pines del PIC12F683 [1]

2.1.4 Características Eléctricas

En la Figura 3 se muestran las características eléctricas del microcontrolador.

Absolute Maximum Ratings(†)

Ambient temperature under bias	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss	-0.3V to +13.5V
Voltage on all other pins with respect to V_{SS}	-0.3V to (V_{DD} + 0.3V)
Total power dissipation(1)	800 mW
Maximum current out of V_{SS} pin	95 mA
Maximum current into V_{DD} pin	95 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by GPIO	90 mA
Maximum current sourced GPIO	90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Figura 3: Características Eléctricas del PIC12F683 [1]

2.2 Diagrama Funcional del Circuito

En la Figura 4 se muestra el diagrama funcional para el laboratorio, se puede ver la representación de cada una de las partes del circuito, que consta de 3, circuito de entrada, circuito de salida y microcontrolador. En la figura se esboza el funcionamiento del protocolo de comunicación serial, que está compuesto de dos demultiplexores para manejar tanto la entrada del circuito de salida como el reloj que controla los flip flops de conversión a paralelo, y un contador que usa el mismo pulso de los clk de los flip flops pero con una compuerta not para invertir el reloj.

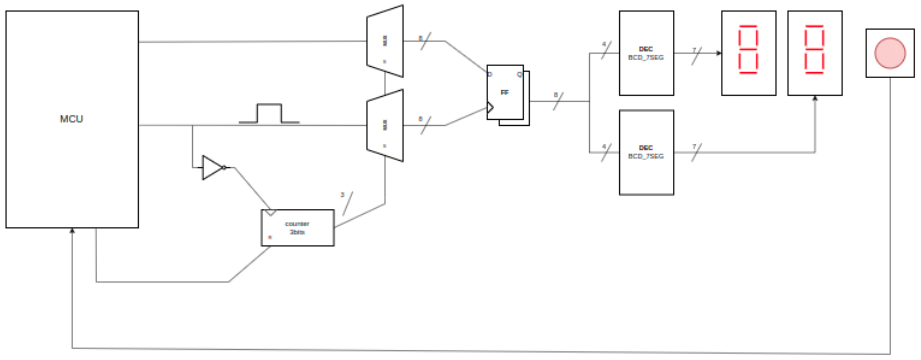


Figura 4: Diagrama funcional para la tómbola electrónica [imagen propia]

2.3 Firmware del Circuito

En la Figura 5 se muestra el diagrama de FSM con el que se creó el firmware del microcontrolador, en este diagrama se explica de forma visual el funcionamiento que tendrá el microcontrolador. Las letras en el diagrama se refieren a lo siguiente:

- A: no se ha presionado el pulsador.
- B: se ha presionado el pulsador.
- C: se ha presionado el pulsador pero la cuenta no llega a 16.
- D: se ha presionado el pulsador y la cuenta es 16.

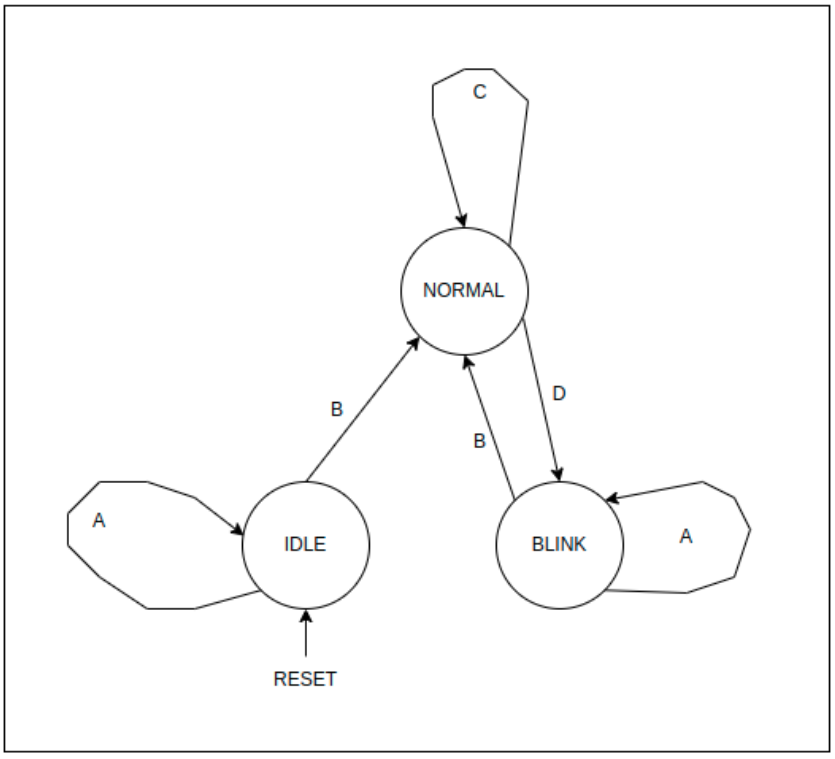


Figura 5: Diagrama de flujo del firmware [imagen propia]

2.4 Componentes Electrónicos Complementarios

El sistema que resuelve el problema planteado para este proyecto se diseñó con tres partes fundamentales, primero el circuito de entrada, segundo el microcontrolador y tercero el circuito de salida (los leds de 7 segmentos junto con su lógica de control, flip flops, etc incluyendo los componentes del protocolo de comunicación). El primero y el tercero corresponden a los componentes complementarios, en la Tabla se listan los componentes utilizados para cada uno de dichas partes, así como su precio en el mercado en colones.

2.5 Diseño de los circuito Complementarios

Los dos circuitos complementarios serán explicados en detalle a continuación, mientras que el diseño del firmware se mostró anteriormente y por su sencillez no requiere de mayor explicación.

Código	Tipo	Característica	Cantidad	Precio	Subsistema
PIC12F683	Microcontrolador	-	1	1549	Microcontrolador
-	Capacitor	10 µF	1	190	Entrada
-	Pulsador	-	1	99	Entrada
-	Resistencia	100 Ω	1	199	Entrada
-	Resistencia	232 Ω	1	199	Entrada
-	Resistencia	90 Ω	20	199	Salida
74HC4511	Decodificador	-	2	915	Salida
157102B12700	Display 7 SEG	2.4 V , 20 mA	2	2373	Salida
-	flip flop RS	5 V	8	450	Salida
SN74LS109ADR	flip flop JK	5 V	2	1119	Salida
74HC238	Demultiplexor	5 V	2	310	Salida
NTE74HC08	AND GATE	5 V	3	1104	Salida
NTE4050B	BUFFER	5 V	1	591	Salida

Tabla 1: Información de los componentes utilizados

2.5.1 Circuito de Entrada

El circuito de entrada se compone de un pulsador y un circuito RC para controlar los picos de tensión al accionar el pulsador. El RC es un poco más complejo debido a que el microcontrolador requiere una resistencia de pull down. Para este circuito se debía determinar el valor de dos resistencias y un capacitor conociendo ciertos datos:

- La tensión de entrada al PIN 3 del microcontrolador debe ser superior a 3 V ya que es suficiente tensión para que el microcontrolador reconozca como un valor en alto.
- El capacitor debe cargarse a su valor final en un tiempo no mayor a 5 ms, un tiempo mucho menor a la velocidad de reacción que puede tener un ser humano al pulsar un botón.

En la Figura 6 se muestra el esquemático del circuito de entrada, con este y un poco de cálculo se obtendrán los valores para las resistencias y la capacitancia.

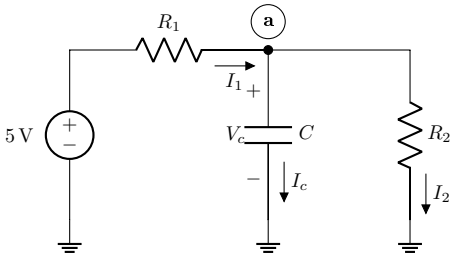


Figura 6: Esquemático del Circuito entrada [imagen propia]

Aplicando Ley de Corrientes de Kirchhoff en el nodo a, obtenemos que:

$$\frac{5 - V_c}{R_1} = C\frac{dV_c}{dt} + \frac{V_c}{R_2} \tag{1}$$

Reacomodando la ecuación llegamos a:

$$\frac{dV_c}{dt} + \frac{R_1 + R_2}{CR_1R_2} \cdot V_c = \frac{5}{CR_1} \tag{2}$$

sea $a = \frac{R_1+R_2}{CR_1R_2}$ y $b = \frac{5}{CR_1}$ tenemos que:

$$\frac{dV_c}{dt} + aV_c = b \tag{3}$$

Claramente el factor integrante para resolver este problema será: e^{at}, multiplicando esto a ambos lados de (3) y luego agrupando tenemos que:

$$e^{at}\frac{dV_c}{dt} + aV_c e^{at} = be^{at}$$
$$\frac{d}{dt}\left[e^{at}V_c\right] = be^{at}$$
$$d\left[e^{at}V_c\right] = be^{at}dt$$

Integrando a ambos lados y luego despejando:

$$e^{at}V_c = \frac{b}{a}e^{at} + k$$

$$V_c = \frac{b}{a} + ke^{-at}$$

Suponiendo que en $t = 0$, $V_c(0) = 0$ (capacitor está descargado en el tiempo 0) entonces $k = -\frac{b}{a}$, por lo que:

$$\boxed{V_c = \frac{b}{a}\left[1 - e^{-at}\right]} \tag{4}$$

Sabemos por tanto que b/a es el valor de la tensión en régimen permanente, y fijaremos tal valor en $3.5\,\mathrm{V}$:

$$\frac{b}{a} = \frac{5R_2}{R_1 + R_2} = 3.5$$

manipulando la ecuación se obtiene la relación entre las resistencias:

$$\boxed{R_2 = \frac{7}{3}R_1} \tag{5}$$

Por otro lado sabemos por los requerimientos mencionados antes que $5\tau \leq 5\,\mathrm{ms}$

$$5\tau = \frac{5}{a} = \frac{5CR_1}{R_1 + R_2} \tag{6}$$

Utilizando la relación de las resistencias obtenida anteriormente tenemos que:

$$5\tau = \frac{7CR_1}{2} \leq 5 \times 10^{-3} \tag{7}$$

despejando C obtenemos finalmente la relación entre C y R_1:

$$\boxed{C \leq \frac{1}{700R_1}} \tag{8}$$

Por lo que tomando un R_1 definimos ya todos los valores:

$$\boxed{R_1 = 100\,\Omega,\ R_2 = 233.33\,\Omega,\ C = 10\,\mu\text{F} \leq 14.29\,\mu\text{F}} \tag{9}$$

2.5.2 Circuito de Salida

El circuito de salida consta de dos partes:

- Protocolo de comunicación: consta de un convertidor serial paralelo con memoria, construido utilizando demultiplexores, algunas compuertas lógicas, un contador hecho con flip flops JK y 8 flip flops para almacenar valores que posteriormente serán convertidos por la siguiente etapa.
- Consta de dos decodificadores BCD a 7 Segmentos unas resistencias y dos displays de 7 segmentos para mostrar los valores de salida.

Para el dimensionamiento de las resistencias se utilizaron valores teóricos de salida para el decodificador que es de 5 V y los valores recomendados para los displays que requieren una tensión de entrada de 2.4 V y una corriente máxima de 2 mA. Por lo que:

$$R \approx \frac{5 - 2.4}{0.02} \approx 130\,\Omega \tag{10}$$

En este caso esta debería ser la resistencia teórica, no obstante a partir de este valor se puede calibrar mediante prueba y error una resistencia que nos de un valor cercano a los 0.02 A para que los displays se vean bien, en este caso debido a que la tensión de salida de los decodificadores es cercana a 4.21 V tenemos que la resistencia más apropiada es:

$$R \approx \frac{4.21 - 2.4}{0.02} \approx 90\,\Omega \tag{11}$$

Para efectos reales siempre se debe empezar con los valores teóricos que son los seguros y luego ir calibrando según los valores experimentales. En la Figura 7 se muestra las mediciones para la resistencia de salida escogida.

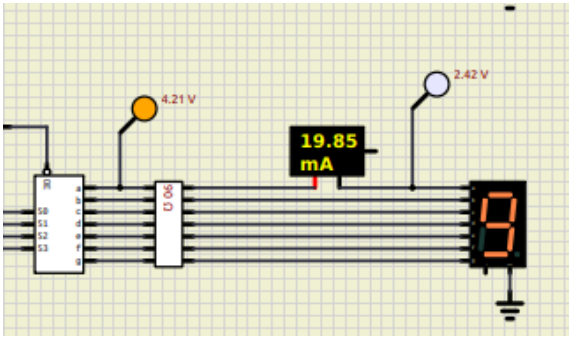


Figura 7: Medición de valores para resistencia de salida de 90 ohms [imagen propia]

3 Análisis de Resultados

En este apartado se mostrarán capturas de pantalla del funcionamiento del circuito en la simulación, para el estado IDLE y para el estado NORMAL, el estado BLINK no se muestra porque no se puede capturar su funcionamiento con imágenes, pero para ello se creó un video donde se ve el funcionamiento, el cual se puede consultar en esta dirección:

https://youtu.be/s3Oc7wJ_rpQ

En la Figura 9 se muestra el estado IDLE en el cual aún no se ha presionado el pulsador por lo que los displays están apagados, para conseguir esto se apagan los decodificadores, para eso son las compuertas and que se conectan a dos flip flops por cada decodificador y a la entrada que sirve para apagar dicho decodificador.

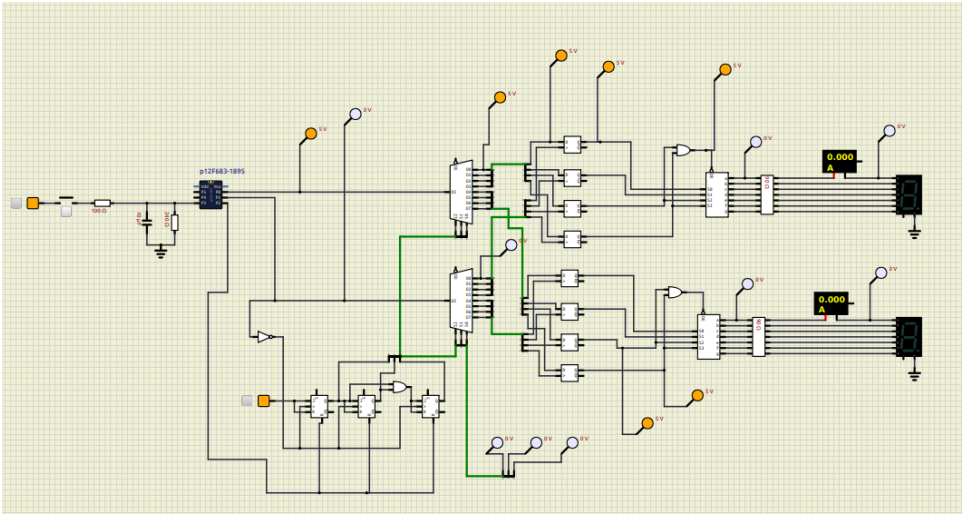


Figura 8: Estado IDLE trabajando [imagen propia]

En la Figura **??** se muestra el funcionamiento del estado Normal, donde los displays están mostrando un valor, se mantendrá en este estado hasta que se hayan mostrado los 16 resultados.

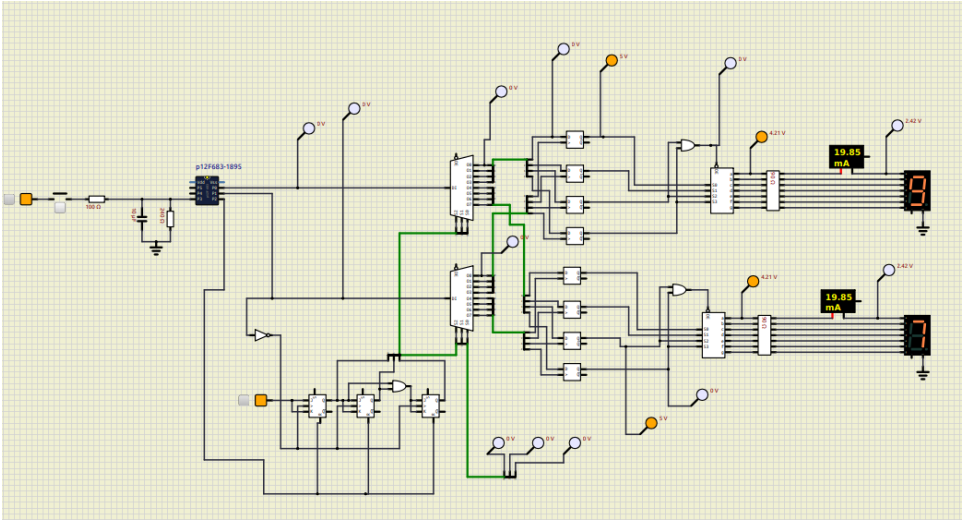


Figura 9: Estado Normal Trabajando [imagen propia]

En el estado BLINK como se muestra en el video se muestran los valores 99 y parpadean, para salir del estado BLINK se debe presionar el pulsador, con lo que se vuelve a estado normal y muestra el primer resultado de la siguiente ronda.

Por otro lado también se deben mencionar los objetivos no alcanzados, en este caso por cuestiones de memoria del micro no fue posible implementar la función que corrobora si un número se ha repetido, sea por ineficiencia a la hora de hacer el código o por que la estrategia elegida para resolver el problema, la FSM requería mucho espacio de memoria, o bien porque el diseño original no tomó en cuenta el problema de la memoria, que en este caso este punto es una certeza, mientras que los otros puntos pueden ser ciertos también. Sea la causa una de estas o una combinación de estas, este objetivo no se logró y dado lo avanzado del proyecto y el tiempo requerido para rediseñar todo el laboratorio se decidió entregar sin esta funcionalidad.

4 Conclusiones y Recomendaciones

En el presente trabajo se mostró como un microcontrolador, específicamente el PIC12F683, puede ser usado para realizar un tarea simple específica, como se mostró anteriormente con el manejo de los displays de 7 segmentos para emular una tómbola electrónica. El laboratorio no se pudo completar con todas las funcionalidades, por lo expuesto en la sección pasada, sin embargo se logró mostrar las otras funcionalidades e implementar un algoritmo que funcionó según lo esperado.

4.1 Recomendaciones

Se recomienda empezar los diseños teniendo en cuenta siempre el espacio de memoria disponible del microcontrolador, para el caso de este laboratorio el diseño era correcto teóricamente, los circuitos auxiliares funcionaron correctamente, la codificación también, pero al no tomar en cuenta el tamaño de la memoria no se pudo completar el último objetivo.

Bibliografía

[1] Microchip Technology Inc, *PIC12F683 Data Sheet 8-Pin Flash-Based 8-Bit CMOS Mocrocontrollers with nanoWatt Technology*, 2007.

5 Apéndices

ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748−5089
http://www.nteinc.com

NTE74HC08
Integrated Circuit
TTL − High Speed CMOS,
Quad, 2−Input AND Gate

Description:

The NTE74HC08 is a logic function in a 14−Lead plastic DIP type package fabricated using advanced silicon−gate CMOS technology which provides the inherent benefits of CMOS − low quiescent power and wide power supply range. This device is input and output characteristic and pinout compatible with standard NTE74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

The NTE74HC08 is intended to interface between TTL and NMOS components and standard CMOS devices. This device is also a plug−in replacement for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage range: 2V to 6V
- Low Input Current: 1.0μA
- High Noise Immunity Characteristics of CMOS Devices

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . −0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . −0.5 to V_{CC} +0.5V
DC Output Voltage, V_{OUT} . . . . . −0.5 to V_{CC} + 0.5V
DC Input Current (Per Pin), I_{IN} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . −65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+125	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (Voltages Referenced to GND unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				–55 to +25°C	≤ 85°C	≤ 125°C	
Minimum High Level Input Voltage	V_{IH}	V_{OUT} = 0.1V or V_{CC} –0.1V, $\|I_{OUT}\| \leq$ 20µA	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	V
			4.5	3.15	3.15	3.15	V
			6.0	4.20	4.20	4.20	V
Maximum Low Level Input Voltage	V_{IH}	V_{OUT} = 0.1V or V_{CC} –0.1V, $\|I_{OUT}\| \leq$ 20µA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	V
			4.5	1.35	1.35	1.35	V
			6.0	1.80	1.80	1.80	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq$ 20µA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	V
			6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq$ 2.4mA	3.0	2.48	2.34	2.20	V
		$\|I_{OUT}\| \leq$ 4.0mA	4.5	3.98	3.84	3.70	V
		$\|I_{OUT}\| \leq$ 5.2mA	6.0	5.48	5.34	5.20	V
Maximum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq$ 20µA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	V
			6.0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \leq$ 2.4mA	3.0	0.26	0.33	0.40	V
		$\|I_{OUT}\| \leq$ 4.0mA	4.5	0.26	0.33	0.40	V
		$\|I_{OUT}\| \leq$ 5.2mA	6.0	0.26	0.33	0.40	V
Maximum Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0µA	6.0	2.0	20	40	µA

AC Electrical Characteristics: (t_r = t_f = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				–55 to +25°C	≤ 85°C	≤ 125°C	
Maximum Propagation Delay, Input A or B to Output Y	t_{PLH}, t_{PHL}		2.0	75	95	110	ns
			3.0	30	40	55	ns
			4.5	15	19	22	ns
			6.0	13	16	19	ns

AC Electrical Characteristics (Cont'd): ($t_r = t_f$ = 6ns, C_L = 50pF unless otherwise specified)

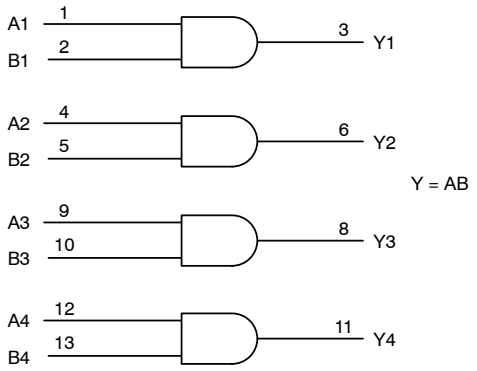
Parameter	Symbol	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55 to +25°C	≤ 85°C	≤ 125°C	
Maximum Output Transition Time, Any Output	t_{TLH}, t_{THL}		2.0	75	95	110	ns
			3.0	27	32	36	ns
			4.5	15	19	22	ns
			6.0	13	16	19	ns
Maximum Input Capacitance	C_{in}		–	10	10	10	pF
Parameter	**Symbol**	**Test Conditions**		**Typical @ +25°C, V_{CC} = 5V, V_{EE} = 0V**			**Unit**
Power Dissipation Capacitance (Per Buffer)	C_{PD}	Note 4		20			pF

Note 4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Truth Table:

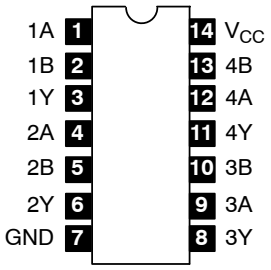
Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

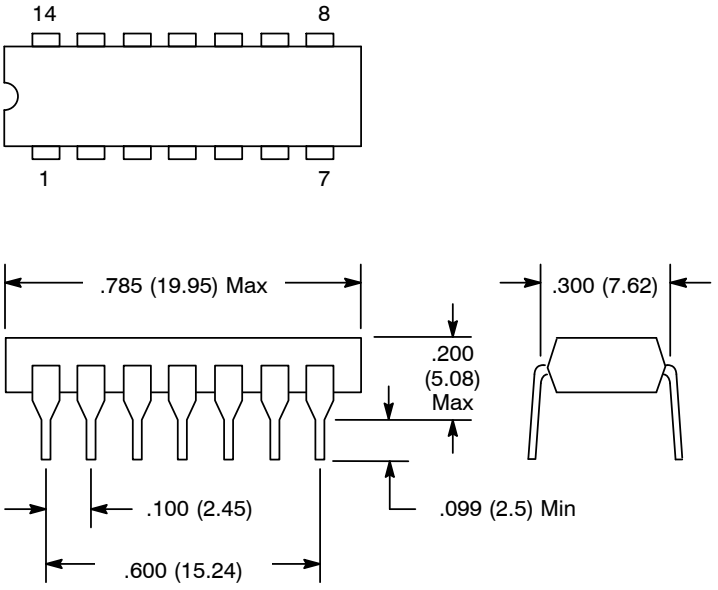
Logic Diagram



Pin14 = V_{CC}
Pin7 = GND

Pin Connection Diagram





DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4511
BCD to 7-segment
latch/decoder/driver

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

BCD to 7-segment latch/decoder/driver 74HC/HCT4511

FEATURES

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D_1 to D_4), an active LOW latch enable input ($\overline{LE}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH segment outputs (Q_a to Q_g).

When $\overline{LE}$ is LOW, the state of the segment outputs (Q_a to Q_g) is determined by the data on D_1 to D_4.
When $\overline{LE}$ goes HIGH, the last data present on D_1 to D_4 are stored in the latches and the segment outputs remain stable.
When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

APPLICATIONS

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	D_n to Q_n		24	24	ns
	$\overline{LE}$ to Q_n		23	24	ns
	$\overline{BI}$ to Q_n		19	20	ns
	$\overline{LT}$ to Q_n		12	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	$\overline{LT}$	lamp test input (active LOW)
4	$\overline{BI}$	ripple blanking input (active LOW)
5	$\overline{LE}$	latch enable input (active LOW)
7, 1, 2, 6	D_1 to D_4	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q_a to Q_g	segments outputs
16	V_{CC}	positive supply voltage

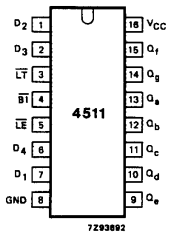


Fig.1 Pin configuration.

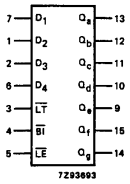


Fig.2 Logic symbol.

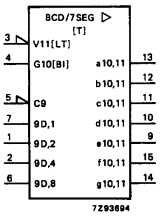


Fig.3 IEC logic symbol.

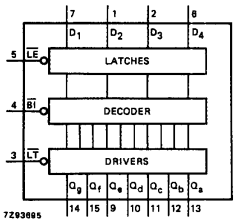


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_4	D_3	D_2	D_1	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	(1)							(1)

Note

1. Depends upon the BCD-code applied during the LOW-to-HIGH transition of $\overline{LE}$.
   H = HIGH voltage level
   L = LOW voltage level
   X = don't care

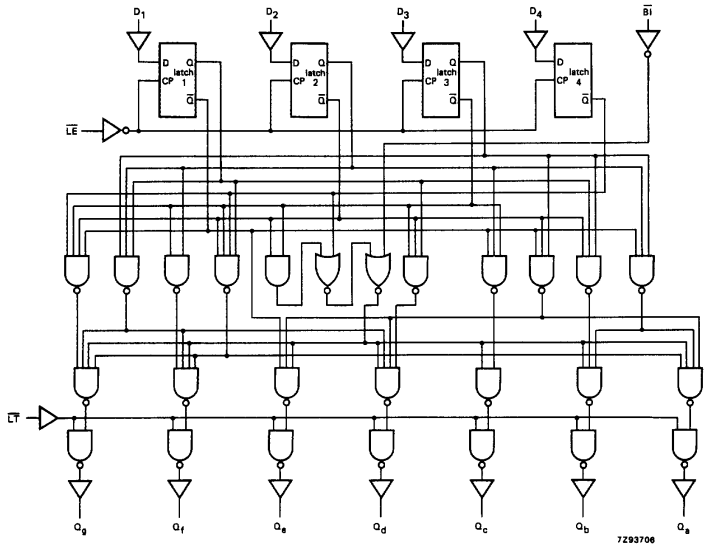


Fig.5 Logic diagram.

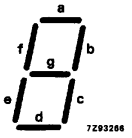


Fig.6 Segment designation.

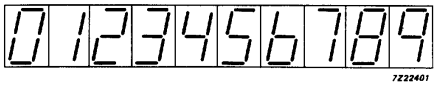


Fig.7 Display.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	$-I_O$ (mA)
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0
V_{OH}	HIGH level output voltage	5.60 5.48 4.80			5.45 5.34 4.50		5.35 5.20 4.20		V	6.0	V_{IH} or V_{IL}	7.5 10.0 15.0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		77 28 22	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BI}$ to Q_n		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time D_n to $\overline{LE}$	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.11
t_h	hold time D_n to $\overline{LE}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard, excepting V_{OH} which is given below
I_{CC} category: MSI

Non-standard DC characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT										
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	$-I_O$ (mA)
		min.	typ.	max.	min.	max.	min.	max.				
V_{OH}	HIGH level output voltage	3.98 3.60			3.84 3.35		3.70 3.10		V	4.5	V_{IH} or V_{IL}	7.5 10.0

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

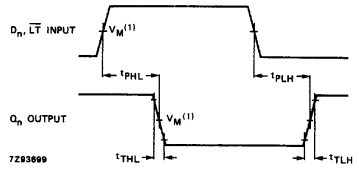
INPUT	UNIT LOAD COEFFICIENT
$\overline{LT}$, $\overline{LE}$	1.50
$\overline{BI}$, D_n	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

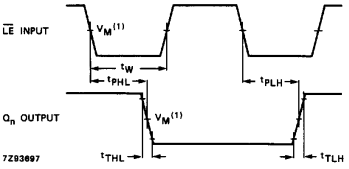
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		28	60		75		90	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{LE}$ to Q_n		27	54		68		81	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{BI}$ to Q_n		23	44		55		66	ns	4.5	Fig.10
t_{PHL}/ t_{PLH}	propagation delay $\overline{LT}$ to Q_n		16	30		38		45	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
t_W	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig.9
t_{su}	set-up time D_n to $\overline{LE}$	12	5		15		18		ns	4.5	Fig.11
t_h	hold time D_n to $\overline{LE}$	0	−4		0		0		ns	4.5	Fig.11

AC WAVEFORMS



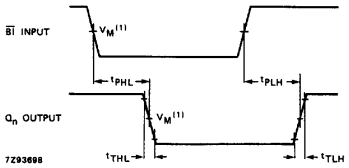
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the input (D_n, $\overline{LT}$) to output (Q_n) propagation delays and the output transition times.



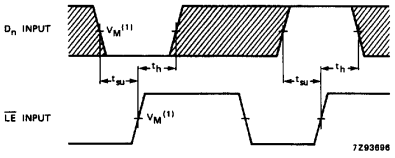
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the input ($\overline{LE}$) to output (Q_n) propagation delays and the latch enable pulse width.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing the input ($\overline{BI}$) to output (Q_n) propagation delays.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing the data set-up and hold times for D_n input to $\overline{LE}$ input.

APPLICATION DIAGRAMS

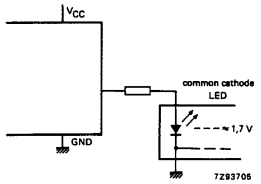


Fig.12 Connection to common cathode LED display readout.

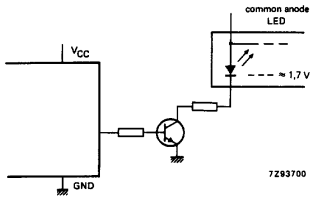
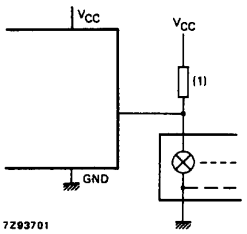


Fig.13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig.14 Connection to incandescent display readout.

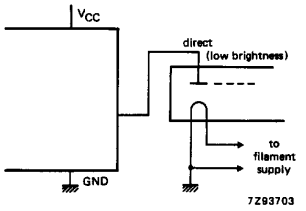


Fig.15 Connection to fluorescent display readout.

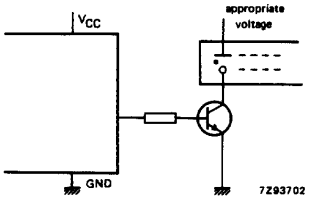


Fig.16 Connection to gas discharge display readout.

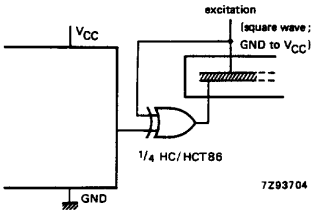


Fig.17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748−5089
http://www.nteinc.com

NTE4049, NTE4049T
NTE4050B, NTE4050BT
Integrated Circuit
CMOS, Hex Buffer/Converter

Description:

The NTE4049/NTE4049T (Inverting) and NTE4050B/NTE4050BT (Non−Inverting) are Hex Buffers and feature logic−level conversion using only one supply voltage (V_{DD}). The input−signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads (V_{DD} = 5V, $V_{OL} \le$ 400mV, $I_{OL} \ge$ 3.2mA).

These devices are available in a standard 16−Lead DIP (NTE4049 and NTE4050B) and SOIC−16 surface mount (NTE4049T and NTE4050BT) type packages.

Features:

- High Sink Current for Driving 2 TTL Loads
- High−to−Low Level Logic Conversion
- Quiescent Current Specified to 20V
- Maximum Input Current of 1μA at 18V (Full Package Temperature Range)
- High “Sink” and “Source” Current Capability
- 5V, 10V, and 15V Parametric Ratings

Absolute Maximum Ratings:

Supply Voltage (Note 1), V_{DD} . . . . . −0.5 to 20V
Input Voltage, V_I . . . . . −0.5 to V_{DD} +0.5V
DC Input Current (Any One Input), I_I . . . . . ±10mA
Total Power Dissipation, P_{tot}
  Per Package 200mW
  Per Output Transistor (T_{op} = −40° to +85°C) 100mW
Operating Temperature Range, T_{opr} . . . . . −40° to +85°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C

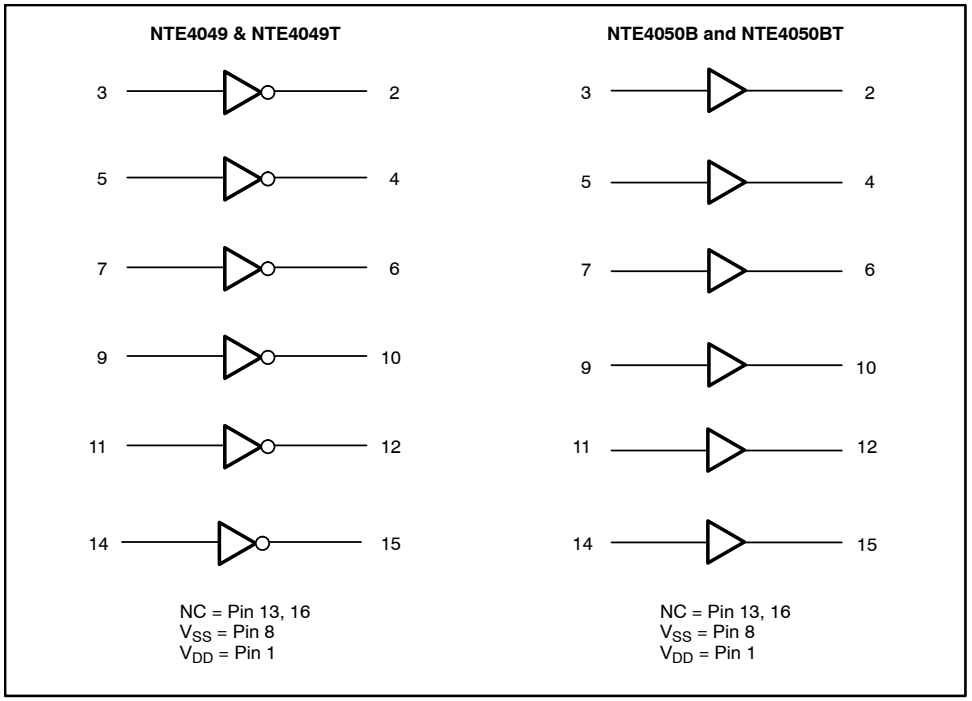
Note 1. All voltage values are referred to V_{SS} pin voltage.

Recommended Operating Conditions:

Supply Voltage, V_{DD} . . . . . 3 to 18V
Input Voltage (Note 2), V_I . . . . . V_{DD} to 18V
Operating Temperature Range, T_{opr} . . . . . −40° to +85°C

Note 2. The NTE4049/T and NTE4050B/BT have high−to−low−level voltage conversion capability but not low−to−high−level; therefore it is recommended that $V_{IN} \ge V_{DD}$.

Rev. 4−15



Static Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
		V_I (V)	V_O (V)	V_{DD} (V)				
Quiescent Supply Current	I_L	0 to 5	–	5	–	0.02	–	μA
		0 to 10	–	10	–	0.02	–	μA
		0 to 15	–	15	–	0.02	–	μA
		0 to 20	–	20	–	0.04	–	μA
Output High Voltage	V_{OH}	0 to 5	–	5	4.95	–	–	V
		0 to 10	–	10	9.95	–	–	V
		0 to 15	–	15	14.95	–	–	V
Input High Voltage NTE4049, NTE4049T	V_{IH}	–	0.5	5	4	–	–	V
		–	1.0	10	8	–	–	V
		–	2.0	15	12	–	–	V
NTE4050B, NTE4050BT		–	4.5	5	3.5	–	–	V
		–	9.0	10	7.0	–	–	V
		–	13.5	15	11.0	–	–	V

Static Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
		V_I (V)	V_O (V)	V_{DD} (V)				
Input Low Voltage NTE4049, NTE4049T	V_{IL}	–	4.5	5	–	–	1	V
		–	9.0	10	–	–	2	V
		–	13.0	15	–	–	3	V
NTE4050B, NTE4050BT		–	0.5	5	–	–	1.5	V
		–	1.0	10	–	–	3.0	V
		–	1.5	15	–	–	4.0	V
Output Drive Current	I_{OH}	0 to 5	2.5	5	–6.0	–6.4	–	mA
		0 to 5	4.6	5	–3.2	–1.6	–	mA
		0 to 10	9.5	10	–0.8	–3.6	–	mA
		0 to 15	13.5	15	–1.8	–12.0	–	mA
Output Sink Current	I_{OL}	0 to 5	0.4	4.5	2.6	5.2	–	mA
		0 to 5	0.4	5	3.2	6.4	–	mA
		0 to 10	0.5	10	8.0	16.0	–	mA
		0 to 15	1.5	15	24.0	48.0	–	mA
Input Leakage Current	I_{IH}, I_{IL}	0 to 18	Any Input	18	–	$\pm10^{-5}$	±0.1	μA
Input Capacitance NTE4049, NTE4049T	C_I	Any Input		–	–	15	22.5	pF
NTE4050B, NTE4050BT					–	5	7.5	pF

Note 3. The Noise Margin (NTE4050B/BT Only) for both "1" and "0" level is:1V min. with V_{DD} =5V
2V min. with V_{DD} =10V
2.5V min. with V_{DD} =15V

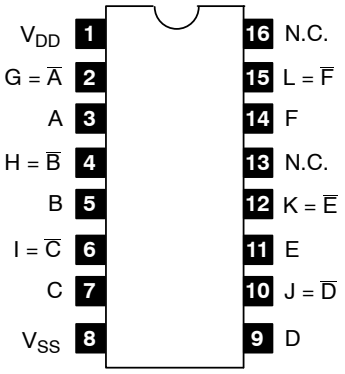
Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		V_I (V)	V_{DD} (V)				
Propagation Delay Time NTE4049, NTE4049T	t_{PLH}	5	5	–	60	120	ns
		10	10	–	32	65	ns
		10	5	–	45	90	ns
		15	15	–	25	590	ns
		15	5	–	45	90	ns
NTE4050B, NTE4050BT		5	5	–	70	140	ns
		10	10	–	40	80	ns
		10	5	–	45	90	ns
		15	15	–	30	60	ns
		15	5	–	40	80	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20ns unless otherwise specified)

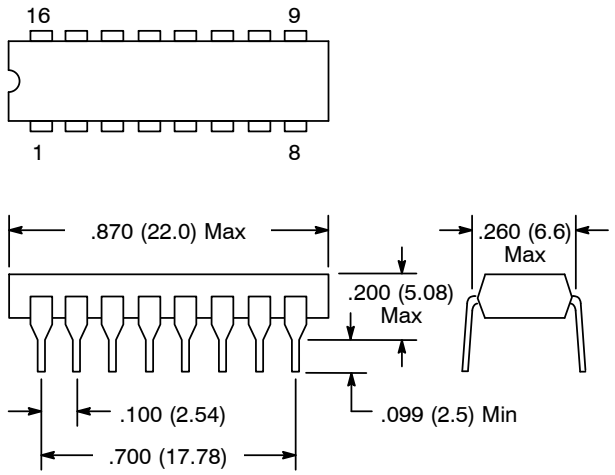
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		V_I (V)	V_{DD} (V)				
Propagation Delay Time NTE4049, NTE4049T	t_{PHL}	5	5	–	32	65	ns
		10	10	–	20	40	ns
		10	5	–	15	30	ns
		15	15	–	15	30	ns
		15	5	–	10	20	ns
NTE4050B, NTE4050BT		5	5	–	55	110	ns
		10	10	–	22	55	ns
		10	5	–	50	100	ns
		15	15	–	15	30	ns
		15	5	–	50	100	ns
Transition Time	t_{TLH}	5	5	–	80	160	ns
		10	10	–	40	80	ns
		15	15	–	30	60	ns
Transition Time	t_{THL}	5	5	–	30	60	ns
		10	10	–	20	40	ns
		15	15	–	15	30	ns

Pin Connection Diagram

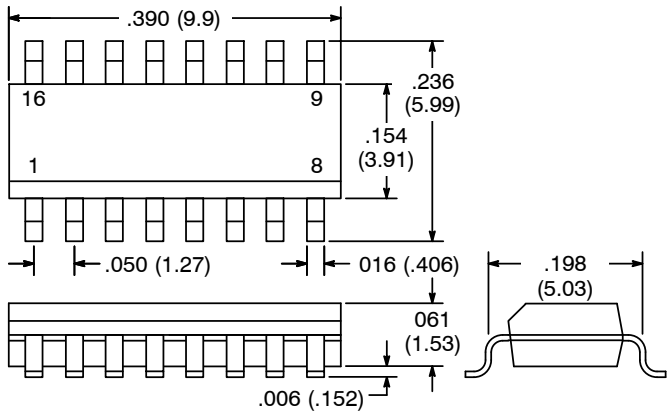


Note: On NTE4050B/BT, Pins 2, 4, 6, 10, 12, and 15 are not inverted.

NTE4049 / **NTE4050B**



NTE4049T / **NTE4050BT**



NOTE: Pin1 on Beveled Edge

SDLS037

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

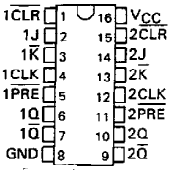
The SN54109 and SN54LS109A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74109 and SN74LS109A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

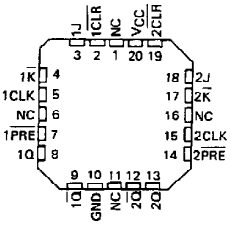
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

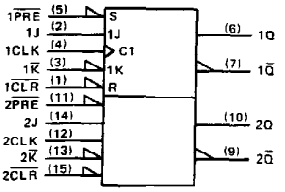
SN54109, SN54LS109A . . . J OR W PACKAGE
SN74109 . . . N PACKAGE
SN74LS109A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS109A . . . FK PACKAGE
(TOP VIEW)



logic symbol‡



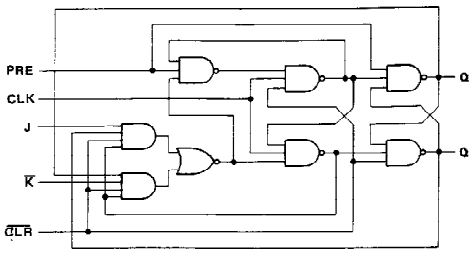
‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

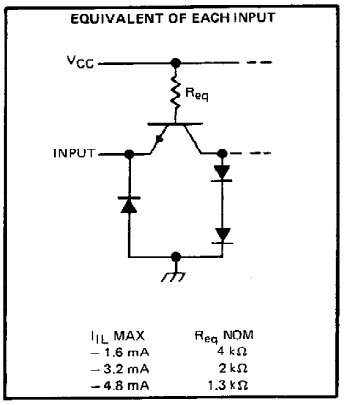
logic diagram (positive logic)

'109

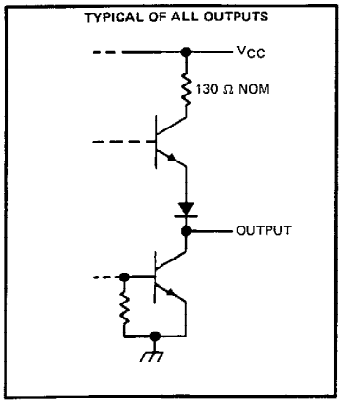


schematics of inputs and outputs

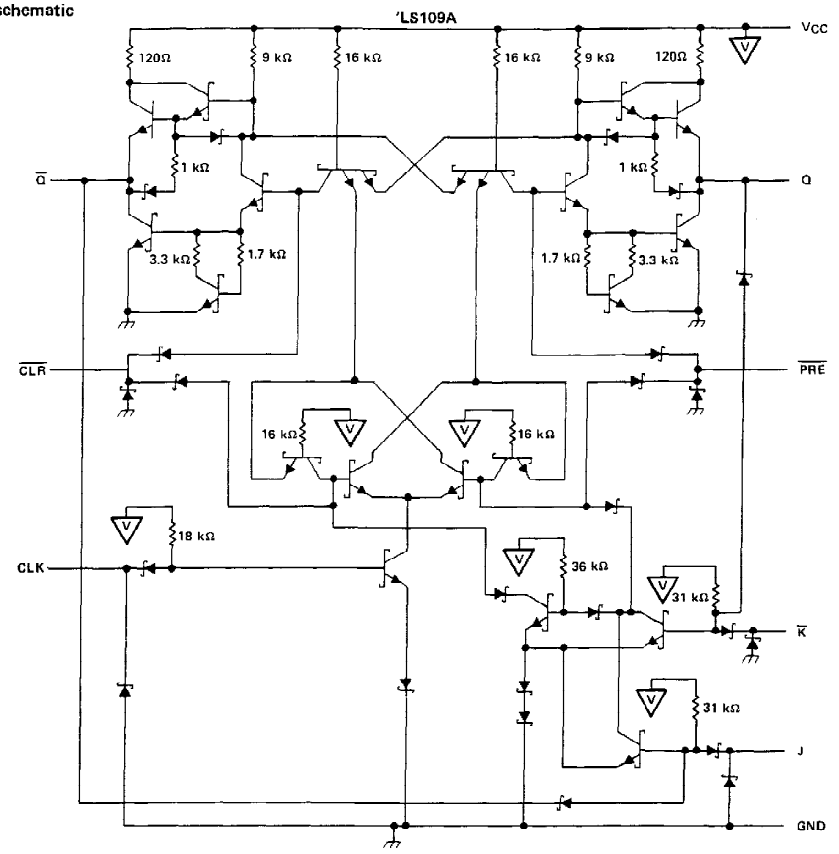
'109



I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ
−4.8 mA	1.3 kΩ



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '109 . . . . . 5.5 V
'LS109A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54109			SN74109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.8			−0.8	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high or low	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	20			20			
t_{su}	Input setup time before CLK↑		10			10			ns
t_h	Input hold time-data after CLK↑		6			6			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54109			SN74109			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.8 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J or $\overline{K}$	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	$\overline{CLR}$						160			160	
	$\overline{PRE}$ or CLK						80			80	
I_{IL}	J or $\overline{K}$	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	$\overline{CLR}$¶						−4.8			−4.8	
	$\overline{PRE}$¶						−3.2			−3.2	
	CLK						−3.2			−3.2	
I_{OS}§		V_{CC} = MAX			−30		−85	−30		−85	mA
I_{CC}#		V_{CC} = MAX,	See Note 2			9	15		9	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
¶ Clear is tested with preset high and preset is tested with clear high.
# Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{PRE}$	Q			10	15	ns
t_{PHL}		$\overline{Q}$			23	35	ns
t_{PLH}	$\overline{CLR}$	$\overline{Q}$			10	15	ns
t_{PHL}		Q			17	25	ns
t_{PLH}	CLK	Q or $\overline{Q}$			10	16	ns
t_{PHL}					18	28	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54LS109A			SN74LS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK ↑	High-level data	35			35			ns
		Low-level data	25			25			
t_h	Hold time-data after CLK ↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS109A			SN74LS109A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	J, $\overline{K}$ or CLK	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.2			0.2	
I_{IH}	J, $\overline{K}$ or CLK	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$						40			40	
I_{IL}	J, $\overline{K}$ or CLK	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$						−0.8			−0.8	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2			4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGE OPTION ADDENDUM

25-Mar-2023

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	Samples
JM38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	Samples
JM38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	Samples
M38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	Samples
M38510/30109BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BEA	Samples
M38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	Samples
M38510/30109BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30109BFA	Samples
SN54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS109AJ	Samples
SN54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS109AJ	Samples
SN74LS109AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	Samples
SN74LS109AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	Samples
SN74LS109ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	Samples
SN74LS109ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS109A	Samples
SN74LS109AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	Samples
SN74LS109AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	Samples
SN74LS109ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	Samples
SN74LS109ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS109AN	Samples
SN74LS109ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS109A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS109ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS109A	Samples
SNJ54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AJ	Samples
SNJ54LS109AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AJ	Samples
SNJ54LS109AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AW	Samples
SNJ54LS109AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS109AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "–" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS109A, SN74LS109A :

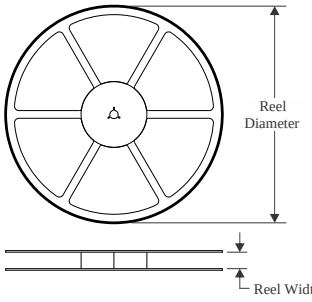
- Catalog : SN74LS109A
- Military : SN54LS109A

NOTE: Qualified Version Definitions:

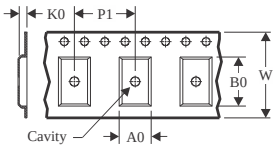
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

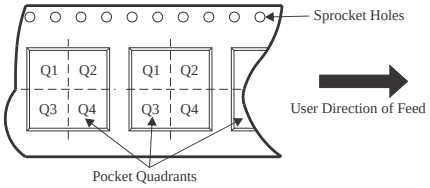


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

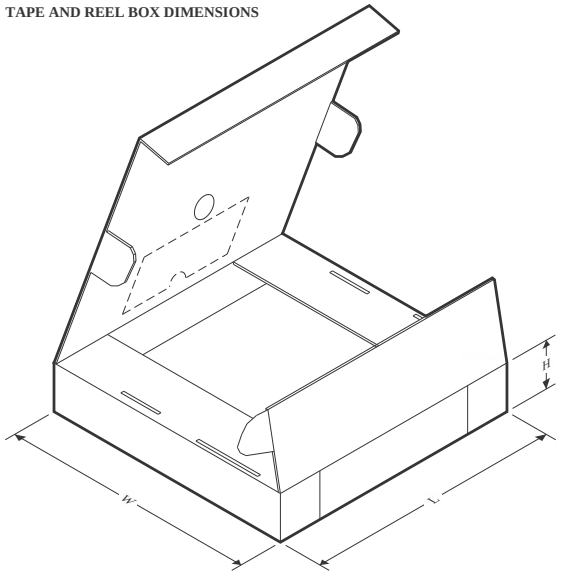
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS109ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS109ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

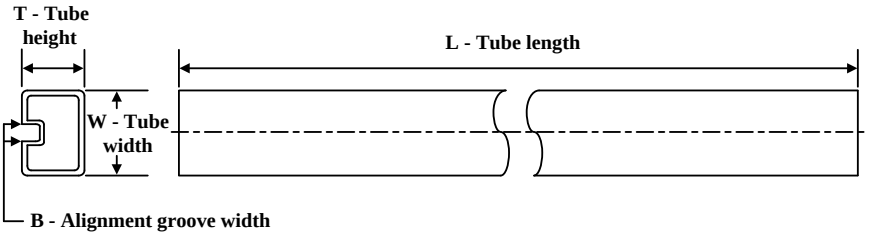
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS109ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS109ANSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
JM38510/30109BFA	W	CFP	16	1	506.98	26.16	6220	NA
M38510/30109BFA	W	CFP	16	1	506.98	26.16	6220	NA
SN74LS109AD	D	SOIC	16	40	507	8	3940	4.32
SN74LS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS109ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS109AW	W	CFP	16	1	506.98	26.16	6220	NA

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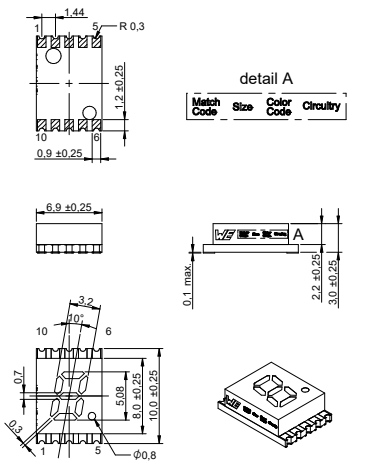
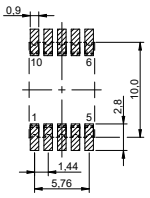
Dimensions: [mm]



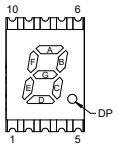
Scale - 2,5:1

Recommended Land Pattern: [mm]



Scale - 2,5:1

Segments Feature & Pin Position:



Scale - 3:1

Absolute Maximum Ratings (Ambient Temperature 25°C):

Properties		Test conditions	Value	Unit
Power Dissipation	P_{Diss}		68	mW
Peak Forward Current	$I_{F\ Peak}$	duty/ 10 @ 1 kHz	100	mA
Continuous Forward Current	I_F		20	mA
Reverse Voltage	V_{REV}		5	V
ESD Threshold/ Human Body Model	$V_{ESD\ HBM}$		1000	V

Optical Properties:

Chip Technology	InGaN
Emitting Color	Blue
Surface Color	Grey
Segment Color	Milky
Circuitry	Common Cathode

General Information:

Operating Temperature	-35 up to +85 °C
Storage Conditions (for single parts)	-35 up to +85 °C
Storage Conditions (in original packaging)	< 40 °C ; < 90 % RH
Moisture Sensitivity Level (MSL)	3

Product Marking:

Marking Matchcode	S7DS
Marking Size	020
Marking Color-Code	B
Marking Circuitry	C
Marking - Lot Number	Lot number

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CHECKED	REVISION	DATE (YYYY-MM-DD)	GENERAL TOLERANCE	PROJECTION METHOD
PLD	001.000	2022-03-04	DIN ISO 2768-1m	

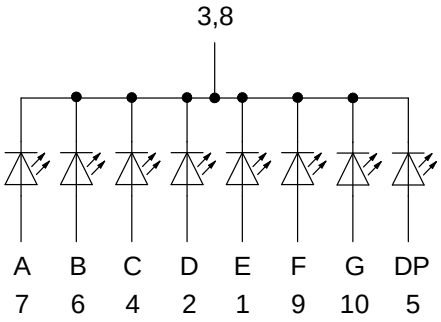
DESCRIPTION: **WL-S7DS 7 Segments Display SMT Single Digit**

ORDER CODE: **157102B12700**

SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0,2"	ePal	Valid	1/10

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc.. Würth Elektronik eiSos GmbH & Co KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance.

Schematic:



Pin Connection:

Pin No	Connection
1	Anode E
2	Anode D
3	Common cathode
4	Anode C
5	Anode DP
6	Anode B
7	Anode A
8	Common cathode
9	Anode F
10	Anode G

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PLD	001.000	2022-03-04	DIN ISO 2768-1m	

DESCRIPTION
WL-S7DS 7 Segments Display SMT Single Digit

ORDER CODE
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SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0.2"	ePal	Valid	2/10

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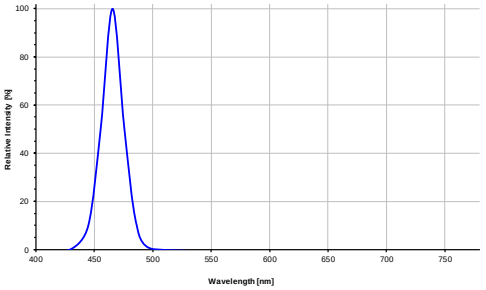
Electrical & Optical Properties:

Properties		Test conditions	Value			Unit
			min.	typ.	max.	
Dominant Wavelength	λ_{Dom}	20 mA		465		nm
Luminous Intensity	I_V	10 mA		15		mcd
Luminous Intensity	I_V	20 mA		24		mcd
Forward Voltage	V_F	20 mA		3	3.4	V
Spectral Bandwidth	$\Delta\lambda$	20 mA		20		nm
Reverse Current	I_{REV}	5 V			5	µA
Luminous Intensity Matching Ratio		10 mA		2:1		

Certification:

RoHS Approval	Compliant [2011/65/EU&2015/863]
REACh Approval	Conform or declared [(EC)1907/2006]
Halogen Free	Conform [IEC 61249-2-21]
Halogen Free	Conform [JEDEC JS709B]

Spectral:



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PLD	001.000	2022-03-04	DIN ISO 2768-1m	

DESCRIPTION
WL-S7DS 7 Segments Display
SMT Single Digit

ORDER CODE
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SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0.2"	ePal	Valid	3/10

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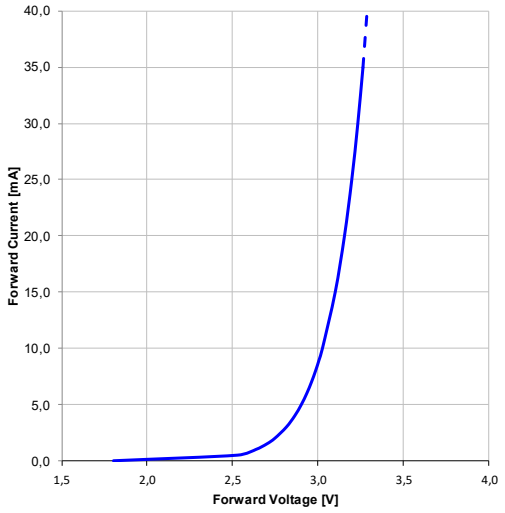
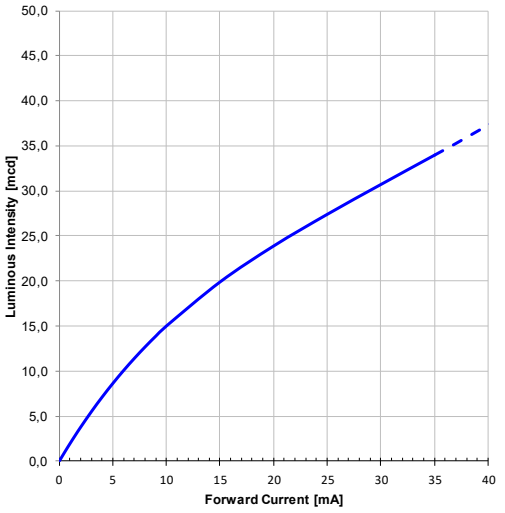
Forward Current vs. Forward Voltage:



Luminous Intensity vs. Forward Current:



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WL-S7DS 7 Segments Display
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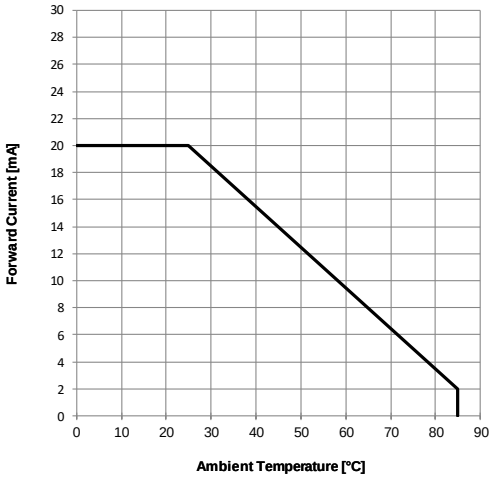
Derating Curve:



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SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0.2"	ePal	Valid	5/10

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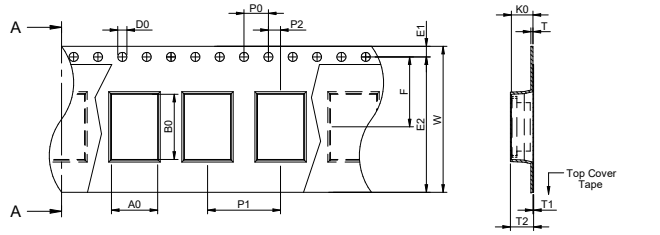
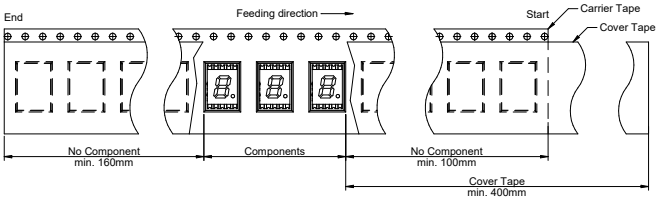
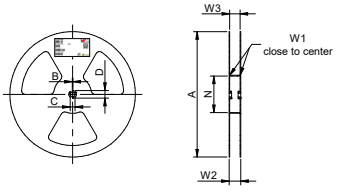
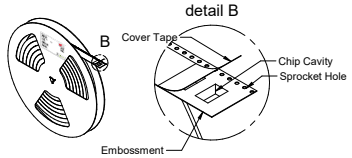
Packaging Specification - Tape: [mm]





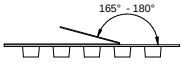




	A (mm)	B (mm)	C (mm)	D (mm)	N (mm)	W1 (mm)	W2 (mm)	W3 (mm)	W3 (mm)	Material
Tolerance	± 2,0	min.	min.	min.	min.	+ 2,0	max.	min.	max.	
Value	330,00	1,50	12,80	20,20	60,00	24,40	30,40	23,90	27,40	Polystyrene

Packaging is referred to the international standard **IEC 60286-3:2019**

	Tape Type	A0 (mm)	B0 (mm)	W (mm)	T (mm)	T1 (mm)	T2 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	D0 (mm)	D1 (mm)	E1 (mm)	E2 (mm)	F (mm)	Material	Qty. (pcs.)
Tolerance		typ.	typ.	+0,3/ -0,1	ref.	ref.	typ.	typ.	±0,1	±0,1	±0,1	+0,1/ -0,0	min.	±0,1	min.	±0,1		
Value	2a	7,60	10,70	24,00	0,35	0,10	3,50	3,25	4,00	12,00	2,00	1,50	1,50	1,75	22,25	11,50	Polystyrene	1500



Tape width	24 mm	Pull-of force 0,1 N - 1,3 N

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PLD	001.000	2022-03-04	DIN ISO 2768-1m	

DESCRIPTION
WL-S7DS 7 Segments Display
SMT Single Digit

ORDER CODE
157102B12700

SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0,2"	ePal	Valid	6/10

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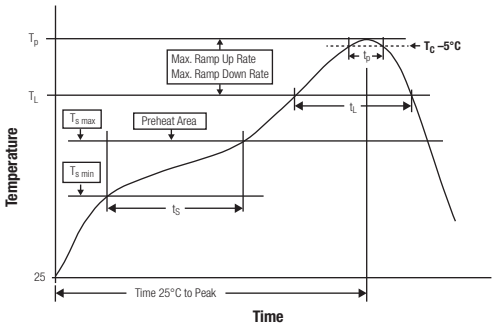
Classification Reflow Profile for SMT components:



Classification Reflow Soldering Profile:

Profile Feature		Value
Preheat Temperature Min	$T_{s\,min}$	150 °C
Preheat Temperature Max	$T_{s\,max}$	200 °C
Preheat Time t_s from $T_{s\,min}$ to $T_{s\,max}$	t_s	max. 60 - 120 seconds
Ramp-up Rate (T_L to T_P)		3 °C/ second max.
Liquidous Temperature	T_L	217 °C
Time t_L maintained above T_L	t_L	max. 60 seconds
Peak package body temperature	T_p	$T_p \leq T_c$, see Table below
Time within 5°C of actual peak temperature	t_p	max. 10 seconds
Ramp-down Rate (T_P to T_L)		6 °C/ second max.
Time 25°C to peak temperature		max. 220 seconds

refer to IPC/ JEDEC J-STD-020E

Package Classification Reflow Temperature (T_c):

Properties	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
PB-Free Assembly I Package Thickness < 1.6 mm	260 °C	260 °C	260 °C
PB-Free Assembly I Package Thickness 1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
PB-Free Assembly I Package Thickness > 2.5 mm	250 °C	245 °C	245 °C
Applied cycles	2 cycles max.		

refer to IPC/ JEDEC J-STD-020E

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SIZE/TYPE	BUSINESS UNIT	STATUS	PAGE
0.2"	ePal	Valid	7/10

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc.. Würth Elektronik eiSos GmbH & Co KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance.

Cautions and Warnings:

The following conditions apply to all goods within the product series of Optoelectronic Components of Würth Elektronik eiSos GmbH & Co. KG:

General:

- This optoelectronic component is designed and manufactured for use in general electronic equipment.
- Würth Elektronik must be asked for written approval (following the PPAP procedure) before incorporating the components into any equipment in fields such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network, etc. where higher safety and reliability are especially required and/or if there is the possibility of direct damage or human injury.
- Optoelectronic components that will be used in safety-critical or high-reliability applications, should be pre-evaluated by the customer.
- The optoelectronic component is designed and manufactured to be used within the datasheet specified values. If the usage and operation conditions specified in the datasheet are not met, the wire insulation may be damaged or dissolved.
- Do not drop or impact the components, the component may be damaged
- Würth Elektronik products are qualified according to international standards, which are listed in each product reliability report. Würth Elektronik does not warrant any customer qualified product characteristics beyond Würth Elektroniks' specifications, for its validity and sustainability over time.
- The responsibility for the applicability of the customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products also apply to customer specific products.

Product specific:

Soldering:

- The solder profile must comply with the technical product specifications. All other profiles will void the warranty.
- All other soldering methods are at the customers' own risk.

Cleaning and Washing:

- Washing agents used during the production to clean the customer application might damage or change the characteristics of the optoelectronic component body, marking or plating. Washing agents may have a negative effect on the long-term functionality of the product.
- Using a brush during the cleaning process may break the optoelectronic component body. Therefore, we do not recommend using a brush during the PCB cleaning process.

Potting:

- If the product is potted in the customer application, the potting material might shrink or expand during and after hardening. Shrinking could lead to an incomplete seal, allowing contaminants into the optoelectronic component body, pins or termination. Expansion could damage the components. We recommend a manual inspection after potting to avoid these effects.

Storage Conditions:

- A storage of Würth Elektronik products for longer than 12 months is not recommended. Within other effects, the terminals may suffer degradation, resulting in bad solderability. Therefore, all products shall be used within the period of 12 months based on the day of shipment.
- Do not expose the optoelectronic component to direct sunlight.
- The storage conditions in the original packaging are defined according to DIN EN 61760-2.
- For a moisture sensitive component, the storage condition in the original packaging is defined according to IPC/JEDEC-J-STD-033. It is also recommended to return the optoelectronic component to the original moisture proof bag and reseal the moisture proof bag again.
- The storage conditions stated in the original packaging apply to the storage time and not to the transportation time of the components.

Packaging:

- The packaging specifications apply only to purchase orders comprising whole packaging units. If the ordered quantity exceeds or is lower than the specified packaging unit, packaging in accordance with the packaging specifications cannot be ensured.

Handling:

- Violation of the technical product specifications such as exceeding the nominal rated current, will void the warranty.
- The product design may influence the automatic optical inspection.
- Certain optoelectronic component surfaces consist of soft material. Pressure on the top surface has to be handled carefully to prevent negative influence to the function and reliability of the optoelectronic components.
- ESD prevention methods need to be applied for manual handling and processing by machinery.
- Resistors for protection are obligatory.
- Luminaires in operation may harm human vision or skin on a photo-biological level. Therefore direct light impact shall be avoided. All products are additionally certified as risk groups 0 to 2 according to DIN EN 62471:2008.
- In addition to optoelectronic components testing, products incorporating these devices have to comply with the safety precautions given in IEC 60825-1, IEC 62471 and IEC 62778
- Please be aware that Products provided in bulk packaging may get bent and might lead to derivations from the mechanical manufacturing tolerances mentioned in our datasheet, which is not considered to be a material defect.

Technical specification:

- The typical and/or calculated values and graphics of technical parameters can only reflect statistical figures. The actual parameters of each single product, may differ from the typical and/or calculated values or the typical characteristic line.
- On each reel, only one bin is sorted and taped. The bin is defined on intensity, chromaticity coordinate or wavelength and forward

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voltage.

- In order to ensure highest availability, the reel binning of standard deliveries can vary. A single bin cannot be ordered. Please contact us in advance, if you need a particular bin sorting before placing your order.
- Test conditions are measured at the typical current with pulse duration < 30ms.
- Wavelength tolerance under measurement conditions ± 2nm.
- Optical intensity tolerance under measurement conditions ±15%.
- Forward voltage tolerance under measurement conditions ± 0.2V.

These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

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Important Notes

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component. Therefore, customer is cautioned to verify that data sheets are current before placing orders. The current data sheets can be downloaded at www.we-online.com.

3. Best Care and Attention

Any product-specific notes, cautions and warnings must be strictly observed. Any disregard will result in the loss of warranty.

4. Customer Support for Product Specifications

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights

All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions

Unless otherwise agreed in individual contracts, all orders are subject to the current version of the "General Terms and Conditions of Würth Elektronik eiSos Group", last version available at www.we-online.com.

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

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157102B12700

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT238
3-to-8 line decoder/demultiplexer

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

3-to-8 line decoder/demultiplexer 74HC/HCT238

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).
The "238" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be LOW unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	A_n to Y_n		14	18	ns
	E_3 to Y_n		16	20	ns
	$\overline{E}_n$ to Y_n		17	21	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	72	76	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

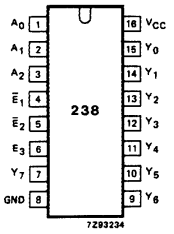


Fig.1 Pin configuration.

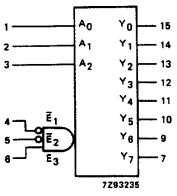
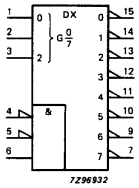
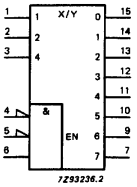


Fig.2 Logic symbol.



(a)



(b)

Fig.3 IEC logic symbol.

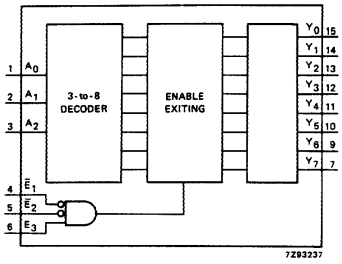


Fig.4 Functional diagram.

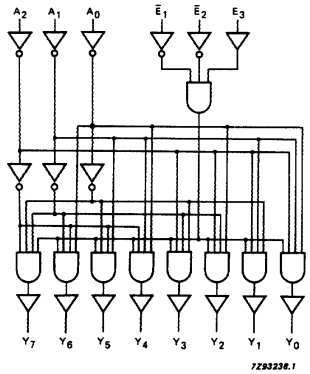


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to Y_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay E_3 to Y_n		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to Y_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.70
$\overline{E}_n$	0.40
E_3	1.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}	propagation delay A_n to Y_n		21	35		44		53	ns	4.5	Fig.6
t_{PLH}	propagation delay A_n to Y_n		17	35		44		53	ns	4.5	Fig.6
t_{PHL}	propagation delay E_3 to Y_n		22	37		46		56	ns	4.5	Fig.6
t_{PLH}	propagation delay E_3 to Y_n		18	37		46		56	ns	4.5	Fig.6
t_{PHL}	propagation delay $\overline{E}_n$ to Y_n		21	35		44		53	ns	4.5	Fig.7
t_{PLH}	propagation delay $\overline{E}_n$ to Y_n		18	35		44		53	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

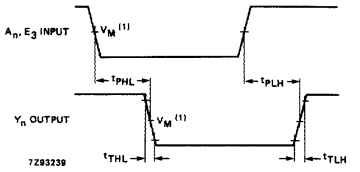


Fig.6 Waveforms showing the address input (A_n) and enable input (E_3) to output (Y_n) propagation delays and the output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

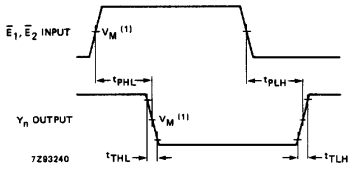


Fig.7 Waveforms showing the enable input ($\overline{E}_n$) to output (Y_n) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.