



UNIVERSITÀ
DEGLI STUDI
DI PADOVA



DIPARTIMENTO
DI INGEGNERIA
DELL'INFORMAZIONE

Implementazione della CPU Z80 su FPGA: un primo approccio

Scheda di sviluppo RUCS7

Z80 – Generalità e Storia

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Z80 – Informazioni
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Z80X – Implementazione su
FPGA

Z80X – Cicli di controllo

RUCS7 – Controllore via
UART

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Scheda di sviluppo RUCS7

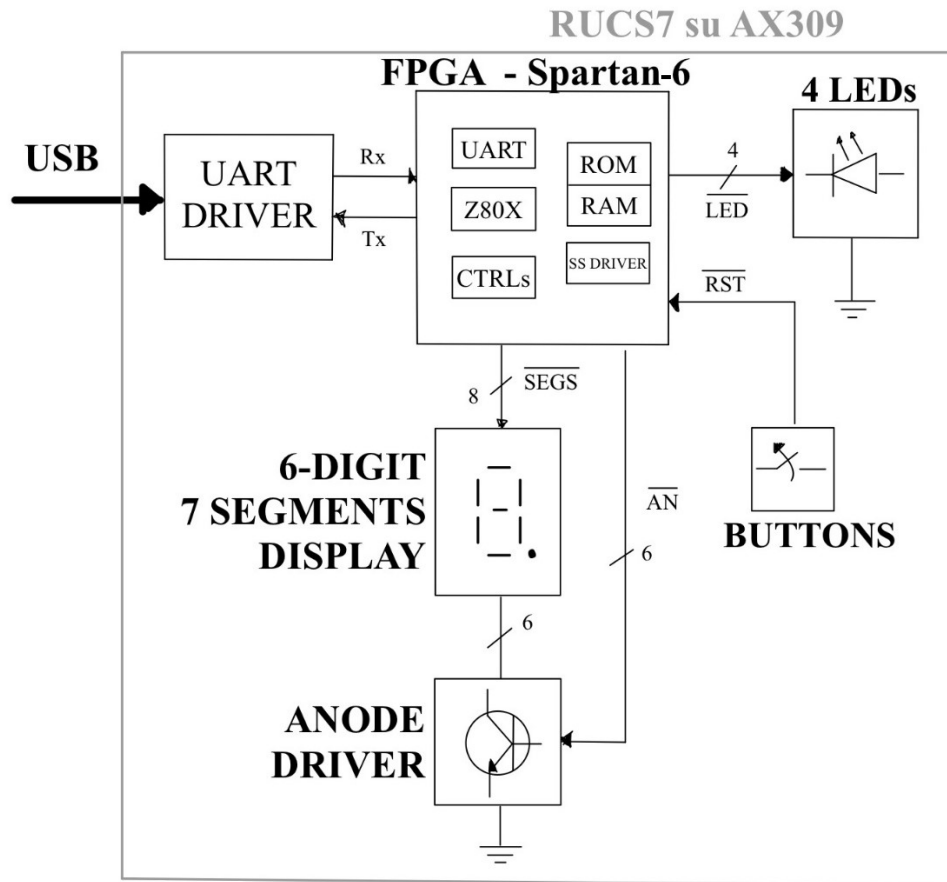


Figura 1 – Schema delle unità usate all'interno della scheda RUCS7

- Z80X - Implementazione comportamentale dello Z80
- Memorie e interfacce per far funzionare lo Z80X
- Sistema per programmare, controllare e fare il debug dello Z80X
- Controllore con interfaccia UART
- Driver per display 7-segmenti con buffer circolare e compatibile con ASCII

Z80 – Generalità e storia

The Battle of the 80's

Think of your next microcomputer as a weapon against horrendous inefficiencies, outrageous costs and antiquated speeds. We invite you to peruse this chart.

Features	8080A	Z80 CPU	Features	8080A	Z80 CPU
Power Supplies	+5, -5, +12	+5	Instructions	78	158*
Clock	24, +12 Volt	14.5 Volt	OP Codes	244	696
Standard Clock Speed	500 ns	400 ns	Addressing Modes	7	11
Interface	Requires 8225, 8208 & 8234	Requires no other logic and includes dynamic RAM Refresh	Working Registers	8	17
Interrupt	1 mode	3 modes; up to 6x faster	Throughput	Up to 5 times greater than the 8080A	
Non-maskable Interrupt	No	Yes	Program Memory Space	Generally 50% less than the 8080A	

*Including all of the 8080A's instructions.

Announcing Zilog Z-80 microcomputer products. With the next generation, the battle is joined.

The Z-80: A new generation LSI component set including CPU and I/O Controllers.

The Z-80: Full software support with emphasis on high-level languages.

The Z-80: A floppy disc-based development system with advanced real-time debug and in-circuit emulation capabilities.

The Z-80: Multiple sourcing available now.

On standby: User support.

Zilog conducts a wide range of strategic meetings and design oriented workshops to provide the know-how required to implement the Z-80 Microcomputer Product line into your design. All hardware software and the development system are thoroughly explained with "hands-on" experience in the classroom. Your Zilog representative can provide you with further details on our user support program.

Mighty weapons against an enemy entrenched: The Z-80 development system.

You'll be equipped with performance and versatility unmatched by any other microcomputer development system in the field. Thanks to a floppy disc operating system in alliance with a sophisticated Real-Time Debug Module.

Your ammunition: A chip off a new block.

A single chip, N-channel processor arms you with a super-set of 158 instructions that include all of the 8080A's 78 instructions with total software compatibility. The new instructions include 1, 4, 8 and 16-bit operations. And that means less programming time, less paper and less end costs.

And you'll be in command of powerful instructions: Memory-to-memory or memory-to-I/O block transfers and searches, 16-bit arithmetic, 8 types of rotates and shifts, bit manipulation and a legion of addressing modes. Along with this army you'll also get a standard instruction speed of 1.6 μ s and all Z-80 circuits require only a single 5V power supply and a single phase 5V clock. And you should know that a family of Z-80 programmable circuits allow for direct interface to a wide range of both parallel and serial interface peripherals and even dynamic memories without other external logic.

With these features, the Z80-CPU generally requires approximately 50% less memory space for program storage.

Reinforcements: A reserve of technological innovations.

The Zilog Z-80 brings to the battlefield new levels of performance and ease of programming not available in second generation systems. And while all the others busy themselves with overtaking the Z-80, we're busy on the next generation—continuing to demonstrate our pledge to stay a generation ahead.

The Z-80's troops are the specialists who were directly responsible for the development of the most successful first and second generation microprocessors. Nowhere in the field is there a corps of seasoned veterans with such a distinguished record of victory.

Signal us for help. We'll dispatch appropriate assistance.

On standby: Software support.

All this is supported by a contingent of software including: resident microcomputer software, time sharing programs, libraries and high-level languages such as PL/Z.

Zilog MICROCOMPUTERS
170 Shaw Street, Los Altos, California 94022
(415) 941-8055; Telex 160-370 ZPMS

Circle 33 on reader service card

AN AFFILIATE OF EXON ENTERPRISES INC.

Figura 2 – Pubblicità dello Z80 nel Maggio 1976

- Progettato da Federico Faggin e Masatoshi Shima
- In relazione con: Intel 4004, Intel 8008, Intel 8080
- Prodotto da Zilog nel 1976
- Singola alimentazione e singolo clock
- Compatibilità con Intel 8080
- Famiglia di periferiche dedicate

Z80 - Architettura

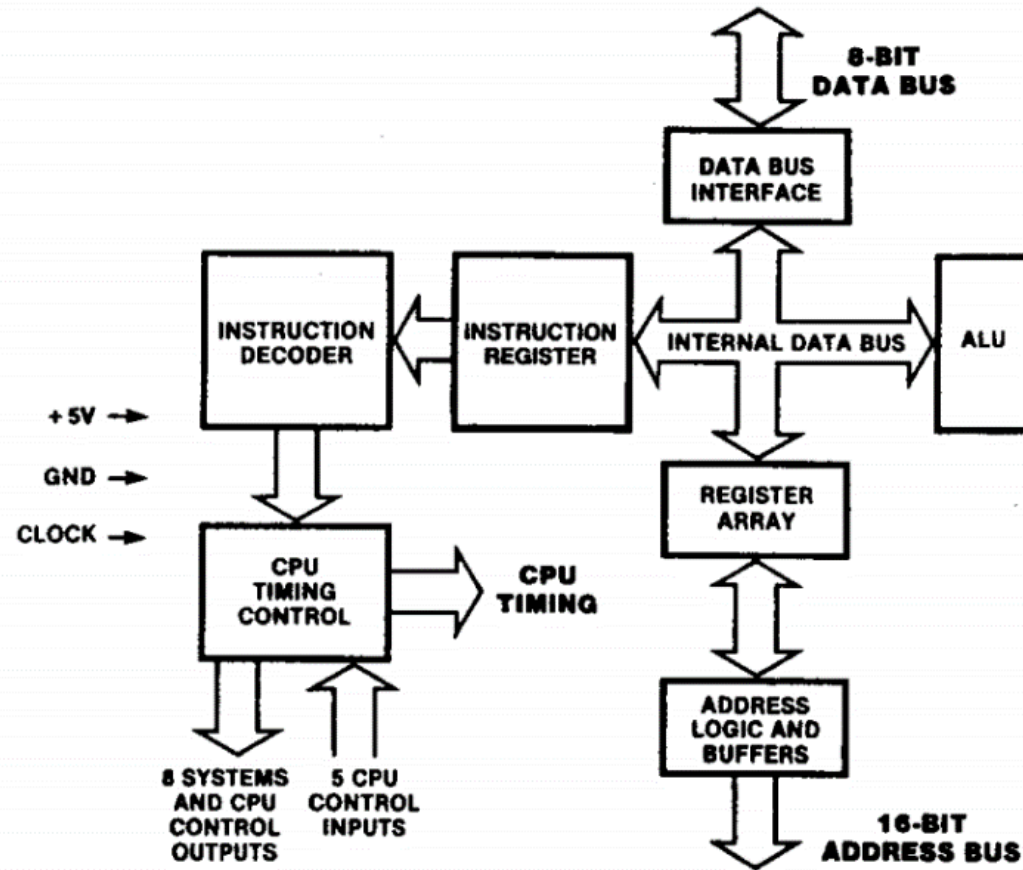


Figura 3 – Diagramma a blocchi dello Z80 dal datasheet

- 2 tipi di interrupt: NMI e INT
- 3 modalità di gestione degli interrupt
- Gestione BUS: BUSREQ
- 6 registri GP: B, C, D, E, H, L
- Registri ombra
- 2 registri d'indicizzazione: IX e IY
- Puntatore stack: SP
- Accumulatore e registro di stato
- Registri dedicati: I e R

Z80 - Informazioni sull'organizzazione

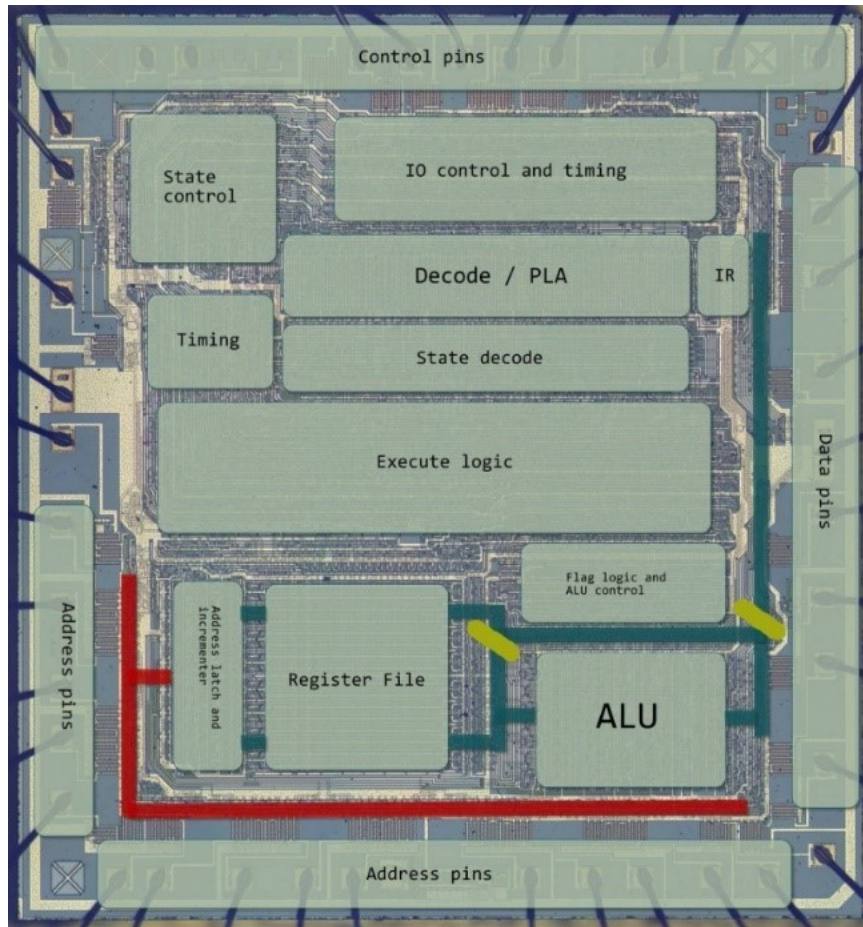


Figura 4 – Die dello Z80 con le unità operative

- ALU a 4 bit anziché 8: registri per i nibble e shift in ALU
- Incrementer/decrementer a 16 bit: PC e I-R, funzione di stop, CLA, 0001H detector
- Due set di registri identici per exchange e due registri d'appoggio
- 3 sezioni del bus a 8 bit
- Decoder basato su PLA e contatore M-cycles e T-cycles
- Comportamenti non documentati

Z80X – Implementazione su FPGA

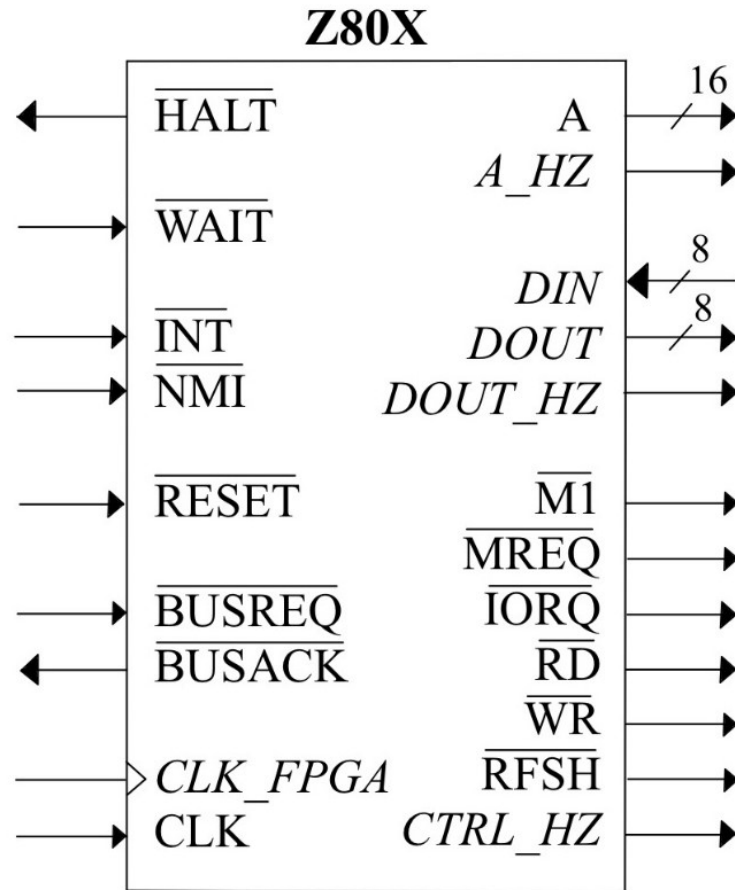
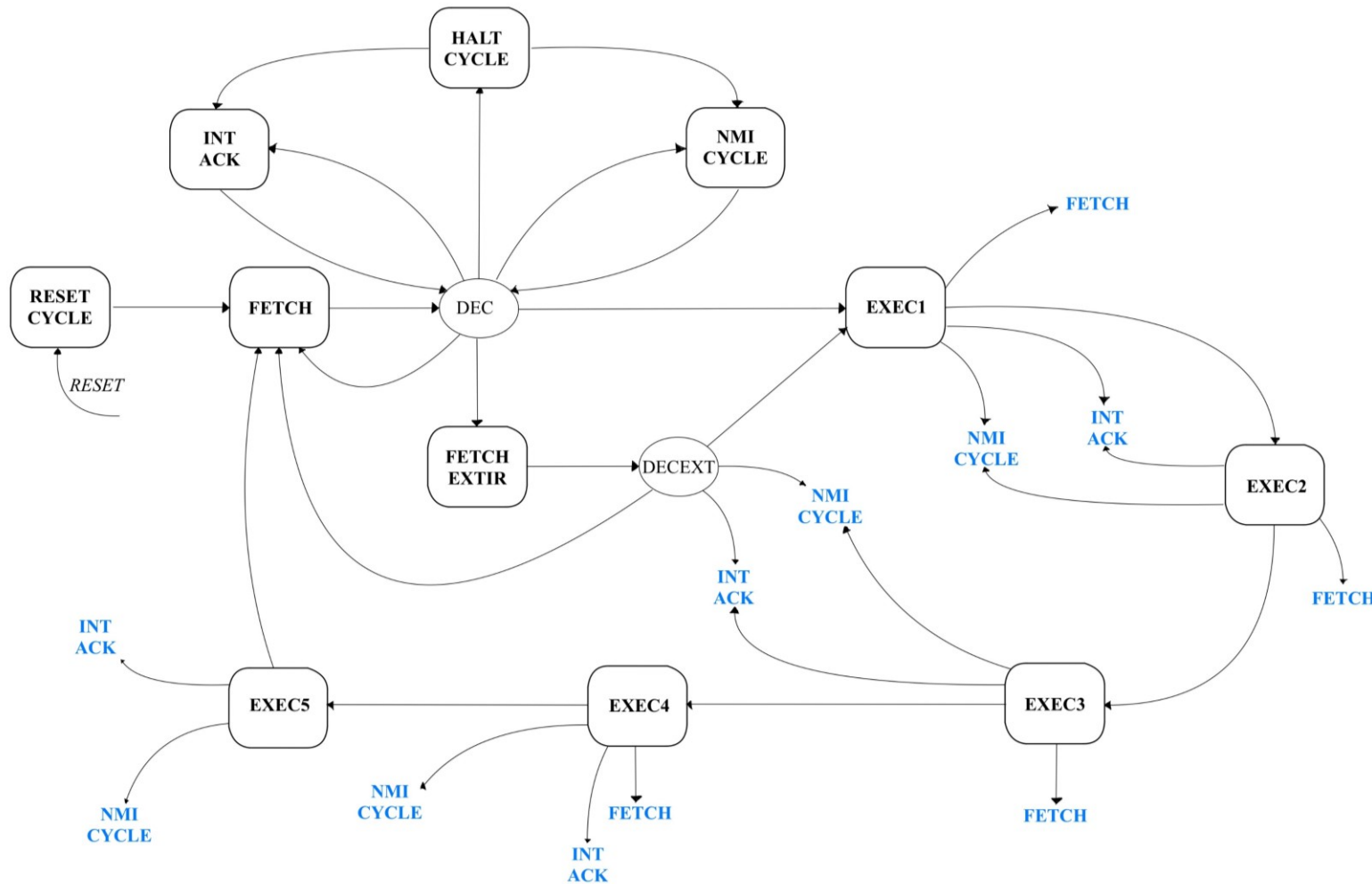


Figura 5 – Schema dell'entity Z80X

Sviluppato dal punto di vista comportamentale:

- Pin dedicati alla gestione 3-state
- Gestione Clock
- Bus dedicati a 8 e 16 bit
- Separazione e gestione registri
- ALU e inc/dec
- Sezione di controllo

Z80X – Cicli di controllo



- FSM Master per BUSREQ
- FSM annidate per il ciclo principale
- μ FSM dedicate: OPFET, MEMRDWR, IORDWR, INTRQ

Figura 6 – Diagramma di stato semplificato della FSM Main di Z80X

RUCS7 – Controllore via UART

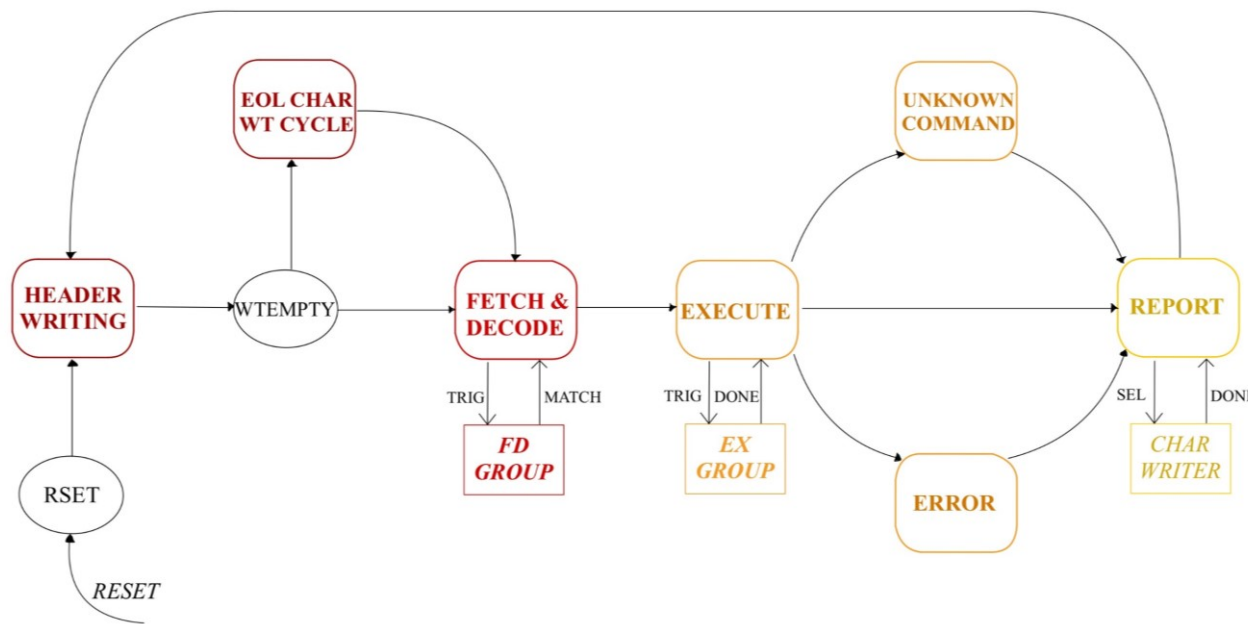


Figura 7 – Diagramma di stato semplificato della FSM di CMD_CTRL

- Realizzato come FSM annidate
- Due gruppi di sottomacchine:
 - FD
 - EX
- Comandi via UART:
 - R/W Memorie
 - Controllo generatore di Clock
 - Istantanee stato dello Z80X
 - Ciclo reset Z80X

Conclusioni

Problemi noti

- Rapporto fra le frequenze di CLK_FPGA e CLK
- OUTI istruzione difettiva
- DECODER richiede molte risorse

Sviluppi futuri

- Decoder basato su BRAM
- Interfaccia tastiera
- Interfaccia VGA
- Z80-DMA



Figura 8 – HP-35