Instruction	Original Instruction Code	Renamed Instruction Code	Entry added to Spec. Reg. Map	InQ	Issued	Completed	Committed	Commited Reg. Map	Reg Free List
1	L.D LR1 0(LR2)	L.D PR33, 0(PR2)	LR1 -> PR33	i	i + 1	i + 7	i + 7	LR1 -> PR33	PR1
2	DADD LR1, LR1, LR3	DADD PR34, PR33, PR3	LR1 -> PR34	i	i + 3	i + 8	i + 8	LR1 -> PR34	PR33
3	DADD LR1, LR1, LR1	DADD PR35, PR34, PR34	LR1 -> PR35	i	i + 4	i + 9	i + 9	LR1 -> PR35	PR34
4	ST.D LR1, 0(LR2)	ST.D PR35 0(PR2)		i + 1	i + 5	i + 11	i + 11		
5	DADD LR2, LR2, 8	DADD PR36, PR2, 8	LR2 -> PR36	i + 1	i + 1	i + 7	i + 11	LR2 -> PR36	PR2
6	BNE LR2, LR4, line1	BNE PR36, PR4, line1		i + 1	i + 2	i + 8	i + 11		
7	L.D LR1 0(LR2)	L.D PR37, 0(PR36)	LR1 -> PR37	i + 2	i + 2	i + 9	i + 12	LR1 -> PR37	PR35
8	DADD LR1, LR1, LR3	DADD PR38, PR37, PR3	LR1 -> PR38	i + 2	i + 4	i + 10	i + 12	LR1 -> PR38	PR37
9	DADD LR1, LR1, LR1	DADD PR1, PR38, PR38	LR1 -> PR1	i + 8	i + 9	i + 15	i + 15	LR1 -> PR1	PR38
10	ST.D LR1, 0(LR2)	ST.D PR1, 0(PR36)		i + 8	i + 10	i + 17	i + 17		
11	DADD LR2, LR2, 8	DADD PR2, PR36, 8	LR2 -> PR2	i + 9	i + 10	i + 16	i + 17	LR2 -> PR2	PR36
12	BNE LR2, LR4, line1	BNE PR2, PR4, line1		i + 9	i + 11	i + 17	i + 17		
	Legend		Assumptions		Answer to question				
	Waiting for free register		The processor has a width of 3 for fetch and issue		The 12th instruction commits in the 22nd cycle, i = 5.				
	Waiting to commit in order		32 LRs and 38 PRs						
	Commit witdth full		Perfect branch prediction						
	Fetch width full		Perfect fetch						