	add	addu	sub	subu	and	or	xor	nor	SLT (a<b 引 比较)
RSC[4:0]	order[25:21]	[25:21]			[25:21]	[25:21]	[25:21]	[25:21]	[25:21]
RTC[4:0]	[20:16]	[20:16]			[20:16]	[20:16]	[20:16]	[20:16]	[20:16]
M1	01	01			01	01	01	01	01
M2	01	01			01	01	01	01	01
M3	1	1			1	1	1	1	1
M4	0	0			0	0	0	0	0
M5	0	0			0	0	0	0	0
~~M6~~									
RDC[4:0]	[15:11]	[15:11]			[15:11]	[15:11]	[15:11]	[15:11]	[15:11]
RF_W	1	1			1	1	1	1	1
RF_clk	~clk	~clk			~clk	~clk	~clk	~clk	~clk
DM_CS	0	0			0	0	0	0	0
DM_W	0	0			0	0	0	0	0
DM_R	0	0			0	0	0	0	0
ALUC[4:0]	0010	0000	0011	0001	0100	0101	0110	0111	1011
31~26	000000	000000	000000	000000	000000	000000	000000	000000	000000
5~0	100000	100001	100010	100011	100100	100101	100110	100111	101010

rd ← rs AND rt

	SLTU	sll	srl	sra	sllv	srlv	srav	jr (寄存器中存的地址全)	addi	addiu	andi
RSC[4:0]	[25:21]				[25:21]	[25:21]	[25:21]	[25:21]	[25:21]	[25:21]	[25:21]
RTC[4:0]	[20:16]	[20:16]	[20:16]	[20:16]	[20:16]	[20:16]	[20:16]				
M1	01	01	01	01	01	01	01	10	01	01	01
M2	01	01	01	01	01	01	01	x	01	01	01
M3	1	0	0	0	1	1	1	1	1	1	1
M4	0	0	0	0	0	0	0	x	1	1	1
M5	0	0	0	0	0	0	0	x	0	0	0
~~M6~~											
RDC[4:0]	[15:11]	[15:11]	[15:11]	[15:11]	[15:11]	[15:11]	[15:11]	x	[20:16]	[20:16]	[20:16]
RF_W	1	1	1	1	1	1	1	0	1	1	1
RF_clk	~clk	~clk	~clk	~clk	~clk	~clk	~clk	~clk	~clk	~clk	~clk
DM_CS	0	0	0	0	0	0	0	0	0	0	0
DM_W	0	0	0	0	0	0	0	0	0	0	0
DM_R	0	0	0	0	0	0	0	0	0	0	0
ALUC[4:0]	1010	111X	1101	1100	111X	1101	1100	x	0010	0000	0100
		sa→ext5	sa→ext5	sa→ext5				多一根连线: M1_out→PC; M1→4位, 若M1[]于, 则将 RS_out→PC	[0~15] →ext16	[0~15] →ext16	[0~15] →ext16
31~26	000000	000000	000000	000000	000000	000000	000000	000000	001000	001001	001100
5~0	101011	000000	000010	000011	000100	000110	000111	001000			

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