88E3082/88E3083 Datasheet

Integrated 8-Port 10/100 Fast Ethernet Transceiver

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Overview

The Marvell® 88E3082/88E3083 devices are the third generation Marvell® DSP-based eight-port physical layer transceivers for Fast Ethernet switch applications. The devices contain all the active circuitry to convert data streams to and from eight Media Access Controllers (MACs) and the physical media. The 88E3082/88E3083 devices incorporate IEEE 802.3u Auto-Negotiation in support of both 100BASE-TX and 10BASE-T networks over twisted-pair cable in full-duplex or half-duplex mode.

To reduce the number of input/output (I/O) pins between the MAC and the Physical layer (PHY), the 88E3082/88E3083 devices support the Serial Media Independent Interface (SMII) as well as the Source Synchronous option of SMII (SSSMII). The SSSMII interface extends the allowed PCB trace distance between the PHY and the MAC, thereby facilitating more robust, higher port density, Fast Ethernet switch designs. The 88E3082/88E3083 devices support the Double Data Rate option of SSSMII (DDR-SSSMII), further reducing the required I/O pin count by nearly one-half. The 88E3082 device also supports Reduced Media Independent Interface (RMII).

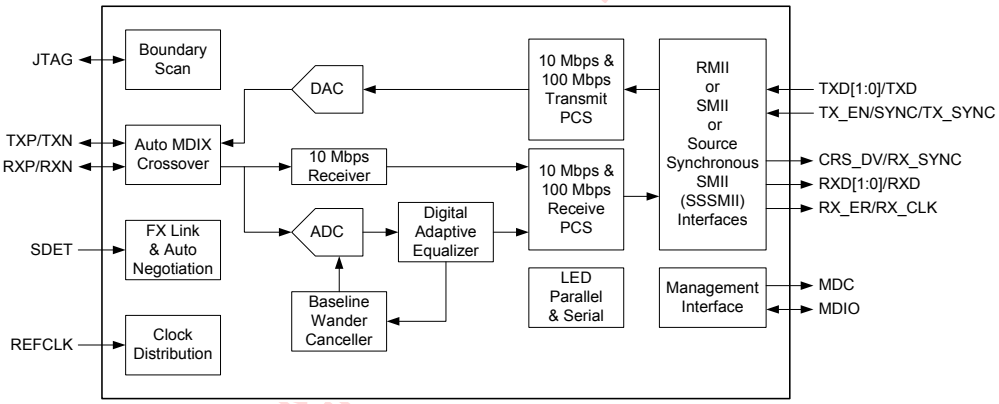
The 88E3082/88E3083 devices feature a mode of operation supporting IEEE compliant 100BASE-FX fiber-optic networks. The 88E3082 device includes a PECL interface that is selectable on a per port basis for 100BASE-FX applications, while the PECL interface is available on a single port (Port 7) for the 88E3083 device. Additionally, the 88E3082/88E3083 devices implement Far-End Fault Indication (FEFI) in order to provide a mechanism for transferring information from the local station to the link partner that indicates a remote fault has occurred in 100BASE-FX mode.

The 88E3082/88E3083 devices feature the Marvell Virtual Cable Tester® (VCT™) technology, which enables IT managers and networking equipment manufacturers to remotely analyze the quality and characteristics of the attached cable plant. Using Time Domain Reflectometry technology, the VCT feature detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew.

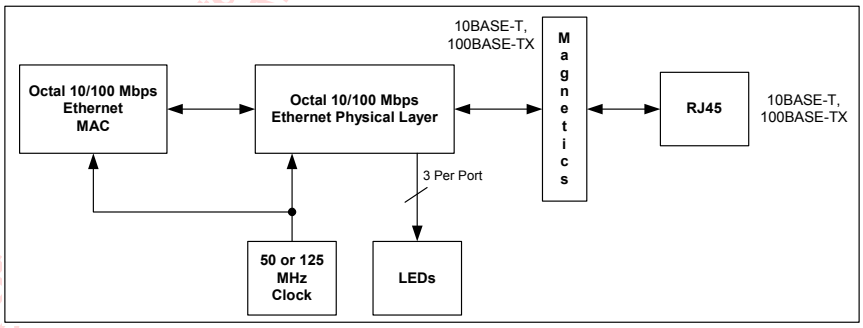
The 88E3082/88E3083 devices use advanced mixed-signal processing and power management techniques for extremely low power dissipation and high port count system integration. The 88E3082 device is manufactured in an all CMOS process and packaged in a 224-pin TFBGA package, while the 88E3083 device is packaged in a small form factor 128-LQFP package.

Features

- Eight independent IEEE 802.3 compliant 100BASE-TX and 10BASE-T ports
- Serial MII (SMII) with Source Synchronous SMII (SSSMII) and Double Data Rate (DDR-SSSMII) options
- Reduced MII (RMII) support (88E3082 only)
- Virtual Cable Tester® (VCT™) Technology
- PECL interface supporting 100BASE-FX applications on a per port basis (Port 7 only for 88E3083)
- Automatic MDI/MDIX crossover for 100BASE-TX and 10BASE-T ports
- Jumbo frame support to 10 Kbytes with up to ±150 ppm clock frequency difference IEEE 802.3u Auto-Negotiation support for automatic speed and duplex selection
- Far-End Fault Indication (FEFI) support for 100BASE-FX applications
- Energy detect feature
- Baseline wander correction
- Flexible serial management interface (MDC/MDIO) for register access
- Programmable interrupt to minimize polling
- IEEE 1149.1 Standard Test Access Port and boundary scan compatible
- Low power dissipation P_{Ave} = 150 mW per port
- Supports three (3) LEDs per port
- 0.15 µm standard digital CMOS process
- 224-pin TFBGA 15 mm x 17 mm package (88E3082 device)
- 128-pin LQFP 14 mm x 20 mm package (88E3083 device)
- 88E3082 available in commercial or industrial grade



Functional Block Diagram



System Diagram

Table 1: 88E3082/88E3083 Devices Feature Differences

	88E3082	88E3083
Package	224-pin TFBGA	128-pin LQFP
RMII	Yes	No
SMII	Yes	Yes
SSSMII	Yes	Yes
DDR-SSSMII	Yes	Yes
Virtual Cable Tester®	Yes	Yes
Fiber Support	All Ports	Available in Port 7 only
Parallel LEDs	Yes	Yes
Serial LED Mode	Yes	No
Power Management	Yes	Yes
Industrial Grade	Yes	No

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Section 1. Signal Description

The 88E3082 is manufactured in a 224-pin TFBGA. Due to the large number of pins, the 224-pin TFBGA is depicted graphically over two facing pages.

1.1 224-Pin TFBGA Pinout

Figure 1: 88E3082 Integrated 8 Port 10/100 Fast Ethernet Transceiver 224-Pin TFBGA Package

	1	2	3	4	5	6	7	
A	VSS	P1_TXD[0]	P1_RXD[0]	P2_TX_EN	P3_TXD[1]	P3_TX_EN	P3_RXD[1]	A
B	P0_CRS_DV	P1_TXD[1]	P1_CRS_DV	P2_TXD[0]	P2_CRS_DV	P3_TXD[0]	P3_RX_ER	B
C	P0_TXD[0]	P0_RXD[0]	P1_RX_ER	P1_RXD[1]	P2_RX_ER	P2_RXD[1]	P3_RXD[0]	C
D	INTn	P0_TX_EN	SEL_25V	P1_TX_EN	P2_TXD[1]	P2_RXD[0]	P3_CRS_DV	D
E	RESETn	P0_TXD[1]	P0_RXD[1]	VDDO	VDDO	VDDO	VDDO	E
F	NORMAL	CONFIG10	P0_RX_ER	VDD	VDD	VSS	VSS	F
G	TDI	TDO	MDIO	MDC	VSS	VSS	VSS	G
H	TMS	TCK	CONFIG8	CONFIG9	VSS	VSS	VSS	H
J	CONFIG6	TRSTn	CONFIG7	CONFIG5	VSS	VSS	VSS	J
K	CONFIG3	CONFIG4	CONFIG1	CONFIG2	VSS	VSS	VSS	K
L	HSDACP	HSDACN	CONFIG0	VSS	VSS	VSS	VSS	L
M	CONTROL	RSET	P1_SDET	VSS	AVDDAH	AVDDAH	AVDDAH	M
N	TST_PT	P0_SDET	P2_SDET	VSS	AVDDAL	AVDDAL	AVDDAL	N
P	P0_RXN	P0_RXP	P3_SDET	VSS	VSS	VSS	VSS	P
R	P0_TXP	P1_TXN	P1_RXP	P2_RXN	P2_TXP	P3_TXN	P3_RXP	R
T	P0_TXN	P1_TXP	P1_RXN	P2_RXP	P2_TXN	P3_TXP	P3_RXN	T
	1	2	3	4	5	6	7	

(TOP VIEW)

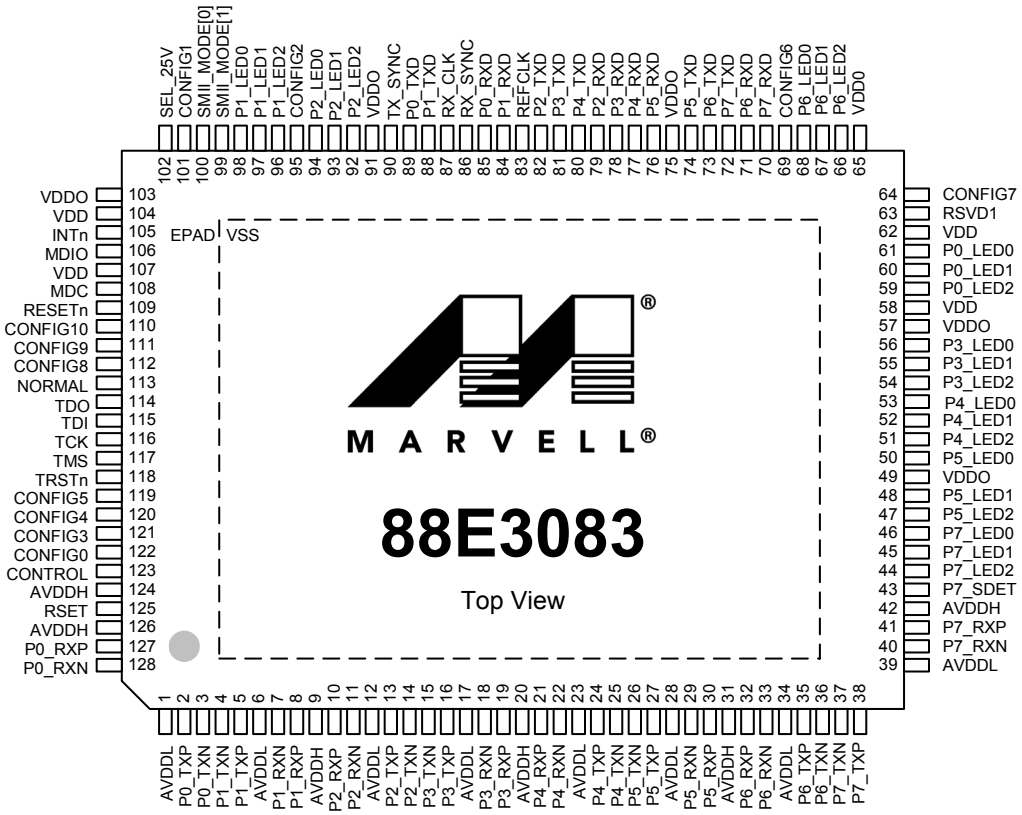
	8	9	10	11	12	13	14	
A	P4_TXD[1]	P4_CRS_DV	P5_TXD[1]	P5_RX_ER	P6_TXD[1]	P6_CRS_DV	P6_RXD[1]	A
B	REFCLK	P4_RX_ER	P5_TXD[0]	P5_CRS_DV	P6_TXD[0]	P6_RXD[0]	P7_TXD[1]	B
C	P4_TX_EN	P4_RXD[0]	P5_TX_EN	P5_RXD[0]	P6_TX_EN	P7_TXD[0]	P7_RXD[1]	C
D	P4_TXD[0]	P4_RXD[1]	P5_RXD[1]	P6_RX_ER	P7_TX_EN	SEL_RMII	P0_LED1	D
E	VDD0	VDD0	VDD0	P7_CRS_DV	P7_RXD[0]	P0_LED2	P1_LED0	E
F	VSS	VSS	VSS	VDD	P7_RX_ER	P1_LED2	P2_LED1	F
G	VSS	VSS	VSS	VDD	P0_LED0	P2_LED0	P2_LED2	G
H	VSS	VSS	VSS	VDD	P1_LED1	P3_LED0	P3_LED1	H
J	VSS	VSS	VSS	VDD	P3_LED2	P4_LED0	P4_LED1	J
K	VSS	VSS	VSS	VDD	P6_LED0	P4_LED2	P5_LED0	K
L	VSS	VSS	VSS	P7_LED2	P7_SDET	P5_LED2	P5_LED1	L
M	AVDDAH	AVDDAH	AVDDAH	P4_SDET	LEDSER	P6_LED2	P6_LED1	M
N	AVDDAL	AVDDAL	AVDDAL	P5_SDET	LEDCLK	P7_LED1	P7_LED0	N
P	VSS	VSS	VSS	P6_SDET	LEDENA	P7_RXP	P7_RXN	P
R	P4_RXP	P4_TXN	P5_TXP	P5_RXN	P6_RXP	P6_TXN	P7_TXP	R
T	P4_RXN	P4_TXP	P5_TXN	P5_RXP	P6_RXN	P6_TXP	P7_TXN	T
	8	9	10	11	12	13	14	

(TOP VIEW)

1.2 128-Pin LQFP Pinout

The 88E3083 is manufactured in a 128-pin LQFP.

Figure 2: 88E3083 Integrated 8 Port 10/100 Fast Ethernet Transceiver 128-Pin LQFP Package



Where the EPAD is the ground plate

1.3 88E3082 Pin Description

Table 2: RMII Interface

224-Pin BGA Package	Pin Name	Type	Description
E11 A13 B11 A9 D7 B5 B3 B1	P7_CRS_DV P6_CRS_DV P5_CRS_DV P4_CRS_DV P3_CRS_DV P2_CRS_DV P1_CRS_DV P0_CRS_DV	Output	In RMII mode, CRS_DV for the designated port asserts when the receive medium is non-idle. The assertion of CRS_DV is asynchronous to REFCLK. At the de-assertion of carrier, CRS_DV de-asserts synchronously to REFCLK only on the first di-bit of RXD[1:0]. If there is still data in the FIFO not yet presented onto RXD[1:0], then on the second di-bit of RXD[1:0], CRS_DV is asserted synchronously to REFCLK. The toggling of CRS_DV on the first and second di-bit continues until all the data in the FIFO is presented onto RXD[1:0]. CRS_DV is asserted for the duration of carrier activity for a false carrier event.
E12 B13 C11 C9 C7 D6 A3 C2	P7_RXD[0] P6_RXD[0] P5_RXD[0] P4_RXD[0] P3_RXD[0] P2_RXD[0] P1_RXD[0] P0_RXD[0]	Output	In RMII mode, RXD[0] and RXD[1] for the designated port di-bits change synchronously to REFCLK. Upon assertion of CRS_DV, RXD[0] and RXD[1] remain at 00 until valid data is output from the FIFO onto RXD[1:0]. The start of valid data is indicated by 01 on RXD[1:0]. If a false carrier or a symbol error is detected, RXD[1:0] are set to 10 for the duration of the activity. **NOTE:** In 100 Mbps mode, RXD[1:0] can change once per REFCLK cycle, whereas in 10 Mbps mode RXD[1:0] will be held steady for 10 consecutive REFCLK cycles.
C14 A14 D10 D9 A7 C6 C4 E3	P7_RXD[1] P6_RXD[1] P5_RXD[1] P4_RXD[1] P3_RXD[1] P2_RXD[1] P1_RXD[1] P0_RXD[1]	Output	See RXD[0] above.
F12 D11 A11 B9 B7 C5 C3 F3	P7_RX_ER P6_RX_ER P5_RX_ER P4_RX_ER P3_RX_ER P2_RX_ER P1_RX_ER P0_RX_ER	Output	In RMII mode, RX_ER for the designated port indicates whether a symbol error has occurred, and it is driven synchronously to REFCLK.

Table 2: RMII Interface (Continued)

224-Pin BGA Package	Pin Name	Type	Description
D12 C12 C10 C8 A6 A4 D4 D2	P7_TX_EN P6_TX_EN P5_TX_EN P4_TX_EN P3_TX_EN P2_TX_EN P1_TX_EN P0_TX_EN	Input	In RMII mode, TX_EN for the designated port indicates that the di-bit on TXD[1:0] is valid, and it should be driven synchronously to REFCLK.
C13 B12 B10 D8 B6 B4 A2 C1	P7_TXD[0] P6_TXD[0] P5_TXD[0] P4_TXD[0] P3_TXD[0] P2_TXD[0] P1_TXD[0] P0_TXD[0]	Input	In RMII mode, TXD[0] and TXD[1] for the designated port input the di-bits that are transmitted and should be driven synchronously to REFCLK. Note that in 100 Mbps mode TXD[1:0] can change once per REFCLK cycle, whereas in 10 Mbps mode TXD[1:0] must be held steady for 10 consecutive REFCLK cycles.
B14 A12 A10 A8 A5 D5 B2 E2	P7_TXD[1] P6_TXD[1] P5_TXD[1] P4_TXD[1] P3_TXD[1] P2_TXD[1] P1_TXD[1] P0_TXD[1]	Input	In RMII mode, see TXD[0] above.

Table 3: SMII/Source Synchronous SMII (SSSMII) Interface

224-Pin BGA Package	Pin Name/ SMII/SSSMII Pin Name	Type	Description
B11 A11 D9 C9 A9 B9 A7 C7	P5_CRS_DV/P7_RXD P5_RX_ER/P6_RXD P4_RXD[1]/P5_RXD P4_RXD[0]/P4_RXD P4_CRS_DV/P3_RXD P4_RX_ER/P2_RXD P3_RXD[1]/P1_RXD P3_RXD[0]/P0_RXD	Output	Serial stream receive data output for SMII/SSSMII mode. In SMII mode, RXD asserts synchronously with respect to REFCLK. In SSSMII mode, RXD asserts synchronously with respect to RX_CLK. In SMII/SSSMII mode, P5_CRS_DV becomes P7_RXD, P5_RX_ER becomes P6_RXD, P4_RXD[1] becomes P5_RXD, P4_RXD[0] becomes P4_RXD, P4_CRS_DV becomes P3_RXD, P4_RX_ER becomes P2_RXD, P3_RXD[1] becomes P1_RXD and P3_RXD[0] becomes P0_RXD. P[7:6]_CRS_DV and P[2:0]_CRS_DV are not used and are driven low. In 100 Mbps mode, RXD outputs a new 10-bit segment starting with SYNC/TX_SYNC. In 10 Mbps mode, RXD repeats each 10-bit segment 10 times. For details on SMII/SSSMII Mode, refer to page 53.
B7	P3_RX_ER/RX_CLK	Output	In SMII mode, P3_RX_ER is not used and is driven low. In SSSMII mode, P3_RX_ER becomes RX_CLK. For details on SMII/SSSMII Mode refer to page 53.
D7	P3_CRS_DV/RX_SYNC	Output	In SMII mode, P3_CRS_DV is not used and is driven low. In SSSMII mode, P3_CRS_DV becomes RX_SYNC and is used as the sync signal that sets the bit stream alignment of RXD for all ports. RX_SYNC requires an active TX_SYNC that asserts every ten clock cycles. For details on SMII/SSSMII Mode, refer to page 53.

Table 3: SMII/Source Synchronous SMII (SSSMII) Interface (Continued)

224-Pin BGA Package	Pin Name/ SMII/SSSMII Pin Name	Type	Description
E11 A13 B5 B3 B1 E12 B13 C11 D6 A3 C2 C14 A14 D10 C6 C4 E3 F12 D11 C5 C3 F3	P7_CRS_DV P6_CRS_DV P2_CRS_DV P1_CRS_DV P0_CRS_DV P7_RXD[0] P6_RXD[0] P5_RXD[0] P2_RXD[0] P1_RXD[0] P0_RXD[0] P7_RXD[1] P6_RXD[1] P5_RXD[1] P2_RXD[1] P1_RXD[1] P0_RXD[1] P7_RX_ER P6_RX_ER P2_RX_ER P1_RX_ER P0_RX_ER	Output	These pins are not used in SMII or SSSMII modes and are driven low.
C10 B10 A10 C8 D8 A8 A6 B6	P5_TX_EN/P7_TXD P5_TXD[0]/P6_TXD P5_TXD[1]/P5_TXD P4_TX_EN/P4_TXD P4_TXD[0]/P3_TXD P4_TXD[1]/P2_TXD P3_TX_EN/ P1_TXD P3_TXD[0]/P0_TXD	Input	In SMII mode, TXD for the designated port latches in the data that will be transmitted, and it is driven synchronously to REFCLK. P5_TX_EN become P7_TXD, P5_TXD[0] becomes P6_TXD, P5_TXD[1] becomes P5_TXD, P4_TX_EN becomes P4_TXD, P4_TXD[0] becomes P3_TXD, P4_TXD[1] become P2_TXD, P3_TX_EN becomes P1_TXD and P3_TXD[0] becomes P0_TXD. In SSSMII mode, TXD for the designated port latches in the data that is transmitted and is driven synchronously to TX_CLK. In 100 Mbps mode, TXD latches in the new 10-bit segment starting with TX_SYNC. In 10 Mbps mode, TXD must repeat each 10-bit segment 10 times. For details on SMII/SSSMII Mode, refer to page 53.

Table 3: SMII/Source Synchronous SMII (SSSMII) Interface (Continued)

224-Pin BGA Package	Pin Name/ SMII/SSSMII Pin Name	Type	Description
D4 A2	P1_TX_EN /SMII_MODE[1] P1_TXD[0] /SMII_MODE[0]	Input	In SMII/SSSMII mode, P1_TX_EN becomes SMII_MODE[1] and P1_TXD0 becomes SMII_MODE[0]. These pins select between various SMII modes. SMII_MODE[1] SMII_MODE[0] Mode Low Low SMII Low High SSSMII High High DDR_SSSMII These pins must be held stable during normal operation, including the entire duration of reset. For details on SMII/SSSMII Mode, refer to page 53.
A5	P3_TXD1/SYNC/ TX_SYNC	Input	In SMII mode, P3_TXD1 becomes SYNC. In SSSMII mode, P3_TXD1 becomes TX_SYNC.
D12 C12 A4 D2 C13 B12 B4 C1 B14 A12 D5 B2 E2	P7_TX_EN P6_TX_EN P2_TX_EN P0_TX_EN P7_TXD[0] P6_TXD[0] P2_TXD[0] P0_TXD[0] P7_TXD[1] P6_TXD[1] P2_TXD[1] P1_TXD[1] P0_TXD[1]	Input	These pins are not used in SMII or SSSMII modes and should be tied to the ground.

Table 4: DDR (Double Data Rate) SSSMII Interface

224-Pin BGA Package	Pin Name/ DDR-SSSMII Pin Name	Type	Description
D9 C9 A7 C7	P4_RXD[1]/P67_RXD P4_RXD[0]/P45_RXD P3_RXD[1]/P23_RXD P3_RXD[0]/P01_RXD	Output	In DDR-SSSMII mode, P4_RXD[1] becomes P67_RXD, P4_RXD[0] becomes P45_RXD, P3_RXD[1] becomes P23_RXD and P3_RXD[0] becomes P01_RXD. In 100 Mbps mode, RXD outputs a new 10-bit segment starting with TX_SYNC. In 10 Mbps mode, RXD repeats each 10-bit segment 10 times. P4_RXD[1] is used for P6_TXD on the negative edge of RX_CLK & P7_RXD on the positive edge of RX_CLK. P4_RXD[0] is used for P4_TXD on the negative edge of RX_CLK & P5_RXD on the positive edge of RX_CLK. P3_RXD[1] is used for P2_TXD on the negative edge of RX_CLK & P3_RXD on the positive edge of RX_CLK. P3_RXD[0] is used for P0_TXD on the negative edge of RX_CLK & P1_RXD on the positive edge of RX_CLK. For details on DDR-SSSMII Mode, refer to page 54.
B7	P3_RX_ER/RX_CLK	Output	In DDR-SSSMII mode, P3_RX_ER becomes RX_CLK. For details on DDR-SSSMII Mode, refer to page 54.
D7	P3_CRS_DV/RX_SYNC	Output	In DDR-SSSMII mode,P3_CRS_DV becomes RX_SYNC and is used as the sync signal that sets the bit stream alignment of RXD for all ports. RX_SYNC requires an active TX_SYNC that asserts every ten clock cycles. For details on DDR-SSSMII Mode, refer to page 54.

Table 4: DDR (Double Data Rate) SSSMII Interface (Continued)

224-Pin BGA Package	Pin Name/ DDR-SSSMII Pin Name	Type	Description
E11	P7_CRS_DV	Output	These pins are not used in the DDR-SSSMII mode and are driven low.
A13	P6_CRS_DV		
B11	P5_CRS_DV		
A9	P4_CRS_DV		
B5	P2_CRS_DV		
B3	P1_CRS_DV		
B1	P0_CRS_DV		
E12	P7_RXD[0]		
B13	P6_RXD[0]		
C11	P5_RXD[0]		
D6	P2_RXD[0]		
A3	P1_RXD[0]		
C2	P0_RXD[0]		
C14	P7_RXD[1]		
A14	P6_RXD[1]		
D10	P5_RXD[1]		
C6	P2_RXD[1]		
C4	P1_RXD[1]		
E3	P0_RXD[1]		
F12	P7_RX_ER		
D11	P6_RX_ER		
A11	P5_RX_ER		
B9	P4_RX_ER		
C5	P2_RX_ER		
C3	P1_RX_ER		
F3	P0_RX_ER		

Table 4: DDR (Double Data Rate) SSSMII Interface (Continued)

224-Pin BGA Package	Pin Name/ DDR-SSSMII Pin Name	Type	Description
C8 D8 A6 B6	P4_TX_EN/P67_TXD P4_TXD[0]/P45_TXD P3_TX_EN/ P23_TXD P3_TXD[0]/P01_TXD	Input	In DDR-SSSMII mode, P4_TX_EN becomes P67_TXD, P4_TXD[0] becomes P45_TXD, P3_TX_EN becomes P23_TXD and P3_TXD[0] become P01_TXD. In DDR-SSSMII mode, TXD for the designated port latches in the data that will be transmitted, and it is driven synchronously to REFCLK. In 100 Mbps mode, TXD inputs a new 10-bit segment starting with TX_SYNC. In 10 Mbps mode, TXD must repeat each 10-bit segment 10 times. P4_TX_EN is used for P6_TXD on the negative edge of REF_CLK & P7_TXD on the positive edge of REF_CLK. P4_TXD[0] is used for P4_TXD on the negative edge of REF_CLK & P5_TXD on the positive edge of REF_CLK. P3_TX_EN is used for P2_TXD on the negative edge of REF_CLK & P3_TXD on the positive edge of REF_CLK. P3_TXD[0] is used for P0_TXD on the negative edge of REF_CLK & P1_TXD on the positive edge of REF_CLK. For details on DDR-SSSMII Mode, refer to page 54.
D4 A2	P1_TX_EN /SMII_MODE[1] P1_TXD[0] /SMII_MODE[0]	Input	In DDR-SSSMII mode, P1_TX_EN becomes SMII_MODE[1] and P1_TXD[0] becomes SMII_MODE[0]. These pins select between various SMII modes. SMII_MODE[1] SMII_MODE[0] Mode Low Low SMII Low High SSSMII High High DDR_SSSMII For details on DDR-SSSMII Mode, refer to page 54.

Table 4: DDR (Double Data Rate) SSSMII Interface (Continued)

224-Pin BGA Package	Pin Name/ DDR-SSSMII Pin Name	Type	Description
A5	P3_TXD[1]/TX_SYNC	Input	In DDR-SSSMII mode, P3_TXD[1] becomes TX_SYNC. For details on DDR-SSSMII Mode, refer to page 54.
D12 C12 C10 A4 D2 C13 B12 B10 B4 C1 B14 A12 A10 A8 D5 B2 E2	P7_TX_EN P6_TX_EN P5_TX_EN P2_TX_EN P0_TX_EN P7_TXD[0] P6_TXD[0] P5_TXD[0] P2_TXD[0] P0_TXD[0] P7_TXD[1] P6_TXD[1] P5_TXD[1] P4_TXD[1] P2_TXD[1] P1_TXD[1] P0_TXD[1]	Input	These pins are not used in DDR-SSSMII mode and should be tied to ground.

Table 5: Network

224-Pin BGA Package	Pin Name	Type	Description
P13 R12 T11 R8 R7 T4 R3 P2	P7_RXP P6_RXP P5_RXP P4_RXP P3_RXP P2_RXP P1_RXP P0_RXP	Input	Receiver input – Differential positive signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. RXP connects directly to the receiver magnetics. If a port is configured for 100BASE-FX mode, RXP connects directly to the fiber-optic receiver's positive output. These pins can become outputs if Auto MDI/MDIX Cross-over is enabled.
P14 T12 R11 T8 T7 R4 T3 P1	P7_RXN P6_RXN P5_RXN P4_RXN P3_RXN P2_RXN P1_RXN P0_RXN	Input	Receiver input – Differential negative signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. RXN connects directly to the receiver magnetics. If a port is configured for 100BASE-FX mode, RXN connects directly to the fiber-optic receiver's negative output. These pins can become outputs if Auto MDI/MDIX Cross-over is enabled.
R14 T13 R10 T9 T6 R5 T2 R1	P7_TXP P6_TXP P5_TXP P4_TXP P3_TXP P2_TXP P1_TXP P0_TXP	Output	Transmitter output – Differential positive signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. TXP connects directly to the transmitter magnetics. If a port is configured for 100BASE-FX mode, TXP connects directly to the fiber-optic transmitters positive input. These pins can become inputs if Auto MDI/MDIX Cross-over is enabled.
T14 R13 T10 R9 R6 T5 R2 T1	P7_TXN P6_TXN P5_TXN P4_TXN P3_TXN P2_TXN P1_TXN P0_TXN	Output	Transmitter output – Differential negative signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. TXN connects directly to the transmitter magnetics. If a port is configured for 100BASE-FX mode, TXN connects directly to the fiber-optic transmitters negative input. These pins can become inputs if Auto MDI/MDIX Cross-over is enabled.
L12 P11 N11 M11 P3 N3 M3 N2	P7_SDET P6_SDET P5_SDET P4_SDET P3_SDET P2_SDET P1_SDET P0_SDET	Input	In 100BASE-FX mode, SDET indicates whether a signal is detected by the fiber-optic transceiver. In 100BASE-TX/10BASE-T modes, these pins are not used and should be tied to ground.

Table 6: Selection

224-pin TFBGA Package	Pin Name	Type	Description
D13	SEL_RMII	Input	SEL_RMII selects between the RMII and the three SMII modes namely SMII, SSSMII, and DDR-SSSMII mode. This pin must be held stable during normal operation, including the entire duration of reset, since SEL_RMII determines the expected clock frequency of REFCLK. If the SEL_RMII is not stable, the internal clock dividers and multipliers will not work properly. SEL_RMII is internally pulled high via resistor. High = RMII Low = SMII or SSSMII or DDR-SSSMII

Table 7: Serial Management Interface

224-pin TFBGA Package	Pin Name	Type	Description
G4	MDC	Input	MDC is the clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.33 MHz.
G3	MDIO	I/O	MDIO is the management data. MDIO is used to transfer management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
D1	INTn	Open Drain	INTn is an active low pin that is asserted to indicate an interrupt event has occurred. INTn is an open drain pin. To set the INTn pin high when it is inactive, multiple INTn lines may be tied together with a single, external pull-up resistor. See “Programming Interrupts” on page 60.

Table 8: LED

224-pin TFBGA Package	Pin Name	Type	Description
L11 M13 L13 K13 J12 G14 F13 E13	P7_LED2 P6_LED2 P5_LED2 P4_LED2 P3_LED2 P2_LED2 P1_LED2 P0_LED2	Output	Parallel LED outputs. See “LED Interface” on page 82.
N13 M14 L14 J14 H14 F14 H12 D14	P7_LED1 P6_LED1 P5_LED1 P4_LED1 P3_LED1 P2_LED1 P1_LED1 P0_LED1	Output	Parallel LED outputs. See “LED Interface” on page 82.
N14 K12 K14 J13 H13 G13 E14 G12	P7_LED0 P6_LED0 P5_LED0 P4_LED0 P3_LED0 P2_LED0 P1_LED0 P0_LED0	Output	Parallel LED outputs. See “LED Interface” on page 82.
M12	LEDSER	Output	LEDSER transmits serial status bits that can be shifted into a shift register to be displayed via the LEDs. LEDSER is output synchronously to LEDCLK. See “LED Interface” on page 82.
P12	LEDENA	Output	LEDENA output asserts high during the time LEDSER transmits the status that the user selects to store into the shift register. LEDENA is transmitted synchronously to LEDCLK. See “LED Interface” on page 82.
N12	LEDCLK	Output	LEDCLK outputs the reference clock for the serial LED signals (LEDSER and LEDNA).

Table 9: JTAG

224-pin TFBGA Package	Pin Name	Type	Description
G1	TDI	Input	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
H1	TMS	Input	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
H2	TCK	Input	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
J2	TRSTn	Input	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
G2	TDO	Output	Boundary scan test data output.

Table 10: Clock/Configuration/Reset

224-pin TFBGA Package	Pin Name	Type	Description
B8	REFCLK/TX_CLK	Input	In RMII mode, this pin is REFCLK with an expected frequency of 50 MHz. In SMII mode, this pin is REFCLK with an expected frequency of 125 MHz. In SSSMII mode, this pin is TX_CLK with an expected frequency of 125 MHz. In DDR-SSSMII mode, this pin is TX_CLK with an expected frequency of 125 MHz.
J3 J1 J4 K2 K1 K4 K3 L3	CONFIG7 CONFIG6 CONFIG5 CONFIG4 CONFIG3 CONFIG2 CONFIG1 CONFIG0	Input	CONFIG[7:0] pins. These pins are used to configure Ports [7: 0] for advertising bits, Auto-Negotiation, and physical connection type (10BASE-T/100BASE-TX or 100BASE-FX) by connecting these pins to an LED output, VDDO, or VSS pin. Each LED pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. The CONFIG[7:0] pins should not be left floating. See “Hardware Configuration” on page 72.

Table 10: Clock/Configuration/Reset (Continued)

224-pin TFBGA Package	Pin Name	Type	Description
H3	CONFIG8	Input	CONFIG8 pin. This global configuration pin is used to configure LED_DEF[1], LED_DEF[0] and DIS_FEFI by connecting this pin to an LED output, VDDO, or VSS as pin follows: VSS (000) = LED_DEF[1] = 0, LED_DEF[0] = 0, FEFI disabled P0_LED0 (001) = LED_DEF[1] = 0, LED_DEF[0] = 0, FEFI enabled P0_LED1 (010) = LED_DEF[1] = 0, LED_DEF[0] = 1, FEFI disabled P0_LED2 (011) = LED_DEF[1] = 0, LED_DEF[0] = 1, FEFI enabled P1_LED0 (100) = LED_DEF[1] = 1, LED_DEF[0] = 0, FEFI disabled P1_LED1 (101) = LED_DEF[1] = 1, LED_DEF[0] = 0, FEFI enabled P1_LED2 (110) = LED_DEF[1] = 1, LED_DEF[0] = 1, FEFI disabled VDDO (111) = LED_DEF[1] = 1, LED_DEF[0] = 1, FEFI enabled **NOTE:** FEFI enabled applies to 100BASE-FX mode only Each LED, VSS, and VDDO pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. The CONFIG[10:0] pins should not be left floating. See “Hardware Configuration” on page 72.

Table 10: Clock/Configuration/Reset (Continued)

224-pin TFBGA Package	Pin Name	Type	Description
H4	CONFIG9	Input	CONFIG9 pin. This global configuration pin is used to configure ENA_XC, CLASS_A/B and ENA_EDET by connecting this pin to an LED output, VDDO, or VSS pin as follows: VSS (000) = No Crossover, Back Plane drivers, Energy Detect disabled P0_LED0 (001) = No Crossover, Back Plane drivers, Energy Detect Enabled P0_LED1 (010) = No Crossover, CAT 5 drivers, Energy Detect disabled P0_LED2 (011) = No Crossover, CAT 5 drivers, Energy Detect enabled P1_LED0 (100) = Auto Crossover, Back Plane drivers, Energy Detect disabled P1_LED1 (101) = Auto Crossover, Back Plane drivers, Energy Detect enabled P1_LED2 (110) = Auto Crossover, CAT 5 drivers, Energy Detect disabled VDDO (111) = Auto Crossover, CAT 5 drivers, Energy Detect enabled - default Each LED, VSS, and VDDO pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. They should not be left floating. See “Hardware Configuration” on page 72.

Table 10: Clock/Configuration/Reset (Continued)

224-pin TFBGA Package	Pin Name	Type	Description
F2	CONFIG10	Input	CONFIG10 pin. This global conflagration pin is used to configure PHY_ADR[4], and PHY_ADR[3] by connecting this pin to an LED output, or VSS pin as follows: VSS (000) = PHYADR[4:3] = 00 P0_LED1 (010) = PHYADR[4:3] = 01 P1_LED0 (100) = PHYADR[4:3] = 10 P1_LED2 (110) = PHYADR[4:3] = 11 Each LED and VSS pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. They should not be left floating. See “Hardware Configuration” on page 72.
F1	NORMAL	Input	Reserved. This pin should be left floating.
E1	RESETn	Input	Hardware reset. Active low. REFCLK must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be pulled high for normal operation.
D3	SEL_25V	Input	Output clamping voltage selection. If the digital I/O pins are operating at 2.5V, tie this pin to 2.5V. If the digital I/O pins are operating at 3.3V, tie this pin to ground. Refer to “VDDO” on page 29.

Table 11: Regulator & Reference

224-Pin TFBGA Package	Pin Name	Type	Description
M2	RSET	Input	Constant voltage reference. External 2 kohm 1% resistor connection to VSS is required for this pin.
M1	CONTROL	Output	Regulator Control Pin. This pin connects to the base of an external BJT for internal voltage regulation of 1.5V.

Table 12: Test

224-Pin TFBGA Package	Pin Name	Type	Description
L1	HSDACP	Output	Test Pin. Connect to VSS through a 1% tolerance 49.9 ohm resistor to support analog debug of the system. If debug is not important and there are board space constraints, this pin can be left floating.
L2	HSDACN	Output	Test Pin. Connect to VSS through a 1% tolerance 49.9 ohm resistor to support analog debug of the system. If debug is not important and there are board space constraints, this pin can be left floating.
N1	TST_PT	Output	Test point. Leave unconnected.

Table 13: Power & Ground

224-Pin TFBGA Package	Pin Name	Type	Description
E4 E5 E6 E7 E8 E9 E10	VDDO	Power	3.3V/2.5V Power to digital I/O SEL_2.5V is used to choose between 3.3V and 2.5V.
M5 M6 M7 M8 M9 M10	AVDDAH	Power	2.5V Power to analog core
N5 N6 N7 N8 N9 N10	AVDDAL	Power	1.5V Power to analog core
F4 F5 F11 G11 H11 J11 K11	VDD	Power	1.5V Power to digital core

Table 13: Power & Ground

224-Pin TFBGA Package	Pin Name	Type	Description
A1 F6 F7 F8 F9 F10 G5 G6 G7 G8 G9 G10 H5 H6 H7 H8 H9 H10 J5 J6 J7 J8 J9 J10 K5 K6 K7 K8 K9 K10 L4 L5 L6 L7 L8 L9 L10 M4 N4 P4 P5 P6 P7 P8 P9 P10	VSS	Ground	Ground

1.3.1 224-Pin TFBGA Assignments - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
M5	AVDDAH	B1	P0_CRS_DV
M6	AVDDAH	G12	P0_LED0
M7	AVDDAH	D14	P0_LED1
M8	AVDDAH	E13	P0_LED2
M9	AVDDAH	P1	P0_RXN
M10	AVDDAH	F3	P0_RX_ER
N5	AVDDAL	P2	P0_RXP
N6	AVDDAL	C2	P0_RXD[0]
N7	AVDDAL	E3	P0_RXD[1]
N8	AVDDAL	N2	P0_SDET
N9	AVDDAL	T1	P0_TXN
N10	AVDDAL	D2	P0_TX_EN
L3	CONFIG0	R1	P0_TXP
K3	CONFIG1	C1	P0_TXD[0]
K4	CONFIG2	E2	P0_TXD[1]
K1	CONFIG3	B3	P1_CRS_DV
K2	CONFIG4	E14	P1_LED0
J4	CONFIG5	H12	P1_LED1
J1	CONFIG6	F13	P1_LED2
J3	CONFIG7	T3	P1_RXN
H3	CONFIG8	C3	P1_RX_ER
H4	CONFIG9	R3	P1_RXP
F2	CONFIG10	A3	P1_RXD[0]
M1	CONTROL	C4	P1_RXD[1]
L2	HSDACN	M3	P1_SDET
L1	HSDACP	R2	P1_TXN
D1	INTn	D4	P1_TX_EN
N12	LEDCLK	T2	P1_TXP
P12	LEDENA	A2	P1_TXD[0]
M12	LEDSER	B2	P1_TXD[1]
G4	MDC	B5	P2_CRS_DV
G3	MDIO	G13	P2_LED0
F1	NORMAL	F14	P2_LED1

Pin #	Pin Name	Pin #	Pin Name
G14	P2_LED2	R8	P4_RXP
R4	P2_RXN	C9	P4_RXD[0]
C5	P2_RX_ER	D9	P4_RXD[1]
T4	P2_RXP	M11	P4_SDET
D6	P2_RXD[0]	R9	P4_TXN
C6	P2_RXD[1]	C8	P4_TX_EN
N3	P2_SDET	T9	P4_TXP
T5	P2_TXN	D8	P4_TXD[0]
A4	P2_TX_EN	A8	P4_TXD[1]
R5	P2_TXP	B11	P5_CRS_DV
B4	P2_TXD[0]	K14	P5_LED0
D5	P2_TXD[1]	L14	P5_LED1
D7	P3_CRS_DV	L13	P5_LED2
H13	P3_LED0	R11	P5_RXN
H14	P3_LED1	A11	P5_RX_ER
J12	P3_LED2	T11	P5_RXP
T7	P3_RXN	C11	P5_RXD[0]
B7	P3_RX_ER	D10	P5_RXD[1]
R7	P3_RXP	N11	P5_SDET
C7	P3_RXD[0]	T10	P5_TXN
A7	P3_RXD[1]	C10	P5_TX_EN
P3	P3_SDET	R10	P5_TXP
R6	P3_TXN	B10	P5_TXD[0]
A6	P3_TX_EN	A10	P5_TXD[1]
T6	P3_TXP	A13	P6_CRS_DV
B6	P3_TXD[0]	K12	P6_LED0
A5	P3_TXD[1]	M14	P6_LED1
A9	P4_CRS_DV	M13	P6_LED2
J13	P4_LED0	T12	P6_RXN
J14	P4_LED1	D11	P6_RX_ER
K13	P4_LED2	R12	P6_RXP
T8	P4_RXN	B13	P6_RXD[0]
B9	P4_RX_ER	A14	P6_RXD[1]

Pin #	Pin Name	Pin #	Pin Name
P11	P6_SDET	F5	VDD
R13	P6_TXN	F11	VDD
C12	P6_TX_EN	G11	VDD
T13	P6_TXP	H11	VDD
B12	P6_TXD[0]	J11	VDD
A12	P6_TXD[1]	K11	VDD
E11	P7_CRS_DV	E4	VDDO
N14	P7_LED0	E5	VDDO
N13	P7_LED1	E6	VDDO
L11	P7_LED2	E7	VDDO
P14	P7_RXN	E8	VDDO
F12	P7_RX_ER	E9	VDDO
P13	P7_RXP	E10	VDDO
E12	P7_RXD[0]	A1	VSS
C14	P7_RXD[1]	F6	VSS
L12	P7_SDET	F7	VSS
T14	P7_TXN	F8	VSS
D12	P7_TX_EN	F9	VSS
R14	P7_TXP	F10	VSS
C13	P7_TXD[0]	G5	VSS
B14	P7_TXD[1]	G6	VSS
B8	REFCLK	G7	VSS
E1	RESETn	G8	VSS
M2	RSET	G9	VSS
D3	SEL_25V	G10	VSS
D13	SEL_RMII	H5	VSS
H2	TCK	H6	VSS
G1	TDI	H7	VSS
G2	TDO	H8	VSS
H1	TMS	H9	VSS
J2	TRSTn	H10	VSS
N1	TST_PT	J5	VSS
F4	VDD	J6	VSS

Pin #	Pin Name	Pin #	Pin Name
J7	VSS	L7	VSS
J8	VSS	L8	VSS
J9	VSS	L9	VSS
J10	VSS	L10	VSS
K5	VSS	M4	VSS
K6	VSS	N4	VSS
K7	VSS	P4	VSS
K8	VSS	P5	VSS
K9	VSS	P6	VSS
K10	VSS	P7	VSS
L4	VSS	P8	VSS
L5	VSS	P9	VSS
L6	VSS	P10	VSS

1.4 88E3083 Pin Description

Table 14: SMII/Source Synchronous SMII (SSSMII) Interface

128-Pin LQFP Package	Pin Name	Type	Description
70 71 76 77 78 79 84 85	P7_RXD P6_RXD P5_RXD P4_RXD P3_RXD P2_RXD P1_RXD P0_RXD	Output	Serial stream receive data output for SMII/SSSMII mode. In SMII mode, RXD asserts synchronously with respect to REFCLK. In SSSMII mode, RXD asserts synchronously with respect to RX_CLK. In 100 Mbps mode, RXD outputs a new 10-bit segment starting with SYNC/TX_SYNC. In 10 Mbps mode, RXD repeats each 10-bit segment 10 times. For details on SMII/SSSMII Mode, refer to page 53.
87	RX_CLK	Output	In SMII mode this pin is not used and is driven low. In SSSMII mode, this pin provides the receive clock for the MAC. The receive data is synchronous with the RX_CLK. For details on SSSMII Mode refer to page 53.
86	RX_SYNC	Output	In SMII mode this pin is not used and is driven low. RX_SYNC is used as the sync signal that sets the bit stream alignment of RXD for all ports in SSSMII mode. RX_SYNC requires an active TX_SYNC that asserts every ten clock cycles. For details on SSSMII Mode, refer to page 53.
72 73 74 80 81 82 88 89	P7_TXD P6_TXD P5_TXD P4_TXD P3_TXD P2_TXD P1_TXD P0_TXD	Input	Serial stream transmit data input for SMII/SSSMII mode. In SMII/SSSMII mode, TXD for the designated port latches in the data that will be transmitted, and is driven synchronously to REFCLK/TX_CLK. In 100 Mbps mode, TXD inputs a new 10-bit segment starting with SYNC/TX_SYNC. In 10 Mbps mode, TXD must repeat each 10-bit segment 10 times. For details on SMII/SSSMII Mode, refer to page 53.

Table 14: SMII/Source Synchronous SMII (SSSMII) Interface (Continued)

128-Pin LQFP Package	Pin Name	Type	Description
99 100	SMII_MODE[1] SMII_MODE[0]	Input	SMII_MODE[0]/SMII_MODE[1]. These pins select between various SMII modes. These pins select between various SMII modes. SMII_MODE[1] SMII_MODE[0] Mode Low Low SMII Low High SSSMII High High DDR_SSSMII These pins must be held stable during normal operation, including the entire duration of reset. For details on SMII/SSSMII Mode, refer to page 53.
90	TX_SYNC	Input	In SMII mode, TX_SYNC is used as the SYNC signal that sets the bit stream alignment of TXD and RXD for all ports. In SSSMII mode, TX_SYNC is used as the sync signal that sets the bit stream alignment of TXD for all ports. For details on SMII/SSSMII mode, refer to page 53

Table 15: DDR (Double Data Rate) SSSMII Interface

128-Pin LQFP Package	Pin Name/ DDR-SSMII Pin Name	Type	Description
76 77 84 85	P5_RXD/P67_RXD P4_RXD/P45_RXD P1_RXD/P23_RXD P0_RXD/P01_RXD	Output	Double data rate serial stream receive data output. In DDR-SSSMII mode, RXD asserts synchronously with respect to RX_CLK. In DDR-SSSMII mode, P5_RXD becomes P67_RXD, P4_RXD becomes P45_RXD, P1_RXD becomes P23_RXD, and P0_RXD becomes P01_RXD. In 100 Mbps mode, RXD outputs a new 10-bit segment starting with TX_SYNC. In 10 Mbps mode, RXD repeats each 10-bit segment 10 times. P5_RXD is used for P6_RXD on the negative edge of RX_CLK and P7_RXD on the positive edge of RX_CLK. P4_RXD is used for P4_RXD on the negative edge of RX_CLK and P5_RXD on the positive edge of RX_CLK. P1_RXD is used for P2_RXD on the negative edge of RX_CLK and P3_RXD on the positive edge of RX_CLK. P0_RXD is used for P0_RXD on the negative edge of RX_CLK and P1_RXD on the positive edge of RX_CLK. For details on DDR-SSSMII Mode, refer to page 54.
70 71 78 79	P7_RXD P6_RXD P3_RXD P2_RXD	Output	These pins are not used in DDR-SSSMII mode and are driven low.
87	RX_CLK	Output	In DDR-SSSMII mode, this pin provides the receive clock for the MAC. The receive data is synchronous with the RX_CLK. For details on DDR-SSSMII Mode, refer to page 54.
86	RX_SYNC	Output	In DDR-SSSMII mode, RX_SYNC is used as the sync signal that sets the bit stream alignment of RXD for all ports. RX_SYNC requires an active TX_SYNC that asserts every ten clock cycles. For details on DDR-SSSMII Mode, refer to page 54.

Table 15: DDR (Double Data Rate) SSSMII Interface (Continued)

128-Pin LQFP Package	Pin Name/ DDR-SSMII Pin Name	Type	Description
80 81 88 89	P4_TXD/P67_TXD P3_TXD/P45_TXD P1_TXD/P23_TXD P0_TXD/P01_TXD	Input	Double data rate serial stream transmit data input. These pins are data output pins on DDR-SSSMII mode.In DDR-SSSMII mode, P4_TXD becomes P67_TXD, P3_TXD becomes P45_TXD, P1_TXD becomes P23_TXD, and P0_TXD becomes P01_TXD. In DDR-SSSMII mode, TXD for the designated port latches in the data that will be transmitted, and it is driven synchronously to REFCLK. In 100 Mbps mode, TXD inputs a new 10-bit segment starting with TX_SYNC. In 10 Mbps mode, TXD must repeat each 10-bit segment 10 times. P4_TXD is used for P6_TXD on the negative edge of REF_CLK and P7_TXD on the positive edge of REF_CLK. P3_TXD is used for P4_TXD on the negative edge of REF_CLK and P5_TXD on the positive edge of REF_CLK. P1_TXD is used for P2_TXD on the negative edge of REF_CLK and P3_TXD on the positive edge of REF_CLK. P0_TXD is used for P0_TXD on the negative edge of REF_CLK and P1_TXD on the positive edge of REF_CLK. For details on DDR-SSSMII Mode, refer to page 54.
90	TX_SYNC	Input	In SMII mode, TX_SYNC is used as the sync signal which sets the bit stream alignment of TXD for all ports. For details on DDR-SSSMII Mode, refer to page 54.
72 73 74 82	P7_TXD P6_TXD P5_TXD P2_TXD	Input	These pins are not used in DDR-SSSMII mode and must be tied to the ground.

Table 16: Network

128-Pin LQFP Package	Pin Name	Type	Description
41 32 30 21 19 10 8 127	P7_RXP P6_RXP P5_RXP P4_RXP P3_RXP P2_RXP P1_RXP P0_RXP	Input	Receiver input – Differential positive signal shared by 100BASE-TX, 100BASE-FX[1], and 10BASE-T modes. RXP connects directly to the receiver magnetics. If port 7 is configured for 100BASE-FX mode, RXP connects directly to the fiber-optic receiver's positive output. These pins can become outputs if Auto MDI/MDIX Cross-over is enabled.
40 33 29 22 18 11 7 128	P7_RXN P6_RXN P5_RXN P4_RXN P3_RXN P2_RXN P1_RXN P0_RXN	Input	Receiver input – Differential negative signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. RXN connects directly to the receiver magnetics. If port 7 is configured for 100BASE-FX mode, RXN connects directly to the fiber-optic receiver's negative output. These pins can become outputs if Auto MDI/MDIX Cross-over is enabled.
38 35 27 24 16 13 5 2	P7_TXP P6_TXP P5_TXP P4_TXP P3_TXP P2_TXP P1_TXP P0_TXP	Output	Transmitter output – Differential positive signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. TXP connects directly to the transmitter magnetics. If port 7 is configured for 100BASE-FX mode, TXP connects directly to the fiber-optic transmitters positive input. These pins can become inputs if Auto MDI/MDIX Cross-over is enabled.
37 36 26 25 15 14 4 3	P7_TXN P6_TXN P5_TXN P4_TXN P3_TXN P2_TXN P1_TXN P0_TXN	Output	Transmitter output – Differential negative signal shared by 100BASE-TX, 100BASE-FX, and 10BASE-T modes. TXN connects directly to the transmitter magnetics. If port 7 is configured for 100BASE-FX mode, TXN connects directly to the fiber-optic transmitters negative input. These pins can become inputs if Auto MDI/MDIX Cross-over is enabled.
43	P7_SDET	Input	In 100BASE-FX mode, P7_SDET indicates whether a signal is detected by the fiber-optic transceiver for port 7.

1. For the 88E3083 device, 100BASE-FX is only available in Port 7 only.

Table 17: Selection

128-Pin LQFP Package	Pin Name	Type	Description
63	RSVD1	Input	For test purposes only. This pin must be tied to ground.

Table 18: Serial Management Interface

128-Pin LQFP Package	Pin Name	Type	Description
108	MDC	Input	MDC is the clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.33 MHz.
106	MDIO	I/O	MDIO is the management data. MDIO is used to transfer management data in and out of the device synchronously to MDC. This pin requires a pull up resistor in a range from 1.5 kohm to 10 kohm.
105	INTn	Open Drain	INTn is an active low pin that is asserted to indicate an interrupt event has occurred. INTn is an open drain pin. To set the INTn pin high when it is inactive, multiple INTn lines may be tied together with a single, external pull-up resistor. See “Programming Interrupts” on page 60.

Table 19: LED

128-pin LQFP Package	Pin Name	Type	Description
44 66 47 51 54 92 96 59	P7_LED2 P6_LED2 P5_LED2 P4_LED2 P3_LED2 P2_LED2 P1_LED2 P0_LED2	Output	Parallel LED outputs. See “LED Interface” on page 82.
45 67 48 52 55 93 97 60	P7_LED1 P6_LED1 P5_LED1 P4_LED1 P3_LED1 P2_LED1 P1_LED1 P0_LED1	Output	Parallel LED outputs. See “LED Interface” on page 82.
46 68 50 53 56 94 98 61	P7_LED0 P6_LED0 P5_LED0 P4_LED0 P3_LED0 P2_LED0 P1_LED0 P0_LED0	Output	Parallel LED outputs. See “LED Interface” on page 82.

Table 20: JTAG

128-Pin LQFP Package	Pin Name	Type	Description
115	TDI	Input	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
117	TMS	Input	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
116	TCK	Input	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
118	TRSTn	Input	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
114	TDO	Output	Boundary scan test data output.

Table 21: Clock/Configuration/Reset

128-Pin LQFP Package	Pin Name	Type	Description
83	REFCLK/TX_CLK	Input	In SMII mode, this pin is REFCLK with an expected frequency of 125 MHz. In SSSMII mode, this pin is TX_CLK with an expected frequency of 125 MHz. In DDR-SSSMII mode, this pin is TX_CLK with an expected frequency of 125 MHz.
64 69 119 120 121 95 101 122	CONFIG7 CONFIG6 CONFIG5 CONFIG4 CONFIG3 CONFIG2 CONFIG1 CONFIG0	Input	CONFIG[7:0] pins. These pins are used to configure Ports [7: 0] for advertising bits, Auto-Negotiation, and physical connection type (10BASE-T/100BASE-TX or 100BASE-FX) by connecting these pins to an LED output, VDDO, or VSS pin as follows: Each LED pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. The CONFIG[7:0] pins should not be left floating. See “Hardware Configuration” on page 72.

Table 21: Clock/Configuration/Reset (Continued)

128-Pin LQFP Package	Pin Name	Type	Description
112	CONFIG8	Input	CONFIG8 pin. This global configuration pin is used to configure LED_DEF[1], LED_DEF[0] and DIS_FEFI by connecting this pin to an LED output, VDDO, or VSS as pin follows: VSS (000) = LED_DEF[1] = 0, LED_DEF[0] = 0, FEFI disabled P0_LED0 (001) = LED_DEF[1] = 0, LED_DEF[0] = 0, FEFI enabled P0_LED1 (010) = LED_DEF[1] = 0, LED_DEF[0] = 1, FEFI disabled P0_LED2 (011) = LED_DEF[1] = 0, LED_DEF[0] = 1, FEFI enabled P1_LED0 (100) = LED_DEF[1] = 1, LED_DEF[0] = 0, FEFI disabled P1_LED1 (101) = LED_DEF[1] = 1, LED_DEF[0] = 0, FEFI enabled P1_LED2 (110) = LED_DEF[1] = 1, LED_DEF[0] = 1, FEFI disabled VDDO (111) = LED_DEF[1] = 1, LED_DEF[0] = 1, FEFI enabled **NOTE:** FEFI enabled applies to 100BASE-FX mode only Each LED, VSS, and VDDO pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. The CONFIG[10:0] pins should not be left floating. See “Hardware Configuration” on page 72.

Table 21: Clock/Configuration/Reset (Continued)

128-Pin LQFP Package	Pin Name	Type	Description
111	CONFIG9	Input	CONFIG9 pin. This global configuration pin is used to configure ENA_XC, CLASS_A/B and ENA_EDET by connecting this pin to an LED output, VDDO, or VSS pin as follows: VSS (000) = No Crossover, Back Plane drivers, Energy Detect disabled P0_LED0 (001) = No Crossover, Back Plane drivers, Energy Detect Enabled P0_LED1 (010) = No Crossover, CAT 5 drivers, Energy Detect disabled P0_LED2 (011) = No Crossover, CAT 5 drivers, Energy Detect enabled P1_LED0 (100) = Auto Crossover, Back Plane drivers, Energy Detect disabled P1_LED1 (101) = Auto Crossover, Back Plane drivers, Energy Detect enabled P1_LED2 (110) = Auto Crossover, CAT 5 drivers, Energy Detect disabled VDDO (111) = Auto Crossover, CAT 5 drivers, Energy Detect enabled - default Each LED, VSS, and VDDO pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. They should not be left floating. See “Hardware Configuration” on page 72.

Table 21: Clock/Configuration/Reset (Continued)

128-Pin LQFP Package	Pin Name	Type	Description
110	CONFIG10	Input	CONFIG10 pin. This global configuring pin is used to configure PHY_ADR[4], and PHY_ADR[3] by connecting this pin to an LED output, or VSS pin as follows: VSS (000) = PHYADR[4:3] = 00 P0_LED1 (010) = PHYADR[4:3] = 01 P1_LED0 (100) = PHYADR[4:3] = 10 P1_LED2 (110) = PHYADR[4:3] = 11 Each LED and VSS pin is hardwired to a constant value. The values associated to the CONFIG[10:0] pins are latched at the de-assertion of hardware reset. They should not be left floating. See “Hardware Configuration” on page 72.
113	NORMAL	Input	Test pin. This pin should be left floating.
109	RESETn	Input	Hardware reset. Active low. REFCLK must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be pulled high for normal operation.
102	SEL_25V	Input	Output clamping voltage selection. If the digital I/O pins are operating at 2.5V, tie this pin to 2.5V. If the digital I/O pins are operating at 3.3V, tie this pin to ground. Refer to “VDDO” on page 46.

Table 22: Regulator & Reference

128-Pin LQFP Package	Pin Name	Type	Description
125	RSET	Input	Constant voltage reference. External 2 kohm 1% resistor connection to GND is required for this pin.
123	CONTROL	Output	Regulator Control Pin. This pin connects to the base of an external BJT for internal voltage regulation of 1.5V.

Table 23: Power & Ground

128-Pin LQFP Package	Pin Name	Type	Description
49 57 65 75 91 103	VDDO	Power	3.3V / 2.5V Power to digital I/O SEL_2.5V is used to choose between 3.3V and 2.5V.
9 20 31 42 124 126	AVDDAH	Power	2.5V Power to analog core
1 6 12 17 23 28 34 39	AVDDAL	Power	1.5V Power to analog core
58 62 104 107	VDD	Power	1.5V Power to digital core
EPAD	VSS	Ground	Ground to device. The 88E3083 device is contained in the 128-pin LQFP package with an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the "88E3083 128-pin 14x20 LQFP package" on page 159 for the exact location and dimensions of the EPAD.

1.4.1 128-Pin PQFP Assignments - Alphabetical by Signal Name

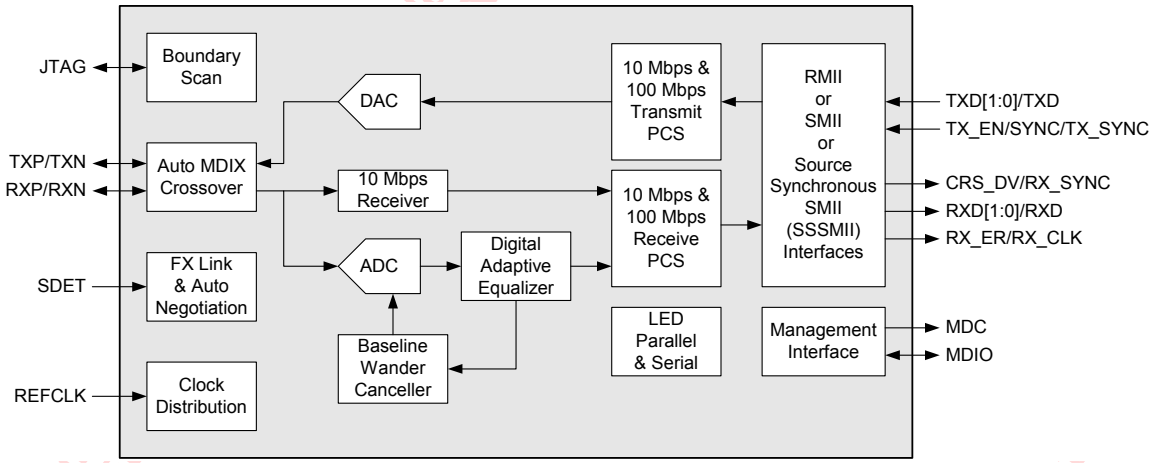
Pin #	Pin Name	Pin #	Pin Name
9	AVDDAH	128	P0_RXN
20	AVDDAH	127	P0_RXP
31	AVDDAH	85	P0_RXD
42	AVDDAH	3	P0_TXN
124	AVDDAH	2	P0_TXP
126	AVDDAH	89	P0_TXD
1	AVDDAL	98	P1_LED0
6	AVDDAL	97	P1_LED1
12	AVDDAL	96	P1_LED2
17	AVDDAL	7	P1_RXN
23	AVDDAL	8	P1_RXP
28	AVDDAL	84	P1_RXD
34	AVDDAL	4	P1_TXN
39	AVDDAL	5	P1_TXP
122	CONFIG0	88	P1_TXD
101	CONFIG1	94	P2_LED0
95	CONFIG2	93	P2_LED1
121	CONFIG3	92	P2_LED2
120	CONFIG4	11	P2_RXN
119	CONFIG5	10	P2_RXP
69	CONFIG6	79	P2_RXD
64	CONFIG7	14	P2_TXN
112	CONFIG8	13	P2_TXP
111	CONFIG9	82	P2_TXD
110	CONFIG10	56	P3_LED0
123	CONTROL	55	P3_LED1
105	INTn	54	P3_LED2
108	MDC	18	P3_RXN
106	MDIO	19	P3_RXP
113	NORMAL	78	P3_RXD
61	P0_LED0	15	P3_TXN
60	P0_LED1	16	P3_TXP
59	P0_LED2	81	P3_TXD

Pin #	Pin Name	Pin #	Pin Name
53	P4_LED0	70	P7_RXD
52	P4_LED1	37	P7_TXN
51	P4_LED2	38	P7_TXP
22	P4_RXN	72	P7_TXD
21	P4_RXP	43	P7_SDET
77	P4_RXD	83	REFCLK
25	P4_TXN	109	RESETn
24	P4_TXP	125	RSET
80	P4_TXD	63	RSVD1
50	P5_LED0	86	RX_SYNC
48	P5_LED1	87	RX_CLK
47	P5_LED2	102	SEL_25V
29	P5_RXN	100	SMII_MODE[0]
30	P5_RXP	99	SMII_MODE[1]
76	P5_RXD	116	TCK
26	P5_TXN	115	TDI
27	P5_TXP	114	TDO
74	P5_TXD	117	TMS
68	P6_LED0	118	TRSTn
67	P6_LED1	90	TX_SYNC
66	P6_LED2	58	VDD
33	P6_RXN	62	VDD
32	P6_RXP	104	VDD
71	P6_RXD	107	VDD
36	P6_TXN	49	VDDO
35	P6_TXP	57	VDDO
73	P6_TXD	65	VDDO
46	P7_LED0	75	VDDO
45	P7_LED1	91	VDDO
44	P7_LED2	103	VDDO
40	P7_RXN	EPAD	VSS (EPAD Center ground plate)
41	P7_RXP		

Section 2. Functional Description

Figure 3 shows the functional block for each port of the 88E3082/88E3083 devices. The transmitter and transmit PCS block are fully described on page 63. The receiver and receive PCS block are fully described on page 64.

Figure 3: 88E3082/88E3083 Devices Functional Block Diagram



2.1 MAC Interface

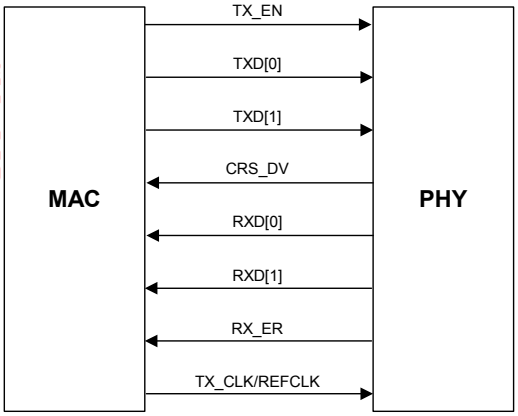
The 88E3082/88E3083 devices interface to eight 10/100 Media Access Controllers (MAC). The interfaces that are available for each device are listed in Table 1, “88E3082/88E3083 Devices Feature Differences,” on page 4.

All ports on the devices operate in the same interface mode that is selected.

2.1.1 Reduced Media Independent Interface (RMII)

The reduced media independent interface (RMII) is compliant to the RMII Consortium’s RMII Rev. 1.2 specification.

Figure 4: RMII Signal Diagram

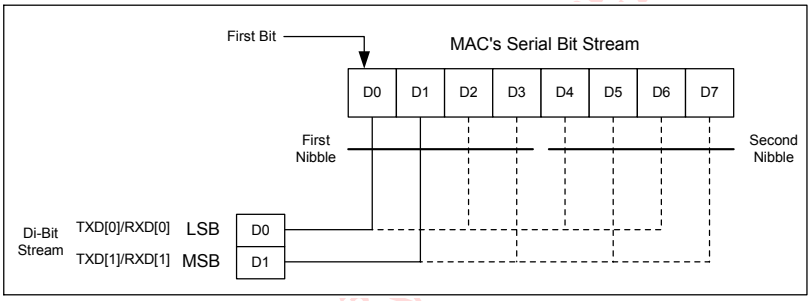


The REFCLK pin that supplies the 50 MHz reference clock to the 88E3082 device is used as the RMII REFCLK signal. All RMII signals with the exception of the assertion of CRS_DV are synchronous to REFCLK.

2.1.2 Di-Bit Presentation of Transmit and Receive Data

Each octet is transmitted and received one di-bit at a time in the order shown in Figure 5.

Figure 5: RMII Bit Ordering



2.1.3 Receive Path

Figure 6 shows the relationship among REFCLK, CRS_DV, RXD[1:0], and RX_ER during a receive of valid packet. Carrier sense is detected, which causes CRS_DV to assert asynchronously to REFCLK. The receive data is then placed into the FIFO for re-synchronization. After a minimum of 12 bits are placed into the FIFO, the receive data is presented onto RXD[1:0] synchronously to REFCLK. Note that while the FIFO is filling up RXD[1:0] is set to 00 until the first received di-bit of preamble (01) is presented onto RXD[1:0]. When carrier sense is de-asserted at the end of a packet, CRS_DV is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0] synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0], then on the second di-bit of a nibble CRS_DV reasserts. This pattern of assertion and de-assertion continues until all receive data in the FIFO has been presented onto RXD[1:0]. RX_ER is inactive for the duration of the received valid packet

Figure 6: RMII Reception with no errors

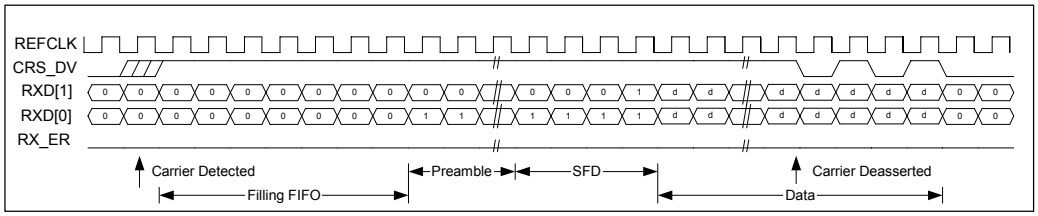


Figure 7 shows the relationship among REFCLK, CRS_DV, RXD[1:0], and RX_ER during a received false carrier event. CRS_DV is asserted asynchronously to REFCLK as in the valid receive case. However, once false carrier is detected, RXD[1:0] is set to 10 and RX_ER is asserted. Both RXD[1:0] and RX_ER transition synchronously to REFCLK. Note that the received data is not sent through the FIFO in a false carrier event and that CRS_DV and RX_ER are de-asserted synchronously to REFCLK after carrier sense is de-asserted.

Figure 7: RMII Reception with False Carrier

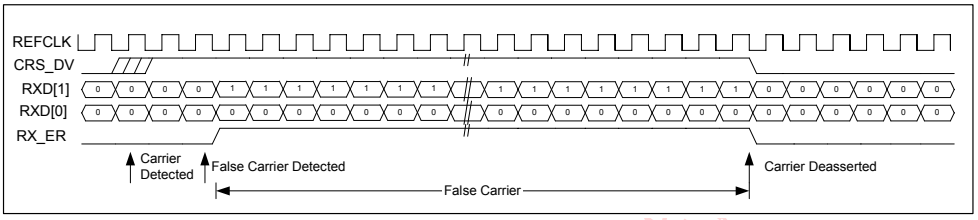
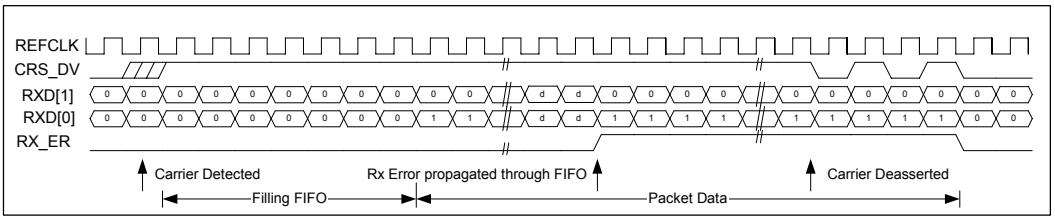


Figure 8 shows the relationship among REFCLK, CRS_DV, RXD[1:0], and RX_ER during a received symbol error event. The packet with the symbol error is treated as if it were a valid packet with the exception that all di-bits after the occurrence of the symbol error are substituted with the 01 pattern.

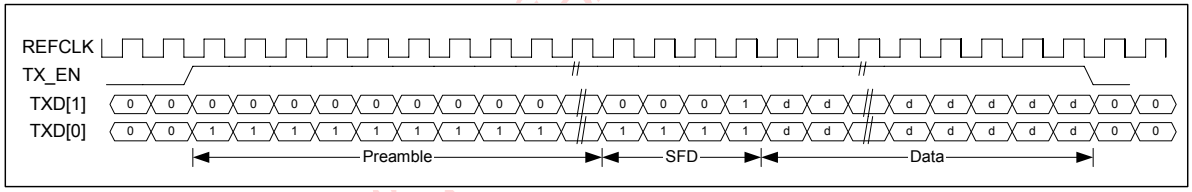
Figure 8: RMII Reception with Receive Error



2.1.4 Transmit Path

Figure 9 shows the relationship among REFCLK, TX_EN, and TXD[1:0] during a transmit event. TX_EN and TXD[1:0] toggle synchronously to REFCLK. When TX_EN is asserted, it indicates that TXD[1:0] contains valid data to be transmitted. When TX_EN is de-asserted, TXD[1:0] is ignored. If an odd number of di-bits is presented to TXD[1:0] and TX_EN, the final di-bit is ignored.

Figure 9: RMII Transmission



2.1.5 10BASE-T Differences

2.1.5.1 Receive Path

When the RMII is operating in 10BASE-T mode, CRS_DV, RXD[1:0], and RX_ER can transition only once per 10 REFCLK cycles. It does not matter which cycle in the 10 consecutive REFCLK cycles the data is sampled on as long as the samples are spaced 10 REFCLK cycles apart. False carrier and symbol error do not apply in the 10BASE-T mode.

In 10BASE-T mode, it is possible that the number of preamble bits and the number of frame bits received are not integer nibbles. The preamble is always padded up (if needed) such that the SFD appears on the RMII aligned to the nibble boundary. Extra bits at the end of the frame that do not complete a nibble are truncated.

Note

The assertion of CRS_DV is asynchronous to REFCLK as well as to the 10 REFCLK cycle boundary.

2.1.5.2 Transmit Path

In 10BASE-T mode, each di-bit must be repeated 10 times by the MAC. When the RMII is operating in 10BASE-T mode, TX_EN and TXD[1:0] toggle synchronously to REFCLK. When TX_EN is asserted, it indicates that TXD[1:0] contain valid data to be transmitted.

2.1.6 Loopback and Isolation

The RMII can be placed in loopback mode by setting register 0.14 high. Isolate is not available in RMII Mode.

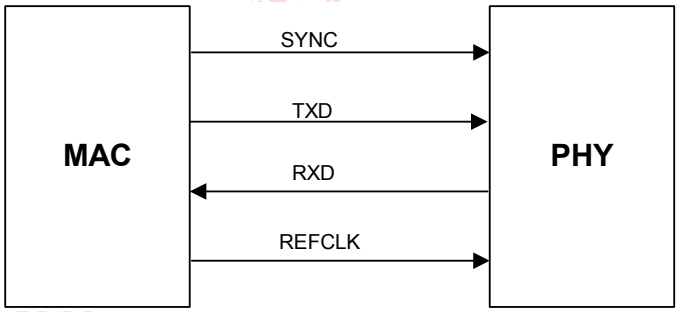
Note

The collision test (Table 51 on page 95) is not supported and does not apply to RMII. Since RMII is designed to interface with switch and MAC devices on the same board, the isolate function (Table 51 on page 95) is not supported.

2.1.7 Serial Media Independent Interface (SMII)

The serial media independent interface (SMII) conforms to the Serial MII specification Rev. 2.1.

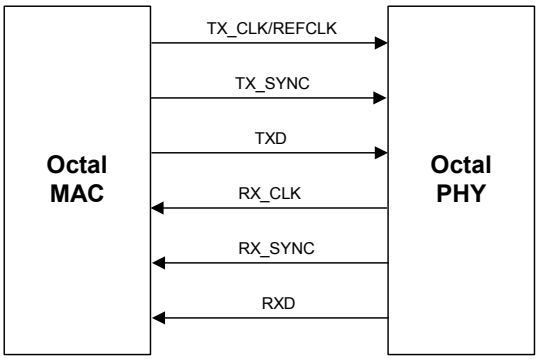
Figure 10: SMII Signal Diagram



The REFCLK pin that supplies the 125 MHz reference clock to the 88E3082/88E3083 devices is used as the SMII reference clock. All SMII signals are synchronous to REFCLK. SMII mode is enabled by setting SEL_RMII pin low and driving P1_TX_EN/SMII_MODE[1] and P1_TXD[0]/SMII_MODE[0] to 0.

2.1.8 Source Synchronous SMII (SSSMII)

Figure 11: Source Synchronous SMII Signal Diagram



Source synchronous SMII (SSSMII) is designed for applications requiring a trace delay of more than 1 ns. Three signals are added to the SMII interface, and the function of SYNC is modified to be TX_SYNC. Two of the added signals, RX_SYNC and RX_CLK, synchronize RX for all ports. Similarly, the signals, TX_CLK and TX_SYNC, synchronize TX for all ports. RX_CLK is frequency locked, but not phase locked to REFCLK.

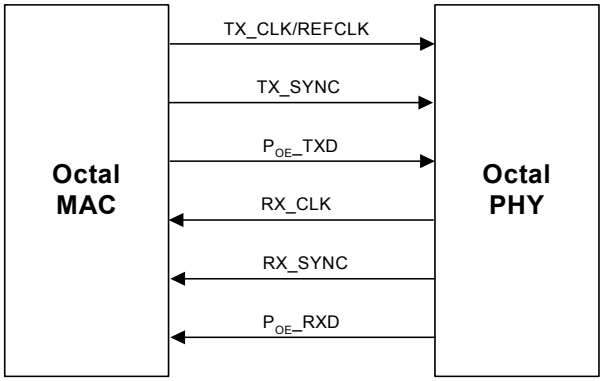
Source Synchronous SMII mode is enabled by setting SEL_RMII pin low and setting P1_TX_EN/SMII_MODE[1] to 0 and P1_TXD[0]/SMII_MODE[0] to 1. For the 88E3082 in this mode, P3_CRS_DV becomes RX_SYNC, P3_RX_ER becomes RX_CLK, and P3_TXD1 becomes TX_SYNC.

The rest of the receive and transmit paths in source synchronous mode operate identically to the SMII interface.

2.1.9 Double Data Rate SSSMII (DDR-SSSMII)

DDR-SSSMII is designed such that the positive edge of the signal corresponds to the odd port i.e Ports 1,3,5,7, and the negative edge corresponds to the even port. i.e Ports 0,2,4,6. In one RX_CLK cycle, the data for one odd and one even port such as P0_RXD and P1_RXD data is passed.

Figure 12: DDR-SSSMII Signal Diagram



The SMII_MODE[1:0] pins determine which SMII mode is enabled for all 8 ports. Refer to Table 24 for details.

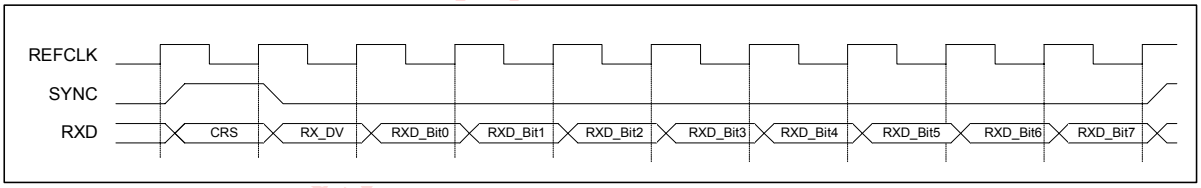
Table 24: SMII/SSSMII/DDR-SSSMII Mode Selection

SMII_MODE[1]	SMII_MODE[0]	Mode
Low	Low	SMII
Low	High	SSSMII
High	High	DDR-SSSMII

2.1.10 Receive Path

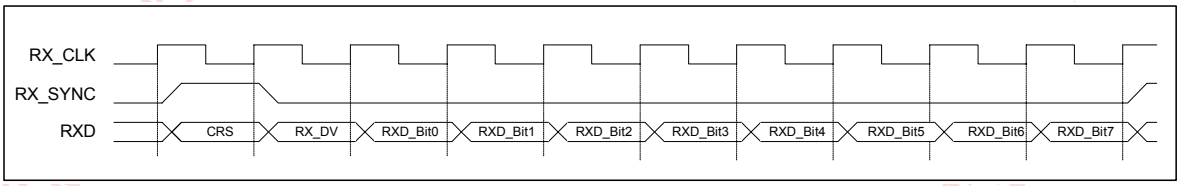
Receive data and control information is grouped in 10-bit segments that are delimited by the SYNC signal (or RX_SYNC when in SSSMII or DDR-SSSMII mode) as shown in Figure 13. In 100BASE-T or 100BASE-FX mode, each segment represents a new byte of data. In 10BASE-T mode, each segment is repeated ten times. The MAC can sample any one of every 10 segments in 10BASE-T mode. The MAC must generate a SYNC pulse once every 10 clock cycles.

Figure 13: SMII Receive Data Path Timing Diagram



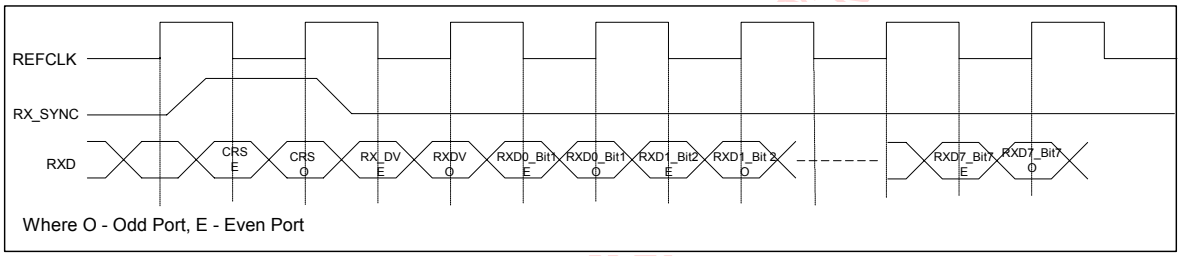
In SSSMII mode, REFCLK and SYNC are no longer common for both transmit and receive. They are renamed to RX_CLK and RX_SYNC. Refer to the “88E3082 Pin Description” on page 11 and “88E3083 Pin Description” on page 35 to determine the pin used for these signals in this mode.

Figure 14: SSSMII Receive Data Path Timing Diagram



In DDR-SSSMII mode, data from 2 ports are multiplexed on one data line. Therefore, there are 4 RXD pins and 4 TXD pins for the 8 ports, thereby further reducing the number of interface pins required for switch applications.

Figure 15: DDR-SSSMII Receive Data Path Timing Diagram



When RX_DV bit is high, RXD_Bit[7:0] are used to convey packet data. When RX_DV bit is low, RXD_Bit[7:0] are used to convey PHY status.

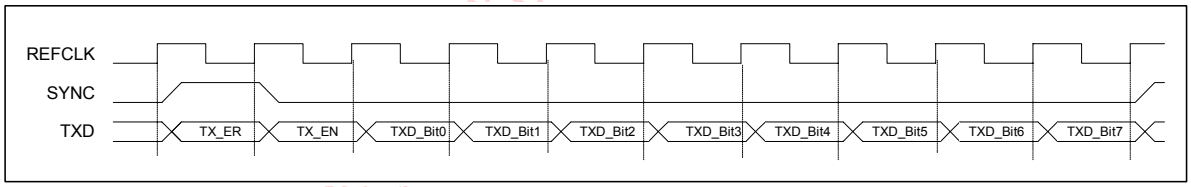
Table 25: SMII, SSSMII, and DDR-SSSMII Receive Data Encoding

CRS	RX_DV	RXD_Bit0	RXD_Bit1	RXD_Bit2	RXD_Bit3	RXD_Bit4	RXD_Bit5	RXD_Bit6	RXD_Bit7
x	0	RX_ER from previous frame	Speed 0 = 10 Mbps 1 = 100 Mbps	Duplex 0 = Half 1 = Full	Link 0 = Down 1 = Up	Jabber 0 = OK 1 = Error	Upper Nibble 0 = Invalid 1 = Valid	False Carrier 0 = Not Detected 1 = Detected	1
x	1	One Data Byte (Two MII Data Nibbles)							

2.1.11 Transmit Path

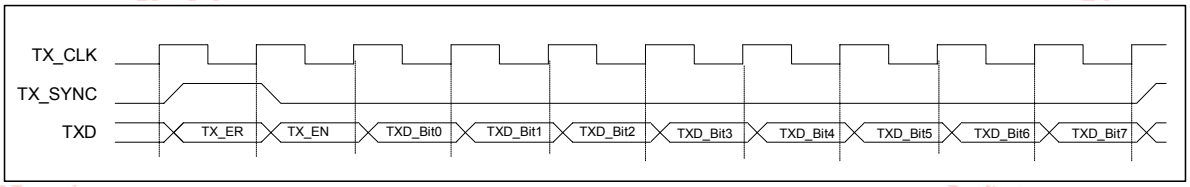
Transmit data is grouped in 10-bit segments that are delimited by the SYNC signal (or TX_SYNC when in SSSMII or DDR-SSSMII mode) as shown in Figure 16. In 100BASE-X mode, each segment represents a new byte of data. In 10BASE-T mode, each segment must be repeated 10 times by the MAC. In this mode, the MAC must generate the same data in each of the 10 segments.

Figure 16: SMII Transmit Data Timing Diagram



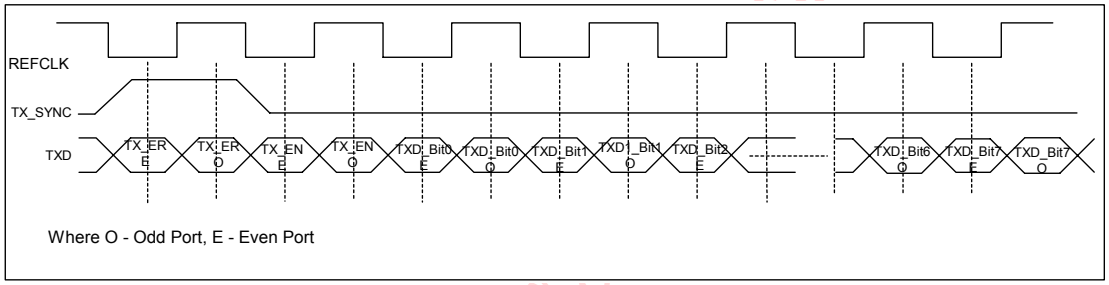
In SSSMII mode, REFCLK and SYNC are no longer common for both transmit and receive. They are renamed to TX_CLK and TX_SYNC. Refer to the “88E3082 Pin Description” on page 11 and “88E3083 Pin Description” on page 35 to determine the pin used for these signals in this mode.

Figure 17: SSSMII Transmission



In DDR-SSSMII mode, data from 2 ports are multiplexed on one data line. Therefore, there are 4 RXD pins and 4 TXD pins for the 8 ports, thereby further reducing the number of interface pins reduced for switch applications.

Figure 18: DDR-SSSMII Transmission



The 88E3082/88E3083 devices ignore any data segment when the TX_EN bit for the designated port is equal to zero as shown in Table 26.

Table 26: SMII, SSSMII, and DDR-SSSMII Transmit Data Encoding

TX_ER	TX_EN	TXD_Bit0	TXD_Bit1	TXD_Bit2	TXD_Bit3	TXD_Bit4	TXD_Bit5	TXD_Bit6	TXD_Bit7
X	0	X	X	X	X	X	X	X	X
X	1	One Data Byte (Two MII Data Nibbles)							

2.1.12 Loopback and Isolation

The SMII, SSSMII, and DDR-SSSMII modes can be placed in the loopback mode by setting register 0.14 high. Isolate is not available in SMII, SSSMII, and DDR-SSSMII modes.

Note

The collision test (Table 51 on page 95) is not supported by the SMII/SSSMII/DDR-SSSMII interfaces. Since these interfaces are designed to interface with switch and MAC devices on the same board, the isolate function (Table 51 on page 95) is not supported.

2.2 Serial Management Interface

The serial management interface provides access to the internal registers via the MDC and MDIO pins and is compliant to IEEE 802.3u section 22. MDC is the management data clock input and can run from DC to a maximum rate of 8.33 MHz. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin requires a 1.5 kohm pull-up resistor that pulls the MDIO high during idle and turnaround times.

2.2.1 MDC/MDIO Read and Write Operations

All the relevant serial management registers are implemented as well as several optional registers. A description of the registers can be found in “Register Description” on page 93.

Figure 19: Typical MDC/MDIO Read Operation

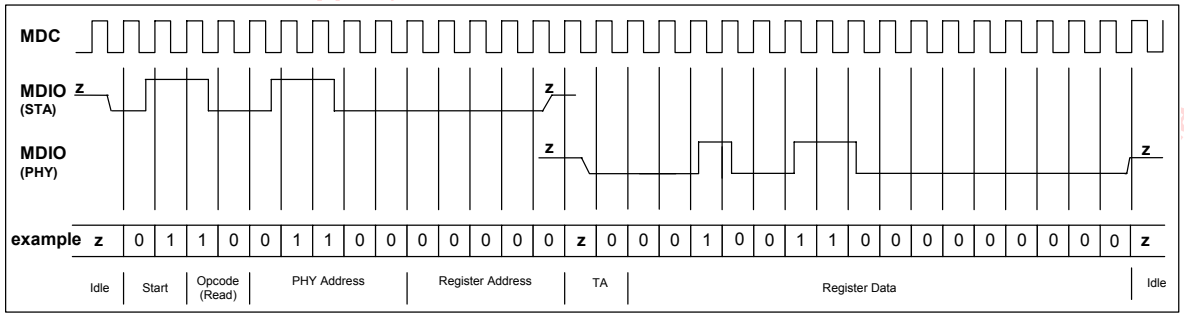


Figure 20: Typical MDC/MDIO Write Operation

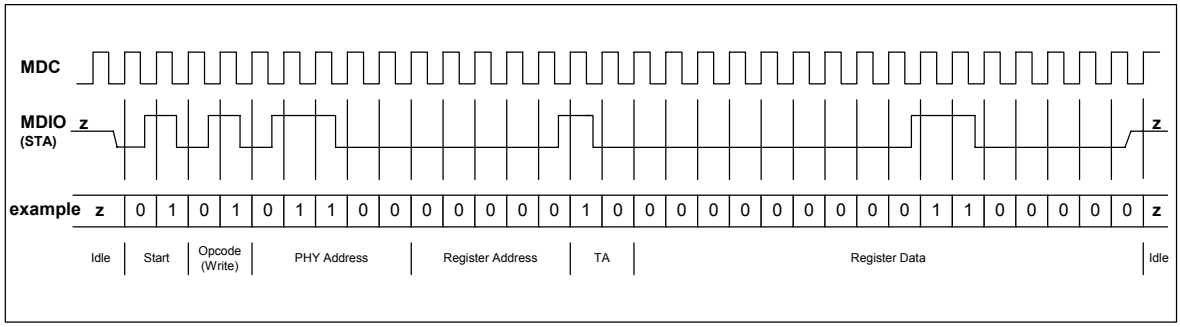


Table 27 is an example of a read operation.

Table 27: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	Opcode Read = 10 Write = 01	5-Bit Phy Device Address	5-Bit Phy Register Address	2-Bit Turn-around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.2.2 Preamble Suppression

The 88E3082/88E3083 devices are permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.2.3 Programming Interrupts

The interrupt function drives the INTn pin low whenever an interrupt event is enabled by programming register 18. This function minimizes the need for polling via the serial management interface. Table 28 shows the interrupts that may be programmed.

Table 28: Programmable Interrupts

Register Address	Programmable Interrupts
18.15	DTE Detect State Changed Interrupt Enable
18.14	Speed Changed Interrupt Enable
18.13	Duplex Changed Interrupt Enable
18.12	Page Received Interrupt Enable
18.11	Auto-Negotiation Completed Interrupt Enable
18.10	Link Status Changed Interrupt Enable
18.9	Symbol Error Interrupt Enable
18.8	False Carrier Interrupt Enable
18.7	FIFO Over/Underflow Interrupt Enable
18.6	MDI/MDIX Crossover Changed
18.5:4	Duplex (Reserved in the 88E3083 device)
18.3:2	Error (Reserved in the 88E3083 device)
18.1:0	COLX (Reserved in the 88E3083 device)

Register 18 determines whether the INTn pin is asserted when an interrupt event occurs. Register 19 reports interrupt status. When an interrupt event occurs, the corresponding bit in register 19 is set and remains set until register 19 is read via the serial management interface. When interrupt enable bits are not set in register 18, interrupt status bits in register 19 are still set when the corresponding interrupt events occur. However, the INTn pin is not asserted.

The INTn pin is low as long as at least one interrupt status bit is set in register 19 with its corresponding interrupt enable bit set in register 18.

To de-assert the INTn pin:

- Clear of register 19 via a serial management read
- Disable the interrupt enable by writing register 18

Register 20, a global register for all ports, lists the ports that have active interrupts. Register 20 provides a quick way to isolate the interrupt so that the MAC or switch does not have to poll register 19 for all ports. Reading register 20 does not de-assert the INTn pin.

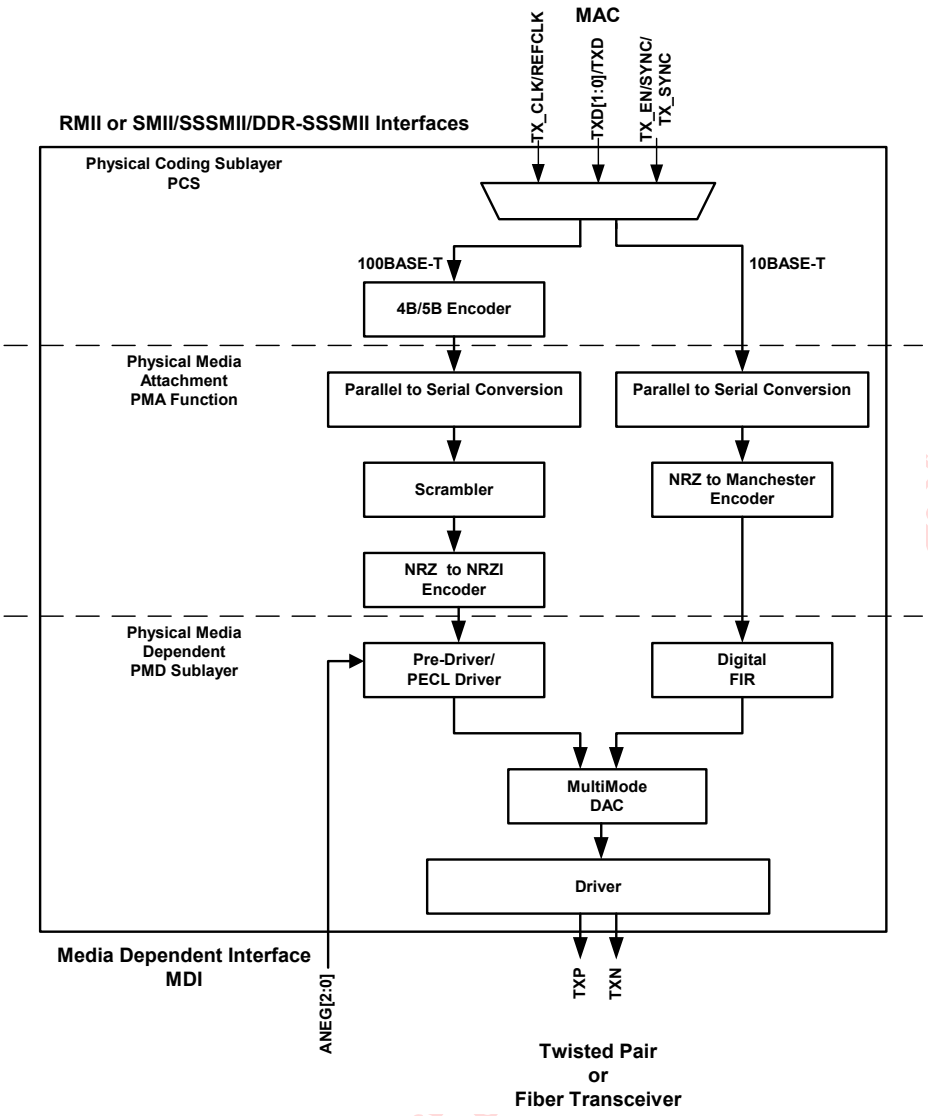
Note

Register 20 can be accessed by reading register 20 using the PHY address of any of the eight ports.

2.3 Transmit and Receive Functions

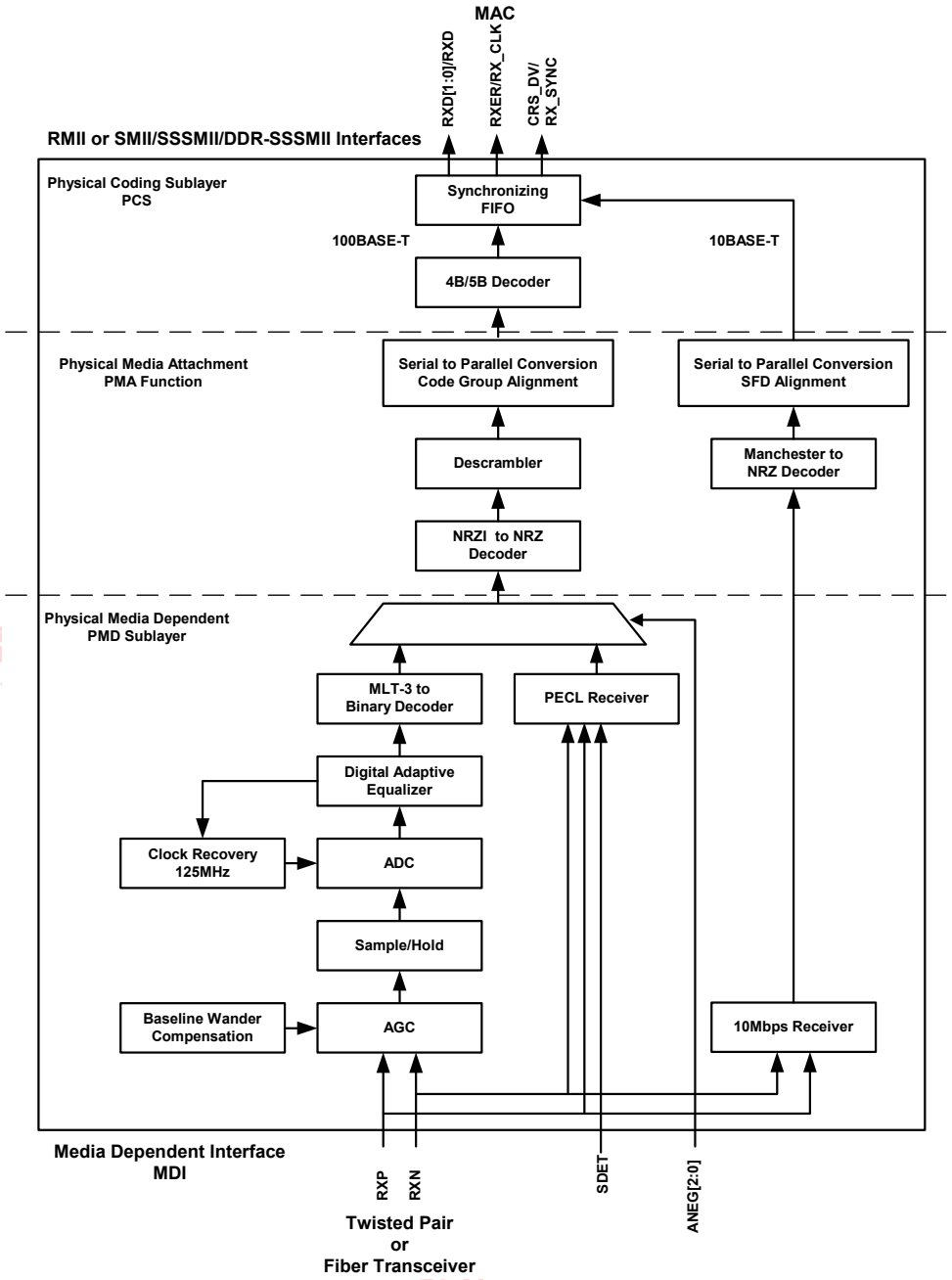
The transmit block in Figure 21 shows the transmit path for twisted pair or fiber connection of the 88E3082/ 88E3083 devices.

Figure 21: Transmit Block Diagram



The receive block in Figure 22 shows the receive path for twisted pair or fiber connection of the 88E3082/88E3083 devices.

Figure 22: Receive Block Diagram



2.3.1 Transmit PCS and PMA

2.3.1.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks that convert synchronous 4-bit nibble data to a scrambled MLT-3 125 Mbps serial data stream.

2.3.1.2 4B/5B Encoding

For 100BASE-TX mode, the 4-bit nibble is converted to a 5-bit symbol with /J/K/ start-of-stream delimiters and /T/R/ end-of-stream delimiters inserted as needed. The 5-bit symbol is then serialized and scrambled.

2.3.1.3 Scrambler

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive OR'ing the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit repeating pseudo-random sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

Note

The enabling and disabling of the scrambler and the far end fault generator are controlled in the same way as for the descrambler detection and far end fault detection on the receive side as mentioned in the sections below.

2.3.1.4 NRZ to NRZI Conversion

The data stream is converted from NRZ to NRZI.

2.3.1.5 Pre-Driver and Transmit Clock

The 88E3082/88E3083 devices use an all digital clock generator circuit to create all the needed receive and transmit clocks in 100BASE-TX, 100BASE-FX, and 10BASE-T modes of operation.

For 100BASE-TX mode, the transmit data is converted to MLT-3 coded symbols. The digital time base generator (TBG) produces the locked 125 MHz transmit clock.

For 100BASE-FX mode, NRZI data is presented directly to the multimode DAC.

For 10BASE-T mode, the transmit data is converted to Manchester encoding. The digital time base generator (TBG) produces the 10 MHz transmit reference clock as well as the over-sampling clock for 10BASE-T waveshaping.

If the 88E3082/88E3083 devices are operating in 10 Mbps the JabberDet bit is enabled (Table 52 on page 97) and a jabber condition occurs, the transmit path is forced into idle until, and CRS_DV is asserted in the RMII mode or the CRS bit is set until the jabber condition ends.

2.3.1.6 Multimode Transmit DAC

The multimode transmit digital to analog converter (DAC) transmits MLT-3 coded symbols in 100BASE-TX mode, NRZI symbols in 100BASE-FX mode, and Manchester-coded symbols in 10BASE-T mode. The transmit DAC utilizes a direct drive current driver which is well balanced to produce very low common mode transmit noise.

In 100BASE-TX mode, the multimode transmit DAC performs slew control to minimize high frequency EMI.

In 100BASE-FX mode, the pseudo ECL level is generated through external resistive terminations.

In 10BASE-T mode, the multimode transmit DAC generates the needed pre-equalization waveform. This pre-equalization is achieved by using a digital FIR filter.

2.3.1.7 Driver

The driver is an amplifier. It conforms the analog signal level from the DAC to the requirements of the twisted pair cable or fiber transceiver. The differential TXP and TXN are shared by the 100BASE-TX, 100BASE-FX, and 10BASE-T transmitters.

2.3.2 Receive PCS and PMA

2.3.2.1 10-BASE-T/100BASE-TX Receiver

The differential RXP and RXN pins are shared by the 100BASE-TX, 100BASE-FX, and 10BASE-T receivers.

The 100BASE-TX receiver consists of several functional blocks that convert the scrambled MLT-3 125 Mbps serial data stream to synchronous 4-bit nibble data presented to the RMII interfaces.

2.3.2.2 AGC and Baseline Wander

In 100BASE-TX mode, after input to the AGC block the signal is compensated for baseline wander with a digitally controlled Digital to Analog converter (DAC). It automatically removes the DC offset from the input before it reaches the ADC input.

2.3.2.3 ADC and Digital Adaptive Equalizer

In 100BASE-T mode, an analog to digital converter (ADC) samples and quantizes the input analog signal and sends the result into the digital adaptive equalizer. The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

2.3.2.4 Digital Phased Locked Loop (DPLL)

In 100BASE-TX mode, the receive clock is locked to the incoming data stream and extracts a 125 MHz reference clock. The input data stream is quantized by the recovered clock and sent through to the digital adaptive equalizer from each port.

Digital interpolator clock recovery circuits are optimized for MLT-3, NRZI, and Manchester modes. A digital approach makes the 88E3082/88E3083 devices receiver paths robust to the presence of variations in process, temperature, on-chip noise, and supply voltage.

2.3.2.5 NRZI to NRZ Conversion

In 100BASE-TX mode, the recovered 100BASE-TX NRZI signal from the receiver is converted to NRZ data, descrambled, aligned, parallelized, and 5B/4B decoded.

2.3.2.6 Descrambler

The descrambler is initially enabled upon hardware reset if 100BASE-TX is selected. The scrambler can be enabled or disabled via software by setting the DisScrambler bit (Table 68 on page 108).

The descrambler “locks” to the descrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization.

The receiver descrambles the incoming data stream by exclusive ORing it with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence.

The descrambler is always forced into the “unlocked” state when a link failure condition is detected or when insufficient idle symbols are detected.

2.3.2.7 Serial to Parallel Conversion and 5B/4B Code-Group Alignment

The Serial to Parallel /Symbol Alignment block performs serial to parallel conversion and aligns 5B code-groups to a nibble boundary.

2.3.2.8 5B/4B Decoder

The 5B/4B decoder translates 5B code-groups into 4B nibbles to be presented to the MAC interfaces. The 5B/4B code mapping is shown in Table 29.

2.3.2.9 FIFO

The 100BASE-X or 10BASE-T packet is placed into the FIFO in order to correct for any clock mismatch between the recovered clock and the reference clock REFCLK.

2.3.2.10 100BASE-FX Receiver

In 100BASE-FX mode, a pseudo-ECL (PECL) receiver is used to decode the incoming NRZI signal passed to the NRZI-NRZ decoder. The NRZI signal from the receiver is converted to NRZ data, aligned, parallelized, and 5B/4B decoded as in the 100BASE-TX mode.

2.3.2.11 Far End Fault Indication (FEFI)

When 100BASE-FX is selected and bit 0 of CONFIG8 is high at hardware reset, then the far end fault detect (FEFD) circuit is enabled. The FEFD enable state can be overridden by programming the DisFEFI bit (Table 68 on page 108).

Note

The FEFI function is always disabled if 100BASE-TX is selected.

2.3.2.12 10BASE-T Receiver

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ and then aligned. The alignment is necessary to ensure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

In 10BASE-T mode, a receiver is used to decode the differential voltage offset of the Manchester data. Carrier sense is decoded by measuring the magnitude of the voltage offset.

In this mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ data. The data stream is converted from serial to parallel format and aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to a byte or nibble boundary.

For cable lengths greater than 100 meters, the incoming signal has more attenuation. Hence, the receive voltage threshold should be lowered via the Extended Distance bit in the PHY Specific Control Register (Table 68 on page 108).

Table 29: 5B/4B Code Mapping

PCS Code-Group [4:0] 4 3 2 1 0	Name	TXD/RXD <3:0> 3 2 1 0	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; used as inter-stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid code
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code

Table 29: 5B/4B Code Mapping

PCS Code-Group [4:0] 4 3 2 1 0	Name	TXD/RXD <3:0> 3 2 1 0	Interpretation
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

2.3.3 Setting Cable Characteristics

Since cable characteristics are different between unshielded twisted pair and shielded twisted pair cable, optimal receiver performance can be obtained in 100BASE-TX and 10BASE-T modes by setting the TPSelect bit in the PHY Specific Control Register (Table 68 on page 108) for cable type.

2.3.4 Scrambler/Descrambler

The scrambler block is initially enabled upon hardware reset if 100BASE-TX is selected. If 100BASE-FX or 10BASE-T is selected, the scrambler is disabled by default. The scrambler is controlled by programming the DisScrambler bit in the PHY Specific Control Register (Table 68 on page 108).

The scrambler setting is also controlled by hardware configuration at the end of hardware reset. Table 30 shows the effect of various configuration settings on the scrambler.

Table 30: Scrambler Settings

CONFIG[7:0]	DisScrambler Bit (Table 68 on page 108)	Scrambler/ Descrambler
11X (FX selected)	HW reset to 1	Disabled
0XX or 10X(Copper selected)	HW reset to 0	Enabled
X	User set to 1	Disabled
X	User set to 0	Enabled (in copper mode only)

2.3.5 Digital Clock Recovery/Generator

The 88E3082/88E3083 devices use an all digital clock recovery and generator circuit to create all the needed receive and transmit clocks. The digital time base generator (TBG) takes the 50 MHz (88E3082 device only) or 125 MHz reference input clock (XTAL_IN) and produces the locked 125 MHz transmit clock for the MAC in 100BASE-TX mode. It produces a 10 MHz transmit clock for the MAC in 10BASE-T mode as well as the over-sample clock for 10BASE-T wave-shaping.

Table 31: Generated Clocks

Reference Input Clock	Mode	TBG Frequency	
		MAC Transmit Clock	MAC Receive Clock
50 MHz (88E3082 only) or 125 MHz	100BASE-X	Locked 25 MHz	Recovered 25 MHz
	10BASE-T	2.5 MHz	2.5 MHz

2.3.6 Link Monitor

The link monitor is responsible for determining whether link is established with a link partner.

In 10BASE-T mode, link monitor function is performed by detecting the presence of the valid link pulses on the RXP/N pins.

In 100BASE-TX mode, the link is established by scrambled idles

In 100BASE-FX mode, the external fiber-optic receiver performs the signal detection function and communicates this information with the 88E3082/88E3083 devices through SDET pins for all individual ports.

If Force Link Good (ForceLink bit is set high - PHY Specific Control Register, Table 68 on page 108), the link is forced to be good, and the link monitor is bypassed. Pulse checking is disabled if Auto-Negotiation is disabled, and DisNLPCheck (PHY Specific Control Register, Table 68 on page 108) is set high. If Auto-Negotiation is disabled and DisNLPGen (PHY Specific Control Register, Table 68 on page 108) is set high, then the link pulse transmission is disabled.

2.3.7 Auto-Negotiation

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset
- Restart Auto-Negotiation
- Transition from power down to power up
- Changing from the *link-up* state to the *linkfail* state

If Auto-Negotiation is enabled, then the 88E3082/88E3083 devices negotiate with the link partner to determine the speed and duplex with which to operate. If the link partner is unable to Auto-Negotiate, the 88E3082/88E3083 devices go into the parallel detect mode to determine the speed of the link partner. Under parallel detect mode, the duplex mode is fixed at half-duplex.

After hardware reset, Auto-Negotiation can be enabled and disabled via the AnegEn bit (PHY Control Register - Table 51 on page 95). When Auto-Negotiation is disabled, the speed and duplex can be changed via the SpeedLSB and Duplex bits (PHY Control Register - Table 51 on page 95), respectively. The abilities that are advertised can be changed via the Auto-Negotiation Advertisement Register (Table 55 on page 100).

2.3.8 Register Update

Changes to the AnegEn, SpeedLSB, and Duplex bits (Table 51 on page 95) do not take effect unless one of the following takes place:

- Software reset (SWReset bit - Table 51 on page 95)
- Restart Auto-Negotiation (RestartAneg bit - Table 51 on page 95)
- Transition from power down to power up (PwrDwn bit - Table 51 on page 95)
- The link goes down

The Auto-Negotiation Advertisement register (Table 55 on page 100) is internally latched once every time Auto-Negotiation enters the *ability detect* state in the arbitration state machine. Hence, a write into the Auto-Negotiation Advertisment Register has no effect once the 88E3082/88E3083 devices begin to transmit Fast Link Pulses (FLPs). This guarantees that a sequence of FLPs transmitted is consistent with one another.

The Next Page Transmit register (Table 59 on page 105) is internally latched once every time Auto-Negotiation enters the *next page exchange* state in the arbitration state machine.

2.3.9 Next Page Support

The 88E3082/88E3083 devices support the use of next page during Auto-Negotiation. By default, the received base page and next page are stored in the Link Partner Ability register - Base Page (Table 56 on page 102). The 88E3082/88E3083 devices have an option to write the received next page into the Link Partner Next Page register - Table 59 on page 105 - (similar to the description provided in the IEEE 802.3ab standard) by programming the Reg8NxtPg bit (PHY Specific Control Register - Table 68 on page 108).

2.3.10 Status Registers

Once the 88E3082/88E3083 devices complete Auto-Negotiation, the various statuses in the PHY Status (Table 52 on page 97), Link Partner Ability (Next Page)(Table 57 on page 103), and Auto-Negotiation Expansion(Table 58 on page 104) registers are updated. Speed, duplex, page received, and Auto-Negotiation completed statuses are also available in the PHY Specific Status (Table 69 on page 110) and PHY Interrupt Status (Table 71 on page 114) registers.

2.4 Power Management

The 88E3082/88E3083 devices support advanced power management modes that conserve power.

2.4.1 Low Power Modes

Two low power modes are supported in the 88E3082/88E3083 devices.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect+™

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect+™ allows the 88E3082/88E3083 devices to wake up when energy is detected on the wire with the additional capability to wake up a link partner. The 10BASE-T link pulses are sent once every second while listening for energy on the line.

2.4.1.1 IEEE Power Down Mode

The standard IEEE power down mode (22.2.4.1.5) is entered by setting the PwrDwn (Table 51 on page 95) bit equal to one. In this mode, the PHY does not respond to any MAC interface signals except the MDC/MDIO. It also does not respond to any activity on the CAT 5 cable.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable. It can only wake up by clearing the PwrDwn bit to 0.

2.4.1.2 Energy Detect +™

In this mode, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. If the 88E3082/88E3083 devices are in Energy Detect+™ mode, it can wake a connected device. When ENA_EDET is 1, the mode of operation is Energy Detect+™. The 88E3082/88E3083 devices also respond to MDC/MDIO.

2.4.1.3 Normal 10/100 Mbps Operation

Normal 10/100 Mbps operation can be entered by either using a configuration option or a register write during the energy detect mode.

2.4.2 MAC Interface and PHY Configuration for Low Power Modes

The 88E3082/88E3083 devices have one CONFIG bit dedicated to support the low power modes. The CONFIG9 pin is sampled during power-on reset and is used to select between normal modes of operation and the energy detect low power modes. Refer to the section "Hardware Configuration" for details.

Low power modes are also register programmable. The EDet bit (Table 68 on page 108) allows the user to turn on Energy Detect+™. When the low power mode is not selected, the PwrDwn bit (Table 51 on page 95) can be used. If during the energy detect mode, the PHY wakes up and starts operating in normal mode, the EDet bit settings are retained. When the link is lost and energy is no longer detected, the 88E3082/88E3083 devices return to the mode stored in the EDet bit.

Table 32 displays the low power operating mode selection.

Table 32: Operating Mode Selection

Power Mode	How to Activate Mode
IEEE Power down	PwrDwn bit write (Table 51 on page 95)
Energy Detect+™	Configuration option & register EDet bit write (Table 68 on page 108)

2.5 Hardware Configuration

The 88E3082/88E3083 devices are 8-port devices. Configuration options like physical address, PHY operating mode, Auto-Negotiation, MDI/MDIX crossover (ENA_XC), and physical connection type are configured by tying the multi-function LED pins to CONFIG[10:0]. CONFIG[10:0] pins must be tied to LED output, VDDO or GND pins based on the configuration options selected. They should not be left floating.

Note

Configuration options can be overwritten by register writes, with the exception of the PHY addresses and the physical connection type (i.e. copper or fiber).

2.5.1 SEL_RMII

This SEL_RMII pin configures the 88E3082 device for the RMII, SMII, SSSMII and DDR_SSSMII interface. Since SEL_RMII indicates whether the master clock (REFCLK) is running at 50 MHz or 125 MHz, it should be stable during the entire reset period with REFCLK running at the correct frequency. SEL_RMII should be held stable for the entire duration of normal operation. Once the RMII or any of the SMII interfaces is selected, all ports operate in the same mode.

All configuration settings with the exception of SEL_RMII are latched at the de-assertion of reset.

2.5.2 PHY Address

Each port is addressed via a unique PHY address. The lower three bits of the address are hardwired with the port number. Table 37 shows how the PHY address is assigned. For example, Port 0 is assigned with the hardwired values “000” and the upper two bits are set by the user when PHY_ADR[4:3] pins are latched at the de-assertion of hardware reset.

Note

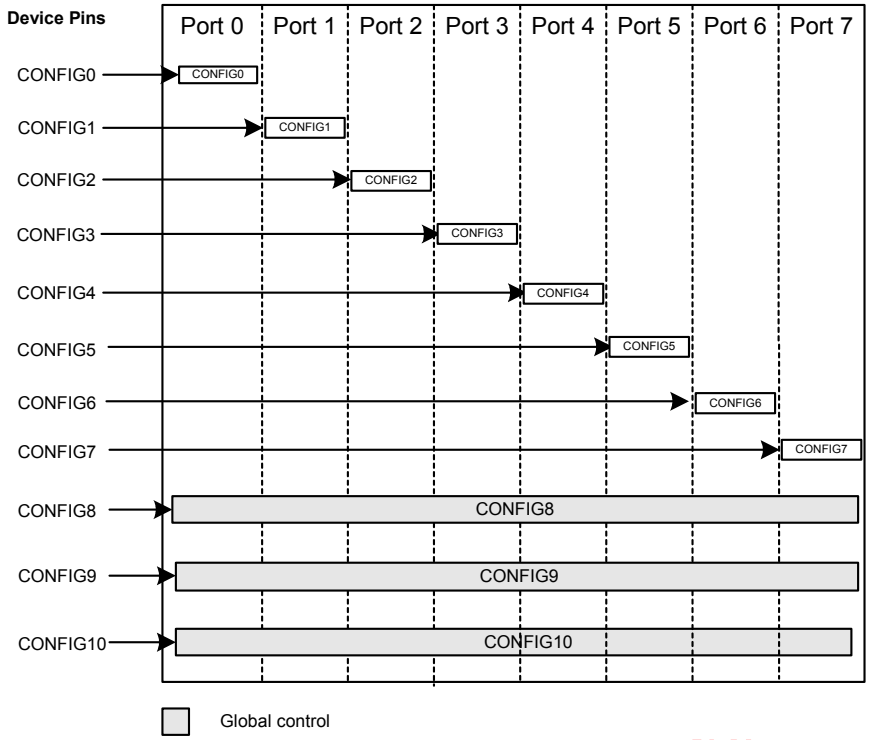
When there is a reference to an odd or even port in this document for DDR-SSSMII mode, it refers to the actual device port number where as PHY_ADR[4:0] are referring to the actual PHY address assignments.

Refer to the Table 37 for the address assignments.

2.5.3 88E3082/88E3083 Devices Configuration Description

The encoded values of the LED output are tied to CONFIG[10:0], and latched at the de-assertion of the RESETn pin. CONFIG[7:0] are tied to Ports [7:0] respectively and CONFIG[10:8] are global configuration pins that are common to all the ports.

Figure 23: 88E3082/88E3083 Devices Configuration Input



Each LED pin outputs a bit stream during initialization that is used by the CONFIG pin inputs. The bit values are latched at the de-assertion of hardware reset by the CONFIG[10:0] pins. Refer to Table 33 below for details.

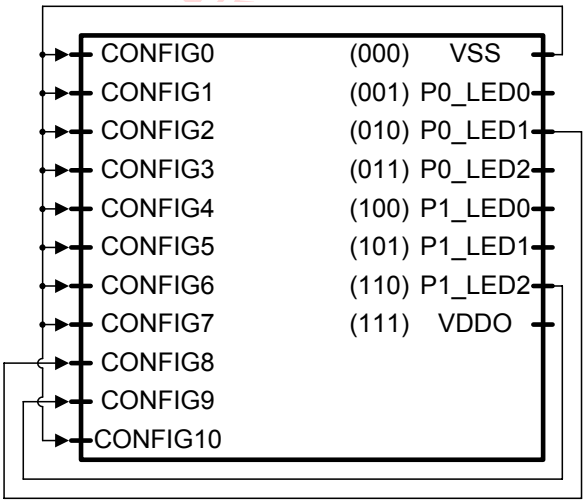
Table 33: Pin to Constant Mapping

Pins	Bit[2:0]
VSS	000
P0_LED0	001
P0_LED1	010
P0_LED2	011
P1_LED0	100
P1_LED1	101
P1_LED2	110
VDDO	111

Figure 24 illustrates a common configuration connection that will enable the conditions listed below:

- CONFIG[7:0] connected to VSS (000) - All ports 10/100BASE-T with ANEG, advertise all
- CONFIG[8] connected to P0_LED1 (010) - LED Mode1, FEFI Off
- CONFIG[9] connected to P1_LED2 (110) - Auto-crossover enable, Class B (CAT 5) drivers, Energy Detect Sleep Mode Off
- CONFIG[10] connected to VSS (000) - PHYADR[4:3] = 00 assigns PHY address for Port[7:0] of the device, Reserved = 0

Figure 24: Configuration Connection Example



The 88E3082/88E3083 devices configuration options associated to each configuration pin are shown in Table 34.

Table 34: 88E3082/88E3083 Devices Pin to Configuration Register Mapping

Pins	Bit[2][1]	Bit[1]	Bit[0
CONFIG0	P0_ANEG[2][1]	P0_ANEG[1][1]	P0_ANEG[0][1]
CONFIG1	P1_ANEG[2][1]	P1_ANEG[1][1]	P1_ANEG[0][1]
CONFIG2	P2_ANEG[2][1]	P2_ANEG[1][1]	P2_ANEG[0][1]
CONFIG3	P3_ANEG[2][1]	P3_ANEG[1][1]	P3_ANEG[0][1]
CONFIG4	P4_ANEG[2][1]	P4_ANEG[1][1]	P4_ANEG[0][1]
CONFIG5	P5_ANEG[2][1]	P5_ANEG[1][1]	P5_ANEG[0][1]
CONFIG6	P6_ANEG[2][1]	P6_ANEG[1][1]	P6_ANEG[0][1]
CONFIG7	P7_ANEG[2][1]	P7_ANEG[1][1]	P7_ANEG[0][1]
CONFIG8	LED_DEF[1]	LED_DEF[0]	EN_FEFI
CONFIG9	ENA_XC	CLASS_A/B	ENA_EDET
CONFIG10	PHYADR[4]	PHYADR[3]	Reserved - Must be = 0

1. It is possible to specify half and full-duplex per port. Refer to Table 35 for details.

Table 35: Pn_ANEG[2:0]

Where Pn_ANEG[2:0]	000 = Auto-Negotiation UTP 001 = Auto-Negotiation STP 010 = 10BASE-T Half-Duplex 011 = 10BASE-T Full-Duplex 100 = 100BASE-TX Half-Duplex 101 = 100BASE-TX Full-Duplex 110 = 100BASE-FX Half-Duplex[1] 111 = 100BASE-FX Full-Duplex[1]

1. For the 88E3083 device, 100BASE-FX mode is only available on Port 7.

Refer to Table 36 for a detailed description of the 88E3082/88E3083 devices configuration options.

Table 36: 88E3082/88E3083 Devices Configuration Register Definitions

Configuration	Description
LED_DEF[1:0]	LED default configuration See “LED Interface” on page 82 for details.
EN_FEFI	Enable FEFI 1 = Enable FEFI 0 = Disable FEFI See “Far End Fault Indication (FEFI)” on page 77 for details.
ENA_XC	Enable crossover 1 = Enable Auto-Crossover 0 = Disable Auto-Crossover and select MDIX
CLASS_A/B	Transmitter Class A/B select 1 = Class B drivers (typically used in CAT 5 applications) 0 = Class A drivers - available for 100BASE-TX mode only (typically used in Backplane or direct connect applications)
ENA_EDET	Enable energy detect 1 = Enable 0 = Disable
PHYADR[4:3]	PHYADR[4:3] = 00 assigns PHY address 0 - 7 for the device. PHYADR[4:3] = 01 assigns PHY address 8 - 15 for the device. PHYADR[4:3] = 10 assigns PHY address 16 - 23 for the device. PHYADR[4:3] = 11 assigns PHY address 24 - 31 for the device. Refer to Table 37 for details.

Table 37: PHY address assignments

Device	PHY_ADR[4:3]	Port Number	Address In Decimal	Actual PHY_ADR[4:0] Assignments
0	00	0	0	00000
		1	1	00001
		2	2	00010
		3	3	00011
		4	4	00100
		5	5	00101
		6	6	00110
		7	7	00111
1	01	0	8	01000
		1	9	01001
		2	10	01010
		3	11	01011
		4	12	01100
		5	13	01101
		6	14	01110
		7	15	01111
2	10	0	16	10000
		1	17	10001
		2	18	10010
		3	19	10011
		4	20	10100
		5	21	10101
		6	22	10110
		7	23	10111
3	11	0	24	11000
		1	25	11001
		2	26	11010
		3	27	11011
		4	28	11100
		5	29	11101
		6	30	11110
		7	31	11111

2.6 Far End Fault Indication (FEFI)

Far-end fault indication provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred in 100BASE-FX mode.

A remote fault is an error in the link that one station can detect while the other one cannot. An example of this is a disconnected wire at a station's transmitter. This station is receiving valid data and detects that the link is good via the link monitor, but is not able to detect that its transmission is not propagating to the other station.

A 100BASE-FX station that detects this remote fault modifies its transmitted idle stream pattern from all ones to a group of 84 ones followed by one zero. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by the FEFI bits in 100BASE-FX mode.

Table 38: FEFI Select

Media	Pn_ANEG[2:0]	EN_FEFI (at reset)	FEFI	FEFI Bit (Table 68 on page 108)
100BASE-FX	11 X	1	Enabled	0 = Enable
	11 X	0	Disabled	1 = Disabled
10/100BASE-T	FEFI is not applicable in 10/100BASE-T modes			

2.7 Virtual Cable Tester® Feature

The 88E3082/88E3083 devices Virtual Cable Tester (VCT™) feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics.

The 88E3082/88E3083 devices transmit a signal of known amplitude (+1V) down each of the two pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the TX and RX pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection. The magnitude of the reflection and the time it takes for the reflection to come back are shown in the VCT registers (Table 79 on page 124 and Table 80 on page 125) on the AmpRfln and DistRfln bits respectively.

Using the information from the VCT registers (Table 79 on page 124 and Table 80 on page 125), the distance to the problem location and the type of problem can be determined. For example, the time it takes for the reflection to come back, can be converted to distance using the cable fault distance trend line tables on page 125. The polarity and magnitude of the reflection together with the distance will indicate the type of discontinuity. For example, a +1V reflection will indicate an open close to the PHY and a -1V reflection will indicate a short close to the PHY.

When the cable diagnostic feature is activated by setting the ENVCT bit to one (Table 79 on page 124), a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending 100BASE-TX idles or 10 Mbit data packets. This is necessary to be able to perform the TDR test. The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E3082/88E3083 devices receive a continuous signal for 125 ms, it will declare test failure because it cannot start the TDR test. In the test fail case, the received data is not valid. The results of the test are also summarized in the VCTTst bits (Table 79 on page 124 and Table 80 on page 125).

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = valid test, normal cable (no short or open in cable)
- 10 = valid test, open in cable (Impedance > 333 ohms)
- 01 = valid test, short in cable (Impedance < 33 ohms)

The definition for shorts and opens is arbitrary and the user can define it anyway they desire using the information in the VCT registers (Table 79 on page 124 and Table 80 on page 125). The impedance mismatch at the location of the discontinuity could also be calculated knowing the magnitude of the reflection. Refer to the App Note "Virtual Cable Tester -- How to use TDR results" for details.

2.8 Data Terminal Equipment (DTE) Detect

The 88E3082/88E3083 devices support the Data Terminal Equipment (DTE) detect function. The IEEE 802.3af - 2003 DTE power scheme requires no role of the PHY to detect a DTE link partner that requires power; however, the 88E3082/88E3083 PHYs offer the ability to detect a DTE link partner that requires power.

The DTE power function can be enabled after a hardware reset by writing to the Enable DTE Detect bit (Register 16.15), followed by a software reset. When DTE Detect is enabled, the 88E3082/88E3083 devices will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and can link with the 88E3082/88E3083 devices. If there is no activity coming from the link partner, DTE Detect engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The detection of the DTE power requirement can be reported to the 88E3082/88E3083 devices in two ways.

- The DTE Detect Status bit (Register 17.15) immediately asserts as soon as the link partner is detected as a device requiring DTE power. The 88E3082/88E3083 devices will continually send special link pulses to detect if the link partner requires DTE power.
- If the DTE Detect Status Change Interrupt bit (Register 18.15) is enabled, an interrupt can be generated if a DTE powered device is detected. The 88E3082/88E3083 devices will then update the DTE Detect Status Drop bit (Register 22.15) and the DTE Detect Status bit (Register 17.15).

If a link partner that requires DTE power is unplugged, the DTE Detect Status bit (Register 17.15) will drop after a user controlled delay (default is 20 seconds - DTE Detect Status Drop bit (Register 22.15:14) = 0x04), since the lowpass filter (or similar fixture) is removed during power up.

A detailed description of the register bits used for DTE power detection for the 88E3082/88E3083 devices are shown in Table 39.

Note

Auto-Negotiation must be enabled to use DTE detect. The DTE detect must be turned off when performing the Virtual Cable Tester® (VCT™) test.

Table 39: Registers for DTE Detect

Register	Description
16.15 - Enable DTE Detect	1 = Enable DTE detect 0 = Disable DTE detect Default at HW reset: 0 At SW reset: Retain
17.15 DTE Detect status	1 = DTE detected 0 = DTE not detected Default at HW reset: 0 At SW reset: 0
18.15 - DTE Detect state changed interrupt enable	1 = Interrupt enable 0 = Interrupt disable Default at HW reset: 0 At SW reset: retain
19.15 DTE Detect state changed interrupt	1 = Changed 0 = No change Default at HW reset: 0 At SW reset: 0
22.15:12 DTE detect status drop	Once the 88E3082/88E3083 no longer detects the link partner's DTE filter, the 88E3082/88E3083 will wait a period of time before clearing the DTE detection status bit (17.15). The wait time is 5 seconds multiplied by the value of these bits. Default at HW reset: 0x4 At SW reset: retain

2.9 Auto MDI/MDIX Crossover

The 88E3082/88E3083 devices automatically determine whether or not it needs to cross over between pairs so that an external crossover cable is not required. If the 88E3082/88E3083 devices interoperate with a device that cannot automatically correct for crossover, the 88E3082/88E3083 devices make the necessary adjustment prior to commencing Auto-Negotiation. If the 88E3082/88E3083 devices interoperate with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the 88E3082/88E3083 devices interoperate with legacy 10BASE-T devices that do not implement Auto-Negotiation, the 88E3082/88E3083 devices follow the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E3082/88E3083 devices use signal detect to determine whether or not to crossover.

The Auto MDI/MDIX crossover function can be disabled via the AutoMDI[X] bits (Table 68 on page 108).

The 88E3082/88E3083 devices are set to MDIX mode by default if auto MDI/MDIX crossover is disabled at hardware reset.

The pin mapping in MDI and MDIX modes is specified in Table 40. Refer to Table 53 on page 98 for magnetics details.

Table 40: MDI/MDIX Pin Functions

Physical Pin	MDIX		MDI	
	100BASE-TX	10BASE-T	100BASE-TX	10BASE-T
TXP/TXN	Transmit	Transmit	Receive	Receive
RXP/RXN	Receive	Receive	Transmit	Transmit

2.10 LED Interface

The LEDs can either be controlled by the PHY or controlled externally, independent of the state of the PHY.

External control is achieved by writing to the PHY Manual LED Override register (Table 78 on page 123). Any of the LEDs can be turned on, off, or made to blink at variable rates independent of the state of the PHY. This independence eliminates the need for driving LEDs from the MAC or the CPU. If the LEDs are driven from the CPU located at the back of the board, the LED lines crossing the entire board will pick up noise. This noise will cause EMI issues. Also, PCB layout will be more difficult due to the additional lines routed across the board.

When the LEDs are controlled by the PHY, the activity of the LEDs is determined by the state of the PHY. Each LED can be programmed to indicate various PHY states, with variable blink rate.

Any one of the LEDs can be controlled independently of the other LEDs (i.e one LED can be externally controlled while another LED can be controlled by the state of the PHY).

The LED interface supports a 3-pin parallel interface for each port or a serial interface for all ports.

The 88E3082 device can be programmed to display serial LED statuses in single or dual LED modes. See “Single and Dual LED Modes” on page 83. Some of the statuses can be pulse stretched. Pulse stretching is necessary because the duration of these status events might be too short to be observable on the LEDs. The pulse stretch duration can be programmed via the PulseStretch bits (Table 77 on page 122). The default pulse stretch duration is set to 170 to 340 ms. The pulse stretch duration applies to all applicable LEDs.

Some of the statuses indicate multiple events by blinking LEDs. The blink period can be programmed via the BlinkRate bits (Table 77 on page 122). The default blink period is set to 84 ms. The blink rate applies to all applicable LEDs.

2.10.1 Parallel LED Interface

The parallel LED interface displays 3 different statuses for each port. LED2, LED1, and LED0 pins are used for each port. The LED Parallel Select Register specifies which single LED mode status to display on the LED pins. The defaults to display shown in Table 41 are based on the LED_DEF[1] and LED_DEF[0] values during hardware configuration through the CONFIG8 pin.

Table 41: Parallel LED Hardware Defaults

LED_DEF[1] (Via CONFIG8)	LED_DEF[0] (Via CONFIG8)	P[7:0]_LED2	P[7:0]_LED1	P[7:0]_LED0
0	0	LINK	RX	TX
0	1	LINK	ACT	SPEED
1	0	LINK/RX	TX	SPEED
1	1	LINK/ACT	DUPLEX/COLX	SPEED

2.10.2 Serial LED Interface

LEDSER, LEDENA, and LEDCLK pins of the 88E3082 device are used for the serial interface. LED_DEF[1] and LED_DEF[0] via CONFIG 8 are used to select 1 of 4 possible modes. The serial LED interface can display up to 11 different statuses in 100BASE-TX and 10BASE-T modes. Statuses to display, pulse stretching, and blink mode can be programmed via the LED Stream Select for Serial LEDs register and the PHY LED Control register bits 5:0.

2.10.3 Single and Dual LED Modes

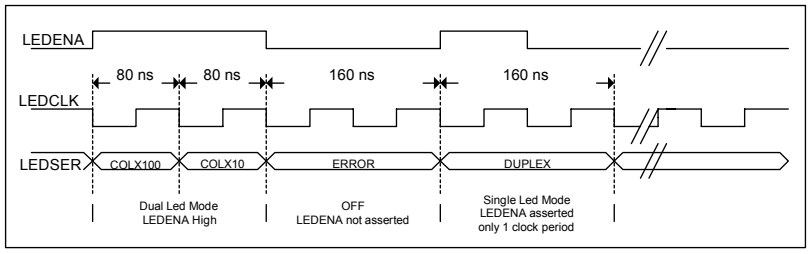
2.10.3.1 Single LED Display Mode

In the single LED display mode, the same status is driven on both status 100 and status 10 positions in the bit stream. However, the LEDENA signal asserts only over the status that is set and de-asserts over the other position that is turned off in the bit stream. For example, DUPLEX shows the same status for DUPLEX100 and DUPLEX10. However, LEDENA signal is high over Duplex100 position only for one clock period. Refer to Figure 25 for more details.

2.10.3.2 Dual LED Display Mode

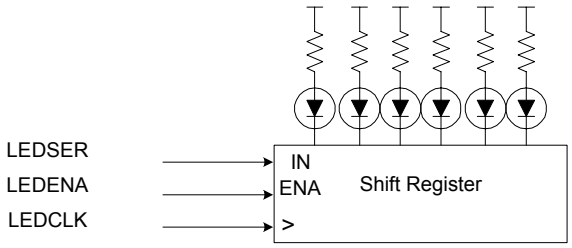
In the dual LED display mode, two LEDs are used: one for 10 Mbps, and one for 100 Mbps activity. A different status is driven on status 100 and status 10 positions in the bit stream. In this case, the LEDENA signal asserts over both 100 and 10 positions in the bit stream. For example, LEDENA signal asserts over COLX100 and COLX10 in Figure 25. LEDENA signal is high for two clock periods. If a particular status bit is turned off, then LEDENA is not asserted in both positions. Figure 25 illustrates single and dual LED modes.

Figure 25: Serial LEDENA High Clocking with COLX in Dual Mode, Error Off, and DUPLEX in Single Mode



The bit stream on LEDSER can be clocked into a shift register with LEDENA as the shift enable signal as shown in Figure 26. The rate of update of the serial LED interface is controlled by programming the PHY LED Control Register bits 8:6. The default value is set to 42 ms.

Figure 26: Serial LED Conversion



After the LED data is shifted into the correct position, the shift sequence is suspended to allow the appropriate LEDs to light or extinguish depending on status. The LED implementation used in the 88E3082/88E3083 devices are self-synchronizing. The default display options are given in Table 42.

Table 42: Serial LED Hardware Defaults (S = Single)

LED_DEF[1] (At Reset)	LED_DEF[0] (At Reset)	COLX	ERROR	DUPLEX	DUPLEX/ COLX	SPEED	LINK	TX	RX	ACT	LINK/RX	LINK/ACT
0	0	Off	S	Off	S	S	Off	Off	Off	Off	Off	S
0	1	S	S	S	Off	S	Off	S	Off	Off	S	Off
1	0	S	S	S	Off	S	S	Off	Off	S	Off	Off
1	1	S	S	S	Off	S	S	S	S	Off	Off	Off

The LED status bits are output in the order shown on the LEDSER pin synchronously to LEDCLK. All statuses for Port 0 are sent out first followed by those for Ports 1 through 7. Each bit in the stream occupies a period of 80ns.

Table 43: Serial LED Display Order

<COLX100> → <COLX10> → <ERROR100> → <ERROR10> → <DUPLEX100> → <DUPLEX10>→ <DUPLEX/COLX100> → <DUPLEX/COLX10> → <SPEED100> → <SPEED10> → <LINK100>→ <LINK10> → <TX100> → <TX10> → <RX100> → <RX10> → <ACT100> → <ACT10> → <LINK/RX100>→ <LINK/RX10> → <LINK/ACT100> → <LINK/ACT10>

The following tables show the status events that can be displayed by programming the 88E3082 device in single and dual LED display modes

Table 44: Single LED Display Mode

Status	Description
COLX	Low = collision activity High = no collision activity This status has a default pulse stretch duration of 170 ms.
ERROR	Low = Jabber, received error, false carrier, or FIFO over/underflow occurred High = none of the above occurred This status has a default pulse stretch duration of 170 ms.
DUPLEX	Low = full-duplex High = half-duplex
DUPLEX/COLX	Low = full-duplex High = half-duplex Blink = collision activity (default blink rate is 84 ms active then 84 ms inactive) The collision activity has a default pulse stretch duration of 84 ms.
SPEED	Low = speed is 100 Mbps High = speed is 10 Mbps
LINK	Low = link up High = link down
TX	Low = transmit activity High = no transmit activity This status has a default pulse stretch duration of 170 ms.
RX	Low = receive activity High = no receive activity This status has a default pulse stretch duration of 170 ms.
ACT	Low = transmit or received activity High = no transmit or receive activity This status has a default pulse stretch duration of 170 ms.
LINK/RX	Low = link up High = link down Blink = receive activity (blink rate is 84 ms active then 84 ms inactive) The receive activity has a pulse stretch duration of 84 ms.
LINK/ACT	Low = link up High = link down Blink = transmit or receive activity (blink rate is 84 ms active then 84 ms inactive) The transmit and receive activity has a pulse stretch duration of 84 ms.

Table 45: Dual LED Display Mode

Event	Status
COLX100	0 = 100 Mbps collision activity 1 = No 100 Mbps collision activity This status has a default pulse stretch duration of 170 ms.
COLX10	0 = 10 Mbps collision activity 1 = No 10 Mbps collision activity This status has a default pulse stretch duration of 170 ms.
ERROR100	0 = Received error, false carrier, or 100 Mbps FIFO over/underflow occurred. 1 = None of the above occurred This status has a default pulse stretch duration of 170 ms.
ERROR10	0 = Jabber or 10 Mbps FIFO over/underflow occurred 1 = None of the above occurred This status has a default pulse stretch duration of 170 ms.
DUPLEX100	0 = 100 Mbps full-duplex 1 = 100 Mbps half-duplex
DUPLEX10	0 = 10 Mbps full-duplex 1 = 10 Mbps half-duplex
DUPLEX/COLX100	0 = 100 Mbps full-duplex 1 = 100 Mbps half-duplex Blink = 100 Mbps collision activity The 100 Mbps collision activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.
DUPLEX/COLX10	0 = 10 Mbps full-duplex 1 = 10 Mbps half-duplex Blink = 10 Mbps collision activity The 10 Mbps collision activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.
SPEED100	0 = Speed is 100 Mbps 1 = Speed is 10 Mbps
SPEED10	0 = Speed is 10 Mbps 1 = Speed is 100 Mbps
LINK100	0 = 100 Mbps link up 1 = 100 Mbps link down
LINK10	0 = 10 Mbps link up 1 = 10 Mbps link down
TX100	0 = 100 Mbps transmit activity 1 = No 100 Mbps transmit activity This status has a default pulse stretch duration of 170 ms.
TX10	0 = 10 Mbps transmit activity 1 = No 10 Mbps transmit activity This status has a default pulse stretch duration of 170 ms.

Table 45: Dual LED Display Mode

Event	Status
RX100	0 = 100 Mbps receive activity 1 = No 100 Mbps receive activity This status has a default pulse stretch duration of 170 ms.
RX10	0 = 10 Mbps receive activity 1 = No 10 Mbps receive activity This status has a default pulse stretch duration of 170 ms.
ACT100	0 = 100 Mbps transmit or 100 Mbps receive activity 1 = No 100 Mbps transmit or 100 Mbps receive activity This status has a default pulse stretch duration of 170 ms.
ACT10	0 = 10 Mbps transmit or 10 Mbps receive activity 1 = No 10 Mbps transmit or 10 Mbps receive activity This status has a default pulse stretch duration of 170 ms.
LINK/RX100	0 = 100 Mbps link up 1 = 100 Mbps link down Blink = 100 Mbps receive activity The 100 Mbps receive activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.
LINK/RX10	0 = 10 Mbps link up 1 = 10 Mbps link down Blink = 10 Mbps receive activity The 10 Mbps receive activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.
LINK/ACT100	0 = 100 Mbps link up 1 = 100 Mbps link down Blink = 100 Mbps transmit or 100 Mbps receive activity The 100 Mbps receive or transmit activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.
LINK/ACT10	0 = 10 Mbps link up 1 = 10 Mbps link down Blink = 10 Mbps transmit or 10 Mbps receive activity This 10 Mbps receive or transmit activity has a default pulse stretch duration of 84 ms. The blink rate can be programmed.

2.11 IEEE 1149.1 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits.

The standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The 88E3082/88E3083 devices implement 5 basic instructions: bypass, sample/preload, extest, and clamp. Upon reset, the bypass instruction is selected instead of the ID_Code instruction (not supported). The instruction opcodes are shown in the table below.

Table 46: TAP Controller OpCodes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
BYPASS	11111111

The 88E3082/88E3083 devices reserve 5 pins, the Test Access Port (TAP), to provide test access:

- Test Mode Select Input (TMS)
- Test Clock Input (TCK)
- Test Data Input (TDI)
- Test Data Output (TDO)
- and Test Reset Input (TRSTn)

To ensure race-free operation, all input and output data is synchronous to the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details, refer to IEEE 1149.1 Boundary Scan Architecture.

2.11.1 Bypass Instruction

The bypass instruction uses the bypass register. The bypass register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the 88E3082/88E3083 when test operation is not required. This allows more rapid movement of test data to and from other testable devices in the system.

2.11.2 Sample/Preload Instruction

The sample/preload instruction allows scanning of the boundary-scan register without causing interference to the normal operation of the 88E3082/88E3083. Two functions are performed when this instruction is selected: sample and preload.

2.11.2.1 Sample

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the *capture-DR* controller state, and the data can be viewed by shifting through the component's TDO output.

2.11.2.2 Preload

While sampling and shifting data out through TDO for observation, preload allows an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence has been completed. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

2.11.3 Extest Instruction

The extest instruction allows circuitry external to the 88E3082/88E3083 (typically the board interconnections) to be tested. Prior to executing the extest instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the 88E3082/88E3083 to its external connections.

2.11.4 The Clamp Instruction

The clamp instruction allows the state of the signals driven from the component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins will not change while the clamp instruction is selected.

2.11.5 The HIGH-Z Instruction

The HIGH-Z instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

2.11.6 Boundary Scan Chain Order

Input indicates input into chip. Output indicates output from chip. Enable indicates output enable and is active high. Note that the INTn pin is defined as an enable pin rather than an output pin.

Table 47: 88E3082 Boundary Scan Chain Order

Pin Name	I/O
RESETn	Input
MDC	Input
MDIO	Input
MDIO	Output
MDIO_EN	Enable (See note 1)
INTn	Enable (See note 2)
SEL_RMII	Input
GEN_OEN	Enable
LEDENA	Output
LEDCLK	Input
LEDSER	Input
LEDSER_EN	Enable (See note 4)
REFCLK	Input
CONFIG8	Input
CONFIG9	Input
CONFIG10	Input
NORMAL	NC
P0_TXD1	Input
P0_TXD0	Input
P0_TX_EN	Input
P0_RX_ER	Output
P0_CRS_DV	Output
P0_RXD0	Output
P0_RXD1	Output
P0_LED0	Output
P0_LED1	Output
P0_LED2	Output
CONFIG0	Input
P1_TXD1	Input
P1_TXD0	Input
P1_TX_EN	Input
P1_RX_ER	Output
P1_CRS_DV	Output
P1_RXD0	Output
P1_RXD1	Output
P1_LED0	Output
P1_LED1	Output
P1_LED2	Output
CONFIG1	Input
P2_TXD1	Input
P2_TXD0	Input
P2_TX_EN	Input
P2_RX_ER	Output
P2_CRS_DV	Output
P2_RXD0	Output
P2_RXD1	Output
P2_LED0	Output
P2_LED1	Output
P2_LED2	Output
CONFIG2	Input
P3_TXD1	Input
P3_TXD0	Input
P3_TX_EN	Input
P3_RX_ER	Output
P3_CRS_DV	Output
P3_RXD0	Output
P3_RXD1	Output
P3_LED0	Output
P3_LED1	Output
P3_LED2	Output
CONFIG3	Input
P4_TXD1	Input
P4_TXD0	Input
P4_TX_EN	Input
P4_RX_ER	Output
P4_CRS_DV	Output
P4_RXD0	Output
P4_RXD1	Output
P4_LED0	Output
P4_LED1	Output
P4_LED2	Output
CONFIG4	Input
P5_TXD1	Input

Pin Name	I/O
P5_TXD0	Input
P5_TX_EN	Input
P5_RX_ER	Output
P5_CRS_DV	Output
P5_RXD0	Output
P5_RXD1	Output
P5_LED0	Output
P5_LED1	Output
P5_LED2	Output
CONFIG5	Input
P6_TXD1	Input
P6_TXD0	Input
P6_TX_EN	Input
P6_RX_ER	Output
P6_CRS_DV	Output
P6_RXD0	Output
P6_RXD1	Output
P6_LED0	Output
P6_LED1	Output
P6_LED2	Output
CONFIG6	Input
P7_TXD1	Input
P7_TXD0	Input
P7_TX_EN	Input
P7_RX_ER	Output
P7_CRS_DV	Output
P7_RXD0	Output
P7_RXD1	Output
P7_LED0	Output
P7_LED1	Output
P7_LED2	Output

Pin Name	I/O
CONFIG7	Input
Note 1: Output enable for MDIO. 1 = Output, 0 = Input	
Note 2: Open drain enable for INTn. 1 = Drive low, 0 = Open drain	
Note 3: Output enable for all digital output only pins. 1 = Output, 0 = Tri-state	
Note 4: Output enable for LEDENA, LEDCLK, LED-SER. 1 = Output, 0 = Tri-state	

Table 48: 88E3083 Boundary Scan Chain Order

Pin Name	I/O
RESETn	Input
MDC	Input
MDIO	Input
MDIO	Output
MDIO_EN	Enable (See Note 1)
INTn	Enable (See Note 2)
SEL_RMII RSVD1	Input
GEN_OEN	Enable
REFCLK	Input
CONFIG[8]	Input
CONFIG[9]	Input
CONFIG[10]	Input
NORMAL	Input
P0_LED0	Output
P0_LED1	Output
P0_LED2	Output
CONFIG0	Input
CONFIG[1]	Input
SMII_MODE[0]	Input
SMII_MODE[1]	Input
P1_LED0	Output
P1_LED1	Output
P1_LED2	Output
CONFIG[2]	Input
P2_LED0	Output
P2_LED1	Output
P2_LED2	Output
TX_SYNC	Input
P0_TXD	Input
P1_TXD	Input
RX_CLK	Output
RX_SYNC	Output
P0_RXD	Output
P1_RXD	Output
P3_LED0	Output
P3_LED1	Output
P3_LED2	Output
CONFIG[3]	Input
P2_TXD	Input
P3_TXD	Input
P4_TXD	Input
P2_RXD	Output
P3_RXD	Output
P4_RXD	Output
P5_RXD	Output
P4_LED0	Output
P4_LED1	Output
P4_LED2	Output
CONFIG[4]	Input
P5_TXD	Input
P6_TXD	Input
P7_TXD	Input
P6_RXD	Output
P7_RXD	Output
P5_LED0	Output
P5_LED1	Output
P5_LED2	Output
CONFIG[5]	Input
CONFIG[6]	Input
P6_LED0	Output
P6_LED1	Output
P6_LED2	Output
CONFIG[7]	Input
P7_LED0	Output
P7_LED1	Output
P7_LED2	Output
Note 1: Output enable for MDIO. 1 = Output, 0 = Input	
Note 2: Open drain enable for INTn. 1 = Drive low, 0 = Open drain	
Note 3: Output enable for all digital output only pins. 1 = Output, 0 = Tri-state	

Section 3. Register Description

Table 49 defines the register types used in the register map.

Table 49: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to the register field does take effect without a software reset, and the register maintains its value after a software reset.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROC	Read only clear. After read, register field is cleared to zero.
R/W	Read and write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until soft reset is executed; however, the written value can be read even before the software reset.
WO	Write only. Reads to this type of register field return undefined data.

Table 50: PHY Register Map

Description	Offset Hex	Offset Decimal	Page Number
PHY Control Register	0x00	0	page 95
PHY Status Register	0x01	1	page 97
PHY Identifier	0x02	2	page 98
PHY Identifier	0x03	3	page 99
Auto-Negotiation Advertisement Register	0x04	4	page 100
Link Partner Ability Register (Base Page)	0x05	5	page 102
Link Partner Ability Register (Next Page)	0x05	5	page 103
Auto-Negotiation Expansion Register	0x06	6	page 104
Next Page Transmit Register	0x07	7	page 105
Link Partner Next Page Register	0x08	8	page 106
Reserved Registers	0x09-0x0F	9 - 15	page 106
PHY Specific Control Register I	0x10	16	page 108
PHY Specific Status Register	0x11	17	page 110
PHY Interrupt Enable	0x12	18	page 112
PHY Interrupt Status	0x13	19	page 114
PHY Interrupt Port Summary	0x14	20	page 116
PHY Receive Error Counter	0x15	21	page 117
LED Parallel Select Register	0x16	22	page 118
LED Stream Select Register - 88E3082 Only	0x17	23	page 120
Reserved - 88E3083 Only	0X17	23	page 121
PHY LED Control Register	0x18	24	page 122
PHY Manual LED Override Register	0x19	25	page 123
VCT™ Control Register	0x1A	26	page 124
VCT Status Register	0x1B	27	page 125
PHY Specific Control Register II	0x1C	28	page 126
Reserved Registers	0x1D to 0x1F	29 - 31	page 126

Table 51: PHY Control Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SWReset	R/W, SC	0x0	0	PHY Software Reset Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 0 = Normal operation 1 = PHY reset
14	Loopback	R/W	0x0	Retain	Enable Loopback Mode When loopback mode is activated, the transmitter data presented on TXD is looped back to RXD internally. The PHY has to be in forced 10 or 100 Mbps mode. Auto-Negotiation must be disabled. 0 = Disable loopback 1 = Enable loopback
13	SpeedLSB	R/W	ANEG [2:0]	Update	Speed Selection (LSB) When a speed change occurs, the PHY drops link and tries to determine speed when Auto-Negotiation is on. Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to this register bit has no effect unless any one of the following also occurs: Software reset is asserted (bit 15) or Power down (bit 11) transitions from power down to normal operation. 0 = 10 Mbps 1 = 100 Mbps
12	AnegEn	R/W	ANEG [2:0]	Update	Auto-Negotiation Enable Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to this register bit has no effect unless any one of the following also occurs: Software reset is asserted (bit 15, above), Power down (bit 11, below), or the PHY transitions from power down to normal operation. If the AnegEn bit is set to 0, the speed and duplex bits of the PHY Control Register (Offset 0x00) take effect. If the AnegEn bit is set to 1, speed and duplex advertisement is found in the Auto-Negotiation Advertisement Register (Offset 0x04). 0 = Disable Auto-Negotiation Process 1 = Enable Auto-Negotiation Process

Table 51: PHY Control Register (Continued)
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
11	PwrDwn	R/W	0x0	Retain	Power Down Mode When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (bit 15, above) and Restart Auto-Negotiation (bit 9, below) are not set by the user. 0 = Normal operation 1 = Power down
10	Isolate	RO	Always 0	Always 0	Isolate Mode Will always be 0. The Isolate function is not available, since full MII is not implemented. 0 = Normal operation
9	RestartAneg	R/W, SC	0x0	Self Clear	Restart Auto-Negotiation Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit is set. 0 = Normal operation 1 = Restart Auto-Negotiation Process
8	Duplex	R/W	ANEG [2:0]	Update	Duplex Mode Selection Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15), Power down (bit 11), or transitions from power down to normal operation. 0 = Half-duplex 1 = Full-duplex
7	ColTest	RO	Always 0	Always 0	Collision Test Mode Will always be 0. The Collision test is not available, since full MII is not implemented. 0 = Disable COL signal test
6	SpeedMSB	RO	Always 0	Always 0	Speed Selection Mode (MSB) Will always be 0. 0 = 100 Mbps or 10 Mbps
5:0	Reserved	RO	Always 0	Always 0	Will always be 0.

Table 52: PHY Status Register
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100T4	RO	Always 0	Always 0	100BASE-T4 This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100FDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X full-duplex 1 = PHY able to perform full-duplex
13	100HDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X half-duplex 1 = PHY able to perform half-duplex
12	10FDX	RO	Always 1	Always 1	10BASE-T full-duplex 1 = PHY able to perform full-duplex
11	10HPX	RO	Always 1	Always 1	10BASE-T half-duplex 1 = PHY able to perform half-duplex
10	100T2FDX	RO	Always 0	Always 0	100BASE-T2 full-duplex. This protocol is not available. 0 = PHY not able to perform full-duplex
9	100T2HDX	RO	Always 0	Always 0	100BASE-T2 half-duplex This protocol is not available. 0 = PHY not able to perform half-duplex
8	ExtdStatus	RO	Always 0	Always 0	Extended Status 0 = No extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MFPreSup	RO	Always 1	Always 1	MF Preamble Suppression Mode Must be always 1. 1 = PHY accepts management frames with preamble suppressed
5	AnegDone	RO	0x0	0	Auto-Negotiation Complete 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed
4	RemoteFault	RO, LH	0x0	0	Remote Fault Mode 0 = Remote fault condition not detected 1 = Remote fault condition detected
3	AnegAble	RO	Always 1	Always 1	Auto-Negotiation Ability Mode 1 = PHY able to perform Auto-Negotiation

Table 52: PHY Status Register (Continued)
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Link	RO, LL	0x0	0	Link Status Mode This register indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read RTLink in Table 69 on page 110. 0 = Link is down 1 = Link is up
1	JabberDet	RO, LH	0x0	0	Jabber Detect 0 = Jabber condition not detected 1 = Jabber condition detected
0	ExtdReg	RO	Always 1	Always 1	Extended capability mode. 1 = Extended register capabilities

Table 53: PHY Identifier
Offset: 0x02 (Hex), or 2 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organization-ally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit 18

Table 54: PHY Identifier
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit 24
9:4	ModelNum	RO	Always 001000	Always 001000	Model Number = 001000
3:0	RevNum	RO	Varies	Varies	Revision Number Contact Marvell® FAEs for information on the device revision number.

Table 55: Auto-Negotiation Advertisement Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	AnegAd NxtPage	R/W	0x0	Retain	Next Page 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
14	Ack	RO	Always 0	Always 0	Must be 0.
13	AnegAd ReFault	R/W	0x0	Retain	Remote Fault Mode 0 = Do not set Remote Fault bit 1 = Set Remote Fault bit Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
12:11	Reserved	R/W	0x0	Retain	Must be 00. Reserved bits are R/W to allow for forward compatibility with future IEEE standards. Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
10	AnegAd Pause	R/W	0x0	Retain	Pause Mode 0 = MAC PAUSE not implemented 1 = MAC PAUSE implemented Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
9	AnegAd 100T4	R/W	0x0	Retain	100BASE-T4 mode 0 = Not capable of 100BASE-T4 Must be 0.
8	AnegAd 100FDX	R/W	0x1	Retain	100BASE-TX full-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.

Table 55: Auto-Negotiation Advertisement Register (Continued)
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
7	AnegAd 100HDX	R/W	0X1	Retain	100BASE-TX half-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
6	AnegAd 10FDX	R/W	0X1	Retain	10BASE-TX full-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
5	AnegAd 10HDX	R/W	0X1	Retain	10BASE-TX half-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 51 on page 95) or link goes down.
4:0	AnegAd Selector	R/W	Always 0x01	Always 0x01	Selector Field Mode 00001 = 802.3

Table 56: Link Partner Ability Register (Base Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxt Page	RO	0x0	0	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 68 on page 108) is disabled. When Reg8NxtPg (Table 68 on page 108) is enabled, then next page is stored in the Link Partner Next Page register (Table 60 on page 106), and the Link Partner Ability Register (Table 56 on page 102) holds the base page. Received Code Word Bit 15 0 = Link partner not capable of next page 1 = Link partner capable of next page
14	LPAck	RO	0x0	0	Acknowledge Received Code Word Bit 14 0 = Link partner did not receive code word 1 = Link partner received link code word
13	LPRemote Fault	RO	0x0	0	Remote Fault Received Code Word Bit 13 0 = Link partner has not detected remote fault 1 = Link partner detected remote fault
12:5	LPTechAble	RO	0x00	0x00	Technology Ability Field Received Code Word Bit 12:5
4:0	LPSelector	RO	00000	00000	Selector Field Received Code Word Bit 4:0

Table 57: Link Partner Ability Register (Next Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxtPage	RO	--	--	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 68 on page 108) is disabled. When Reg8NxtPg (Table 68 on page 108) is enabled, then next page is stored in the Link Partner Next Page register (Table 60 on page 106), and Link Partner Ability Register (Table 56 on page 102) holds the base page. Received Code Word Bit 15
14	LPAck	RO	--	--	Acknowledge Received Code Word Bit 14
13	LPMessage	RO	--	--	Message Page Received Code Word Bit 13
12	LPack2	RO	--	--	Acknowledge 2 Received Code Word Bit 12
11	LPToggle	RO	--	--	Toggle Received Code Word Bit 11
10:0	LPData	RO	--	--	Message/Unformatted Field Received Code Word Bit 10:0

Table 58: Auto-Negotiation Expansion Register
Offset: 0x06 (Hex), or 6 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	Always 0x000	Always 0x000	Reserved. Must be 00000000000. The Auto-Negotiation Expansion Register is not valid until the AnegDone (Table 52 on page 97) indicates completed.
4	ParFaultDet	RO/LH	0x0	0x0	Parallel Detection Level 0 = A fault has not been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function
3	LPNxtPg Able	RO	0x0	0x0	Link Partner Next Page Able 0 = Link Partner is not Next Page able 1 = Link Partner is Next Page able
2	LocalNxtPg Able	RO	Always 0x1	Always 0x1	Local Next Page Able This bit is equivalent to AnegAble (Table 52 on page 97). 1 = Local Device is Next Page able
1	RxNewPage	RO/LH	0x0	0x0	Page Received 0 = A New Page has not been received 1 = A New Page has been received
0	LPAnegAble	RO	0x0	0x0	Link Partner Auto-Negotiation Able 0 = Link Partner is not Auto-Negotiation able 1 = Link Partner is Auto-Negotiation able

Table 59: Next Page Transmit Register
Offset: 0x07 (Hex), or 7 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TxNxtPage	R/W	0x0	0x0	A write to the Next Page Transmit Register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Reserved Transmit Code Word Bit 14
13	TxMessage	R/W	0x1	0x1	Message Page Mode Transmit Code Word Bit 13
12	TxAck2	R/W	0x0	0x0	Acknowledge2 Transmit Code Word Bit 12
11	TxToggle	RO	0x0	0x0	Toggle Transmit Code Word Bit 11
10:0	TxData	R/W	0x001	0x001	Message/Unformatted Field Transmit Code Word Bit 10:0

Table 60: Link Partner Next Page Register
Offset: 0x08 (Hex), or 8 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RxNxtPage	RO	0x0	0x0	If Reg8NxtPg (Table 68 on page 108) is enabled, then next page is stored in the Link Partner Next Page register (Table 60 on page 106); otherwise, theLink Partner Next Page register (Table 60 on page 106) is cleared to all 0's. Received Code Word Bit 15
14	RxAck	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 0 = Link partner not capable of next page 1 = Link partner capable of next page
13	RxMessage	RO	0x0	0x0	Message Page Received Code Word Bit 13
12	RxAck2	RO	0x0	0x0	Acknowledge 2 Received Code Word Bit 12
11	RxToggle	RO	0x0	0x0	Toggle Received Code Word Bit 11
10:0	RxData	RO	0x000	0x000	Message/Unformatted Field Received Code Word Bit 10:0

Table 61: Reserved Registers
Offset: 0x09 (Hex), or 9 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 62: Reserved Registers
Offset: 0x0A (Hex), or 10 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 63: Reserved Registers
Offset: 0x0B (Hex), or 11 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 64: Reserved Registers
Offset: 0x0C (Hex), or 12 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 65: Reserved Registers
Offset: 0x0D (Hex), or 13 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 66: Reserved Registers
Offset: 0x0E (Hex), or 14 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 67: Reserved Registers
Offset: 0x0F (Hex), or 15 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 68: PHY Specific Control Register
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable DTE Detect	R/W	0x0	Retain	Enable DTE Detect 0 = Disable DTE Detect 1 = Enable DTE Detect
14	EDet	R/W	ENA_ EDET	Retain	Energy Detect 0 = Disable 1 = Enable with sense and pulse Enable with sense only is not supported Enable Energy Detect takes on the appropriate value defined by the CONFIG9 pin at hardware reset.
13	DisNLP Check	R/W	0x0	0x0	Disable Normal Linkpulse Check Linkpulse check and generation disable have no effect, if Auto-Negotiation is enabled locally. 0 = Enable linkpulse check 1 = Disable linkpulse check
12	Reg8NxtPg	R/W	0x0	0x0	Enable the Link Partner Next Page register (Table 57 on page 103) to store Next Page. If set to store next page in the Link Partner Next Page register (Table 57 on page 103), then 802.3u is violated to emulate 802.3ab. 0 = Store next page in the Link Partner Ability Register (Base Page) register (Table 56 on page 102). 1 = Store next page in the Link Partner Next Page register (Table 57 on page 103)
11	DisNLPGen	R/W	0x0	0x0	Disable Linkpulse Generation. Linkpulse check and generation disable have no effect, when Auto-Negotiation is enabled locally. 0 = Enable linkpulse generation 1 = Disable linkpulse generation
10	ForceLink	R/W	0x0	0x0	Force Link Good When link is forced to be good, the link state machine is bypassed and the link is always up. 0 = Normal operation 1 = Force link good
9	DisScrambler	R/W	ANEG [2:0]	Retain	Disable Scrambler If either 100BASE-FX or 10BASE-T forced mode is selected, then the scrambler is disabled at hardware reset. However, when 10BASE-T is selected, this register bit equals 0. 0 = Enable scrambler 1 = Disable scrambler

Table 68: PHY Specific Control Register (Continued)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
8	DisFEFI	R/W	EN_ FEFI ANEG [2:0]	Retain	Disable FEFI In 100BASE-FX mode, Disable FEFI takes on the appropriate value defined by the CONFIG8 pin at hardware reset. FEFI is automatically disabled regardless of the state of this bit if copper mode is selected. 0 = Enable FEFI 1 = Disable FEFI For the 88E3083 device, this bit applies to Port 7 only.
7	ExtdDistance	R/W	0x0	0x0	Enable Extended Distance When using cable exceeding 100 meters, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 0 = Normal 10BASE-T receive threshold 1 = Lower 10BASE-T receive threshold
6	TPSelect	R/W	ANEG [2:0]	Update	(Un)Shielded Twisted Pair This setting can be changed by writing to this bit followed by software reset. 0 = Unshielded Twisted Pair - default 1 = Shielded Twisted Pair
5:4	AutoMDI[X]	R/W	ENA_ XC,1	Update	MDI/MDIX Crossover This setting can be changed by writing to these bits followed by software reset. If ENA_XC is 1 at hardware reset and Fiber mode is not selected, then bits 5:4 = 11 00 = Transmit on pins RXP/RXN, Receive on pins TXP/TXN 01 = Transmit on pins TXP/TXN, Receive on pins RXP/RXN 1x = Enable Automatic Crossover
3:2	RxFIFO Depth	R/W	0x0	0x0	Receive FIFO Depth 00 = 4 Bytes 01 = 6 Bytes 10 = 8 Bytes 11 = Reserved
1	AutoPol	R/W	0x0	00	Polarity Reversal If Automatic polarity is disabled, then the polarity is forced to be normal in 10BASE-T mode. Polarity reversal has no effect in 100BASE-TX mode. 0 = Enable automatic polarity reversal 1 = Disable automatic polarity reversal
0	DisJabber	R/W	0x0	00	Disable Jabber Jabber has no effect in full-duplex or in 100BASE-X mode. 0 = Enable jabber function 1 = Disable jabber function

Table 69: PHY Specific Status Register
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DTE Detect Status	RO	0x0	0x0	DTE Detect Status 0 = Disable DTE detect 1 = DTE detected
14	ResSpeed	RO	ANEG [2:0]	Retain	Resolved Speed Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 0 = 10 Mbps 1 = 100 Mbps
13	ResDuplex	RO	ANEG [2:0]	Retain	Resolved Duplex Mode Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 0 = Half-duplex 1 = Full-duplex
12	RcvPage	RO, LH	0x0	0x0	Page Receive Mode 0 = Page not received 1 = Page received
11	Resolved	RO	0x0	0x0	Speed and Duplex Resolved. Speed and duplex bits (14 and 13) are valid only after the Resolved bit is set. The Resolved bit is set when Auto-Negotiation has resolved the highest common capabilities or Auto-Negotiation is disabled. 0 = Not resolved 1 = Resolved
10	RTLink	RO	0x0	0x0	Link (real time) 0 = Link down 1 = Link up
9:7	Reserved	RES	Always 000	Always 000	Always 000.
6	MDI/MDIX	RO	0x0	0x0	MDI/MDIX Crossover Status 0 = Transmit on pins RXP/RXN, Receive on pins TXP/TXN 1 = Transmit on pins TXP/TXN, Receive on pins RXP/RXN
5	Reserved	RES	Always 0	Always 0	Always 0.

Table 69: PHY Specific Status Register (Continued)
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Sleep	RO	0x0	0x0	Energy Detect Status 0 = Chip is not in sleep mode (Active) 1 = Chip is in sleep mode (No wire activity)
3:2	Reserved	RES	Always 00	Always 00	Always 00.
1	RTPolarity	RO	0x0	0x0	Polarity (real time) 0 = Normal 1 = Reversed
0	RTJabber	RO	0x0	Retain	Jabber (real time) 0 = No Jabber 1 = Jabber

Table 70: PHY Interrupt Enable
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DTE Detect State Changed Interrupt Enable	R/W	0x0	Retain	DTE Detect State Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
14	SpeedIntEn	R/W	0x0	Retain	Speed Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
13	DuplexIntEn	R/W	0x0	Retain	Duplex Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
12	RxPageIntEn	R/W	0x0	Retain	Page Received Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
11	AnegDone IntEn	R/W	0x0	Retain	Auto-Negotiation Completed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
10	LinkIntEn	R/W	0x0	Retain	Link Status Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
9	SymErrIntEn	R/W	0x0	Retain	Symbol Error Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
8	FlsCrsIntEn	R/W	0x0	Retain	False Carrier Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
7	FIFOErrInt	R/W	0x0	Retain	FIFO Over/Underflow Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
6	MDI[x]IntEn	R/W	0x0	0x0	MDI/MDIX Crossover Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
5	Reserved	RES	0x0	Retain	Must be 0.
4	EDetIntEn	R/W	0x0	Retain	Energy Detect Interrupt Enable 0 = Disable 1 = Enable
3:2	Reserved	RES	0x0	Retain	Must be 00.

Table 70: PHY Interrupt Enable (Continued)
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1	PolarityIntEn	R/W	0x0	Retain	Polarity Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
0	JabberIntEn	R/W	0x0	Retain	Jabber Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable

Table 71: PHY Interrupt Status
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DTE Detect State Changed Interrupt	RO, LH	0x0	0x0	DTE detect state changed interrupt. 0 = DTE detect state not changed 1 = DTE detect state changed
14	SpeedInt	RO, LH	0x0	0x0	Speed Changed 0 = Speed not changed 1 = Speed changed
13	DuplexInt	RO, LH	0x0	0x0	Duplex Changed 0 = Duplex not changed 1 = Duplex changed
12	RxPageInt	RO, LH	0x0	0x0	0 = Page not received 1 = Page received
11	AnegDoneInt	RO, LH	0x0	0x0	Auto-Negotiation Completed 0 = Auto-Negotiation not completed 1 = Auto-Negotiation completed
10	LinkInt	RO, LH	0x0	0x0	Link Status Changed 0 = Link status not changed 1 = Link status changed
9	SymErrInt	RO, LH	0x0	0x0	Symbol Error 0 = No symbol error 1 = Symbol error
8	FlsCrsInt	RO, LH	0x0	0x0	False Carrier 0 = No false carrier 1 = False carrier
7	FIFOErrInt	RO, LH	0x0	0x0	FIFO Over /Underflow Error 0 = No over/underflow error 1 = Over/underflow error
6	MDIMDIXInt	RO, LH	0x0	0x0	MDI/MDIX Crossover Changed 0 = MDI/MDIX crossover not changed 1 = MDI/MDIX crossover changed
5	Reserved	RO	Always 0	Always 0	Always 0
4	EDetChg	RO, LH	0x0	0x0	Energy Detect Changed 0 = No Change 1 = Changed
3:2	Reserved	RO	Always 00	Always 00	Always 00

Table 71: PHY Interrupt Status (Continued)
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1	PolarityInt	RO	0x0	0x0	Polarity Changed 0 = Polarity not changed 1 = Polarity changed
0	JabberInt	RO, LH	0x0	0x0	Jabber Mode 0 = No Jabber 1 = Jabber

Table 72: PHY Interrupt Port Summary (Global[1])
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x0	0x0	Must be 00000000.
7	Port7Int Active	RO	0x0	0x0	Port 7 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
6	Port6Int Active	RO	0x0	0x0	Port 6 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
5	Port5Int Active	RO	0x0	0x0	Port 5 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
4	Port4Int Active	RO	0x0	0x0	Port 4 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
3	Port3Int Active	RO	0x0	0x0	Port 3 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
2	Port2Int Active	RO	0x0	0x0	Port 2 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt

Table 72: PHY Interrupt Port Summary (Global[1]) (Continued)
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Port1Int Active	RO	0x0	0x0	Port 1 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt
0	Port0Int Active	RO	0x0	0x0	Port 0 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 0 = Port does not have active interrupt 1 = Port has active interrupt

1. A Global register is accessible for writing from any port.

Table 73: Receive Error Counter
Offset: 0x15 (Hex), or 21 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RxErrCnt	RO	0x0000	0x0000	Receive Error Count This register counts receive errors on the media interface. When the maximum receive error count reaches 0xFFFF, the counter will roll over.

Table 74: LED Parallel Select Register (bits 11:0 are Global[1] bits)
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	DTE Detect Status Drop	R/W	0x4	Retain	DTE detect status drop. Once the 88E3082/88E3083 no longer detects the link partner's DTE filter, the 88E3082/88E3083 will wait a period of time before clearing the DTE detection status bit (17.15). The wait time is 5 seconds multiplied by the value of these bits. Example: 5*0x4 = 20 seconds
11:8	LED2	R/W	LED[1:0] 00 = LINK 01 = LINK 10 = LINK/RX 11= LINK/ ACT	Retain	LED2 Control. This is a global[1] setting. The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1010 = LINK/ACT, 1011 = ACT (BLINK mode) 1100 to 1111 = Force to 1
7:4	LED1	R/W	LED[1:0] 00 = RX 01 = ACT 10 = TX 11= DUPLEX /COLX	Retain	LED1 Control. This is a global[1] setting. The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1010 = LINK/ACT, 1011 = ACT (BLINK mode) 1100 to 1111 = Force to 1

Table 74: LED Parallel Select Register (Continued) (bits 11:0 are Global[1] bits)
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	LED0	R/W	LED[1:0] 00 = TX 01 = SPEED 10 = SPEED 11= SPEED	Retain	LED0 Control. This is a global[1] setting. The parallel LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1010 = LINK/ACT, 1011 = ACT (BLINK mode) 1100 to 1111 = Force to 1

1. Global register bits are used to control features and functions that are common to all ports in the device.

Table 75: LED Stream Select for Serial LEDs (Global Register) - 88E3082 Only
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Function	Mode	HW Rst	SW Rst	Description
15:14	LEDLnkActy	R/W	LED[1:0] 00 = Single 01 = Off 10 = Off 11 = Off	Retain	LED Link Activity The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
13:12	LEDRcvLnk	R/W	LED[1:0] 00 = Off 01 = Single 10 = Off 11 = Off	Retain	LED Receive Link The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
11:10	LEDActy	R/W	LED[1:0] 00 = Off 01 = Off 10 = Single 11 = Off	Retain	LED Activity The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
9:8	LEDRcv	R/W	LED[1:0] 00 = Off 01 = Off 10 = Off 11 = Single	Retain	LED Receive The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
7:6	LEDTx	R/W	LED[1:0] 00 = Off 01 = Single 10 = Off 11 = Single	Retain	Transmit The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
5:4	LEDLnk	R/W	LED[1:0] 00 = Off 01 = Off 10 = Single 11 = Single	Retain	Link The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single

Table 75: LED Stream Select for Serial LEDs (Global Register) - 88E3082 Only (Continued)
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Function	Mode	HW Rst	SW Rst	Description
3:2	LEDSpd	R/W	11	Retain	Speed The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
1:0	LEDDx/ COLX	R/W	LED[1:0] 00 = Single 01 = Off 10 = Off 11 = Off	Retain	LED Duplex/ COLX The serial LED settings take on the appropriate value defined by the CONFIG8 pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single

Table 76: Reserved Registers - 88E3083 Only
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 77: PHY LED Control Register (bits 14:0 are Global[1] bits)
Offset: 0X18 (Hex), 0r 24 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Must be 0.
14:12	PulseStretch	R/W	0x4	Retain	Pulse stretch duration. This is a global setting. Default Value = 100. 000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11:9	BlinkRate	R/W	0x1	Retain	Blink Rate. This is a global setting. Default Value = 001 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
8:6	SrStrUpdate	R/W	0x2	Retain	Serial Stream Update. This is a global setting. 000 = 10 ms 001 = 21 ms 010 = 42 ms 011 = 84 ms 100 = 170 ms 101 = 340 ms 110 to 111 = Reserved
5:4	Duplex (Reserved for 88E3083)	R/W	LED[1:0] 00 = Off 01 = Single 10 = Single 11 = Single	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single
3:2	Error (Reserved for 88E3083)	R/W	11	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single
1:0	COLX (Reserved for 88E3083)	R/W	LED[1:0] 00 = Off 01 = Single 10 = Single 11 = Single	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single

1. Global register bits are used to control features and functions that are common to all ports in the device.

Table 78: PHY Manual LED Override
Offset: 0x19 (Hex), or 25 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x0	Retain	0000000000
5:4	LED2	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
3:2	LED1	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
1:0	LED0	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 79: VCT™ Register for TXP/N Pins
Offset: 0x1A[1] (Hex), or 26 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EnVCT	R/W, SC	0x0	0x0	Enable VCT The 88E3082/88E3083 devices must be in forced 100 Mbps mode before enabling this bit. 0 = VCT completed 1 = Run VCT After running VCT once, bit 15 = 0 indicates VCT completed. The cable status is reported in the VCTTst bits in registers 26 and 27. Refer to the "Virtual Cable Tester®" feature on page 78.
14:13	VCTTst	RO	0x0	Retain	VCT Test Status These VCT test status bits are valid after completion of VCT. 00 = valid test, normal cable (no short or open in cable) 01 = valid test, short in cable (Impedance < 33 ohm) 10 = valid test, open in cable (Impedance > 333 ohm) 11 = Test fail
12:8	AmpRfln	RO	0x0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bits 14:13) have not indicated test failure.
7:0	DistRfln	RO	0x0	Retain	Distance of Reflection These bits refer to the approximate distance (+/- 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bit 14:13) have not indicated test failure.

1. The results stored in this register apply to the Tx pin pair.

Table 80: VCT™ Register for RXP/N pins
Offset: 0x1B[1] (Hex), or 27 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14:13	VCTTst	RO	0	Retain	VCT Test Status The VCT test status bits are valid after completion of VCT. 00 = valid test, normal cable (no short or open in cable) 01 = valid test, short in cable (Impedance < 33 ohm) 10 = valid test, open in cable (Impedance > 333 ohm) 11 = Test fail
12:8	AmpRfln	RO	0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bit 14:13) have not indicated test failure.
7:0	DistRfln	RO	0	Retain	Distance of Reflection These bits refer to the approximate distance (+/- 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bits 14:13) have not indicated test failure.

1. The results stored in this register apply to the Rx pin pair.

Figure 27: Cable Fault Distance Trend Line

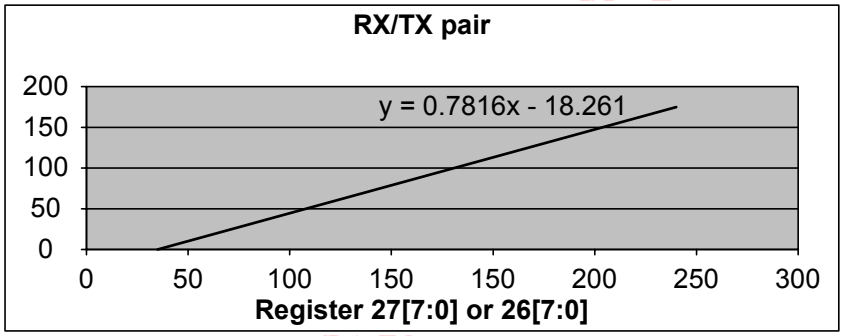


Table 81: PHY Specific Control Register II
Offset: 0x1C (Hex), or 28 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0	0x0	Must be 0000000000000
2	TDRWaitTime	R/W	0x0	Retain	0 = Wait time is 1.5s before TDR test is started 1 = Wait time is 25ms before TDR test is started
1	EnRXCLK	R/W	0x1	Update	0 = Disable MAC interface clock (RXCLK) in sleep mode 1 = Enable MAC interface clock (RXCLK) in sleep mode
0	SelClsA	R/W	SEL_CLASS A	Update	0 = Select Class B driver (typically used in CAT 5 applications) 1 = Select Class A driver - available for 100BASE-TX mode only (typically used in Backplane or direct connect applications, but may be used in CAT 5 applications)

Table 82: Reserved Registers
Offset: 0x1D (Hex), or 29 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 83: Reserved Registers
Offset: 0x1E (Hex), or 30 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Table 84: Reserved Registers
Offset: 0x1F (Hex), or 31 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RES	RES	RES	Do not read or write to this register.

Section 4. Electrical Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can effect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on VDDO with respect to GND[1]	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on AVDDAH or VDDO[2] with respect to GND	-0.5	2.5	+3.6 or VDD(3.3) + 0.5[3] which-ever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on AVDDAL or VDD with respect to GND	-0.5	1.5	+3.6 or VDD(2.5) + 0.5[4] which-ever is less	V
V_{PIN}	Voltage applied to any input pin	-0.5	3.3/2.5	3.6 or VDDO + 0.5[5] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[6]	°C

1. If 3.3V I/O is selected.
2. If 2.5V I/O is selected.
3. $V_{DD(2.5)}$ must never be more than 0.5V greater than $V_{DD(3.3)}$ or damage will result. This implies that power must be applied to $V_{DD(3.3)}$ before or at the same time as $V_{DD(2.5)}$.
4. $V_{DD(1.5)}$ must never be more than 0.5V greater than $V_{DD(2.5)}$ or damage will result. This implies that power must be applied to $V_{DD(2.5)}$ before or at the same time as $V_{DD(1.5)}$.
5. V_{PIN} must never be more than 0.5V greater than VDDO or damage will result.
6. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For Pins VDDO[1, 2]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For Pins AVDDAH, VDDO[2]	2.375	2.5	2.625	V
$V_{DD(1.5)}$	1.5V power supply	For Pins AVDDAL, VDD	1.425	1.5	1.575	V
T_A	Ambient operating temperature	Commercial Devices	0		70[3]	°C
		Industrial Devices[4]	-40		85	°C
T_J	Maximum junction temperature				125[5]	°C

1. If 3.3V I/O is used.
2. The VDDO pins can be set to either 2.5V or 3.3V. To guarantee proper operation, the VDDO voltage level must be set within the range as specified in this table. The VDDO voltage level is selected based on the SEL_25V pin. For example, if 2.5V VDDO is selected, 2.375V Min, 2.5V Typ, and 2.625V Max applies. If 3.3V VDDO is selected, 3.135V Min, 3.3V Typ, and 3.465 Max applies.
3. Commercial operating ambient temperatures are typically below 70 °C, e.g 45 °C ~ 55°C. The 70 °C max is a Marvell® specification limit.
4. Industrial device numbers have an "I" following the Package Code. See "Ordering Part Numbers and Package Markings" on page 168 for details.
5. Refer to white paper TJ Thermal Calculations for more information.

4.3 Package Thermal Information

4.3.1 224-Pin TFBGA package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 224-Pin TFBGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		35.70		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		32.30		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		31.10		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		30.40		C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 224-Pin PQFP package $\psi_{JT} = (T_J - T_C)/P$. P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		0.25		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.46		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.59		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.69		C/W
θ_{JC}	Thermal resistance[1] - junction to case for the 224-Pin TFBGA package $\theta_{JC} = (T_J - T_C)/ PTop$ PTop = Power Dissipation from the top of the package	JEDEC with no air flow		11.70		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the 224-Pin TFBGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		27.00		°C/W
RSET	Internal bias reference	Resistor connected to V_{SS}	1980	2000	2020	Ω

1. Refer to white paper TJ Thermal Calculations for more information.

4.3.2 128-Pin LQFP package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 128-Pin LQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		27.60		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		24.30		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		23.20		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		22.60		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 128-Pin LQFP package $\psi_{JT} = (T_J-T_C)/P$. P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		0.75		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		1.13		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		1.35		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.50		°C/W
θ_{JC}	Thermal resistance[1] - junction to case for the 128-Pin LQFP package $\theta_{JC} = (T_J - T_C)/ PTop$ PTop = Power Dissipation from the top of the package	JEDEC with no air flow		13.80		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the 128-Pin LQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		18.20		°C/W
RSET	Internal bias reference	Resistor connected to GND	1980	2000	2020	Ω

1. Refer to white paper TJ Thermal Calculations for more information.

4.4 Current Consumption

4.4.1 Current Consumption AVDDAH

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(2.5)}$	2.5V Power to analog core, analog I/O	AVDDAH	SMII-100BASE-TX with traffic or idle		203		mA
			SMII-10BASE-T with traffic		222		mA
			RMII - 100BASE-TX with traffic or idle		202		mA
			RMII-10BASE-T with traffic		220		mA
			Auto-Negotiation with no link		220		mA
			Power Down Mode		55		mA
			Sleep Mode		60		mA
			100BASE-FX with traffic		140		mA

1. The values listed are typical values with three LEDs per port and Auto-Negotiation on.

4.4.2 Current Consumption Center Tap

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(2.5)}$	2.5V[2] Power to Center Tap	External Magnetics Center Tap pin	SMII-100BASE-TX with traffic or idle		168[3]		mA
			SMII-10BASE-T with traffic		503		mA
			RMII - 100BASE-TX with traffic or idle		160[3]		mA
			RMII-10BASE-T with traffic		480		mA
			Auto-Negotiation with no link		10		mA
			Power Down Mode		5		mA
			Sleep Mode		5		mA

1. The values listed are typical values with three LEDs per port and Auto-Negotiation on.
2. To determine on chip power from thermal calculations, take the total power and subtract the 62.5 mW per port of power dissipated across the 100 ohm resistors.
3. If Class A (Backplane) drivers are chosen, the center tap current drawn is 322 mA in 100 Mbps mode.

4.4.3 Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(2.5)}$	2.5V/3.3V Power to digital I/O	VDDO	SMII-100BASE-TX with traffic or idle		16		mA
			SMII-10BASE-T with traffic		16		mA
			RMII - 100BASE-TX with traffic or idle		14		mA
			RMII-10BASE-T with traffic		2		mA
			Auto-Negotiation with no link		30		mA
			Power Down Mode		0		mA
			Sleep Mode		0		mA
			100BASE-FX with traffic		16		mA

1. The values listed are typical values with three LEDs per port and Auto-Negotiation on.

4.4.4 Current Consumption AVDDAL

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(1.5)}$	1.5V Power to analog core	AVDDAL	SMII-100BASE-TX with traffic or idle		49		mA
			SMII-10BASE-T with traffic		2		mA
			RMII - 100BASE-TX with traffic or idle		49		mA
			RMII-10BASE-T with traffic		2		mA
			Auto-Negotiation with no link		5		mA
			Power Down Mode		0		mA
			Sleep Mode		0		mA
			100BASE-FX with traffic		0		mA

1. The values listed are typical values with three LEDs per port and Auto-Negotiation on.

4.4.5 Current Consumption VDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(1.5)}$	1.5V Power to digital core	VDD	SMII-100BASE-TX with traffic or idle		162		mA
			SMII-10BASE-T with traffic		80		mA
			RMII - 100BASE-TX with traffic or idle		143		mA
			RMII-10BASE-T with traffic		61		mA
			Auto-Negotiation with no link		84		mA
			Power Down Mode		52		mA
			Sleep Mode		51		mA
			100BASE-FX with traffic		80		mA

1. The values listed are typical values with three LEDs per port and Auto-Negotiation on.

4.4.6 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All digital inputs	VDDO = 3.3V	2.0			V
			VDDO = 2.5V	1.7			V
V_{IL}	Low level input voltage	All digital inputs	VDDO = 3.3V	-0.3		0.8	V
			VDDO = 2.5V	-0.3			V
V_{OH}	High level output voltage	All Pins	I_{OH} = -4 mA V_{DDO} = Min	2.4			V
V_{OL}	Low level output voltage[1]	RXD0, RX_CLK, RX_SYNC	I_{OL}= 4 mA			0.4	V
		All LED and INTn except LEDSER	I_{OL} = 8 mA				
		All other I/O pins	I_{OL}=150 µA				
I_{ILK}	Input leakage current[2]	With pull-up resistor	$0<V_{IN}<V_{DD}$			+ 10 - 50	µA
		With pull-down resistor	$0<V_{IN}<V_{DD}$			+ 50 - 10	µA
		All others	$0<V_{IN}<V_{DD}$			±10	µA
C_{IN}	Input capacitance	All pins				5	pF

1. I/O are dynamically controlled to limit ground bounce.
2. Refer to the table below for Internal Resistor Description.

Table 85: 88E3082/88E3083 Devices Internal Resistor Description

88E3082 Device Pin #	88E3083 Device Pin #	Pin Name	Resistor
D13	--	SEL_RMII	Internal pull-up
H2	116	TCK	Internal pull-up
H1	117	TMS	Internal pull-up
J2	118	TRSTn	Internal pull-up
G1	115	TDI	Internal pull-up
F1	113	NORMAL	Internal pull-up
--	63	RSVD1	Internal pull-up

4.5 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

- 10BASE-T IEEE 802.3 Clause 14
- 100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	P[7:0]_TXP/TXN	10BASE-T no cable	2.2	2.5	2.8	V
		P[7:0]_TXP/TXN	10BASE-T cable model	585[1]			mV
		P[7:0]_TXP/TXN	100BASE-FX mode	0.4	0.8	1.2	V
		P[7:0]_TXP/TXN	100BASE-TX mode	0.950	1.0	1.05	V
	Overshoot	P[7:0]_TXP/TXN	100BASE-TX mode	0		5%	V
	Amplitude symmetry (P/N)	P[7:0]_TXP/TXN	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak differential input voltage accept level	P[7:0]_RXP/RXN	10BASE-T mode	585[2]			mV
		P[7:0]_RXP/RXN	100BASE-FX mode	200			mV
	Peak differential input voltage reject level	P[7:0]_RXP/RXN	100BASE-FX mode	100			mV
	Signal detect assertion	P[7:0]_RXP/RXN	100BASE-TX mode	1000	460[3]		mV peak-peak
	Signal detect de-assertion	P[7:0]_RXP/RXN	100BASE-TX mode	200	360[4]		mV peak-peak

1. IEEE 802.3 Clause 14-2000, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. The input test is actually a template test, IEEE 802.3 Clause 14-2000. Figure 14.17 shows the template for the receive wave form.
3. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The will accept signals typically with 460 mV peak-to-peak differential amplitude.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should be de-assert signal detect (internal signal in 100BASE-TX mode). The will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.6 100BASE-FX Signal Detect Parameters

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH_SDET}	Signal Detect Assertion	P[7:0]_SDET	100BASE-FX mode	2.2			V
V_{IL_SDET}	Signal Detect De-assertion	P[7:0]_SDET	100BASE-FX mode			1.9	V

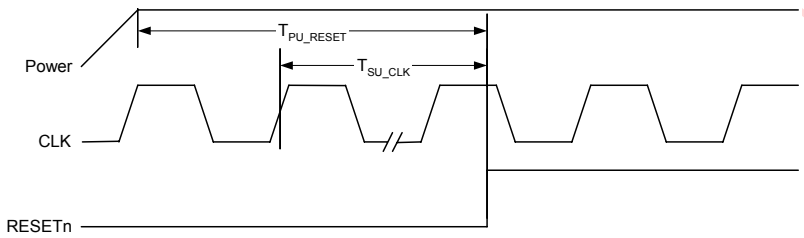
4.7 AC Electrical Specifications

4.7.1 Reset and Configuration Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Power up to hardware de-asserted		10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			clks

Figure 28: Reset Timing

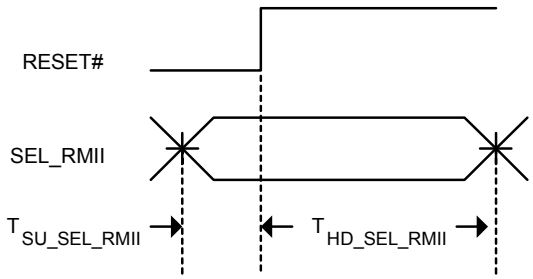


4.7.2 Reset Select RMII

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_SEL\ RMII}$	SEL_RMII to Reset de-asserted Setup Time		1			ns
$T_{HD\_SEL\ RMII}$	SEL_RMII to Reset de-asserted Hold Time		∞			ns

Figure 29: Reset Select RMII

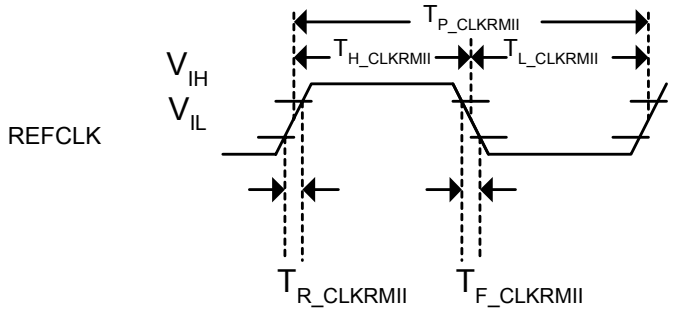


4.7.3 Clock Timing RMII

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{R\_CLKRMII}$	REFCLK Rise time	V_{IL}(max) to V_{IH}(min)			3.0	ns
$T_{F\_CLKRMII}$	REFCLK Fall time	V_{IH}(min) to V_{IL}(max)			3.0	ns
$T_{P\_CLKRMII}$	REFCLK Period		20-50 ppm	20	20+50 ppm	ns
$T_{H\_CLKRMII}$	REFCLK High		7.0	10	13	ns
$T_{L\_CLKRMII}$	REFCLK Low		7.0	10	13	ns

Figure 30: Clock Timing RMII

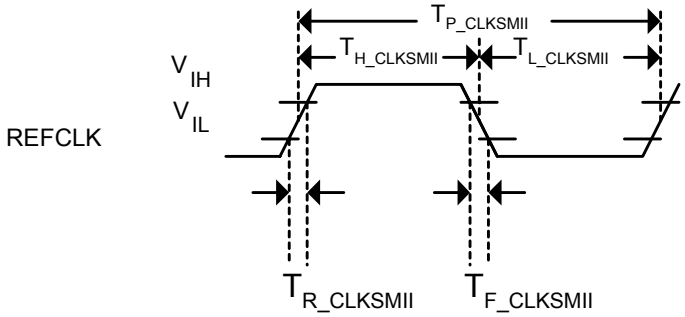


4.7.4 Clock Timing SMII

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{R\_CLKSMII}$	REFCLK Rise time	V_{IL}(max) to V_{IH}(min)			3.0	ns
$T_{F\_CLKSMII}$	REFCLK Fall time	V_{IH}(min) to V_{IL}(max)			3.0	ns
$T_{P\_CLKSMII}$	REFCLK Period		8-50 ppm	8 ppm	8+50 ppm	ns
$T_{H\_CLKSMII}$	REFCLK High		2.8	4.0	5.2	ns
$T_{L\_CLKSMII}$	REFCLK Low		2.8	4.0	5.2	ns

Figure 31: Clock Timing SMII

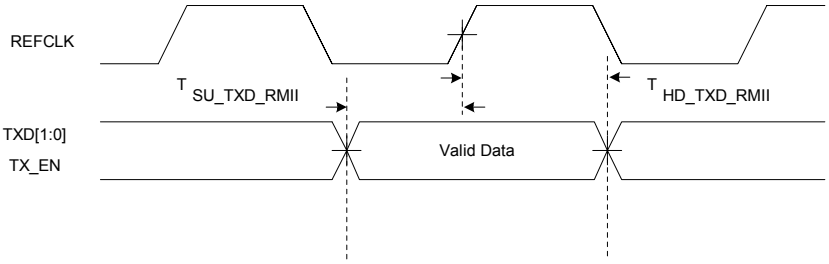


4.7.5 RMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TXD\_RMII}$	TXD[1:0], TX_EN, Data Setup to REFCLK rising edge		4			ns
$T_{HD\_TXD\_RMII}$	TXD[1:0], TX_EN, Data Hold from REFCLK rising edge		2			ns

Figure 32: RMII Transmit Timing

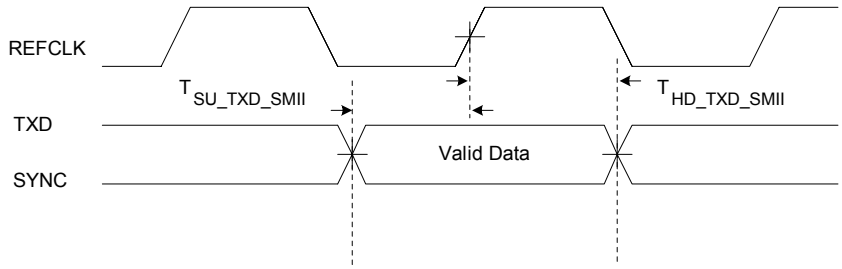


4.7.6 SMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TXD\_SMII}$	P[7:0]_TXD,TX_EN SYNC Setup to REFCLK		1.5			ns
$T_{HD\_TXD\_SMII}$	P[7:0]_TXD, TX_EN SYNC Hold from REFCLK		1.0			ns

Figure 33: SMII Transmit Timing

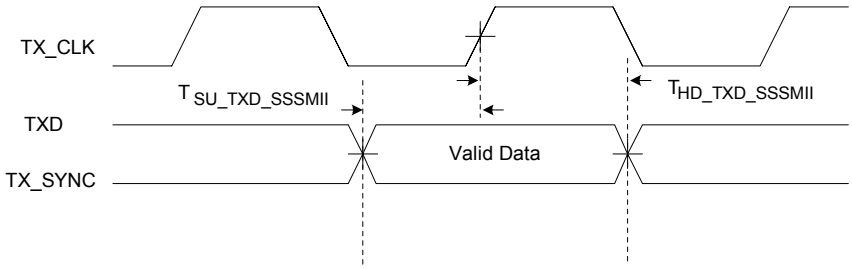


4.7.7 SSSMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TXD\_SSSMII}$	TXD, TX_SYNC Setup to TX_CLK		1.5			ns
$T_{HD\_TXD\_SSSMII}$	TXD, TX_SYNC Hold from TX_CLK		1.0			ns

Figure 34: SSSMII Transmit Timing



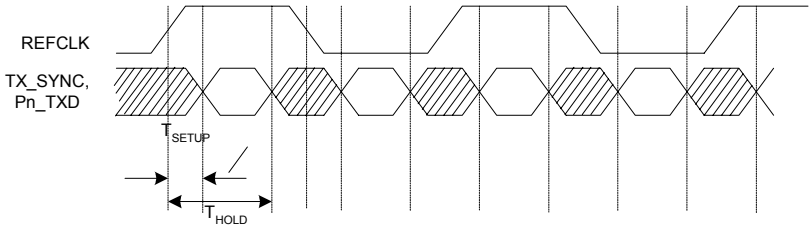
4.7.8 DDR-SSSMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_TXD\_DDR\_SSSMII}$	P[n][1]_TXD, TX_SYNC Setup to REFCLK		-0.9			ns
$T_{HD\_TXD\_DDR\_SSSMII}$	P[n][1]_TXD, TX_SYNC Hold from REFCLK		2.7			ns

1. Where n are the DDR-SSSMII ports.

Figure 35: DDR-SSSMII Transmit Timing



4.7.9 RMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{DLY\_RXD\_RMII}$	REFCLK rising edge to P[1:0]_RXD, RX_ER and CRS_DV delay	Initial rising edge of CRS_DV is asynchronous to REFCLK	2.0		14.0	ns
$T_{R\_RXD\_RMII}$	P[1:0]_RXD, RX_ER, CRS_DV Rise time	V_{IL}(max) to V_{IH}(min)	1.0		2.5	ns
$T_{F\_RXD\_RMII}$	P[1:0]_RXD, RX_ER, CRS_DV Fall time	V_{IH}(min) to V_{IL}(max)	1.0		2.5	ns

Figure 36: RMII Rise and Fall Times

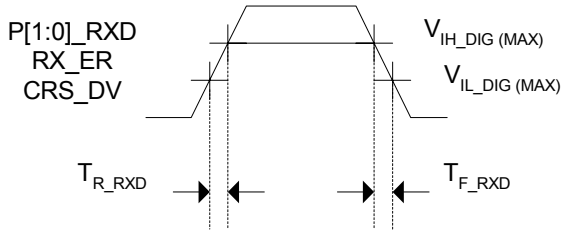
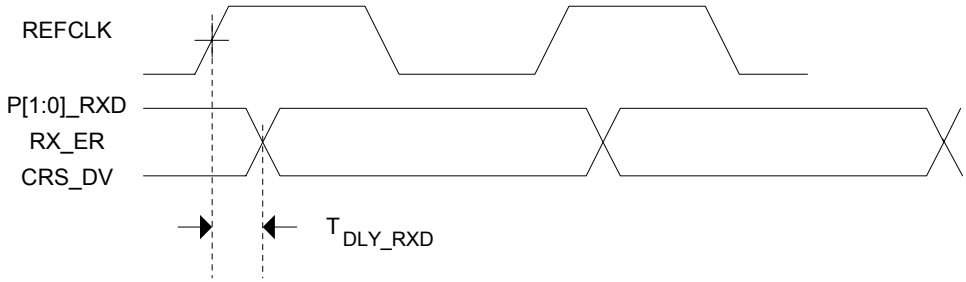


Figure 37: RMII Receive Delay



4.7.10 SMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{DLY\_RXD\_SMII}$	REFCLK rising edge to RXD delay		1.5		5	ns
$T_{R\_RXD\_SMII}$	RXD and SYNC Rise time	V_{IL}(max) to V_{IH}(min)	1.0		2.5	ns
$T_{F\_RXD\_SMII}$	RXD and SYNC Fall time	V_{IH}(min) to V_{IL}(max)	1.0		2.5	ns

Figure 38: SMII Rise and Fall Times

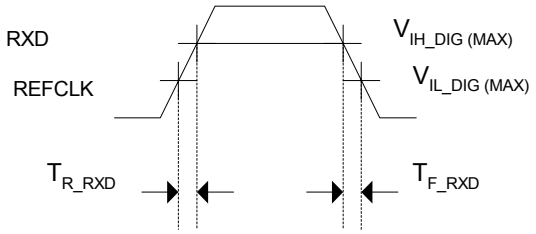
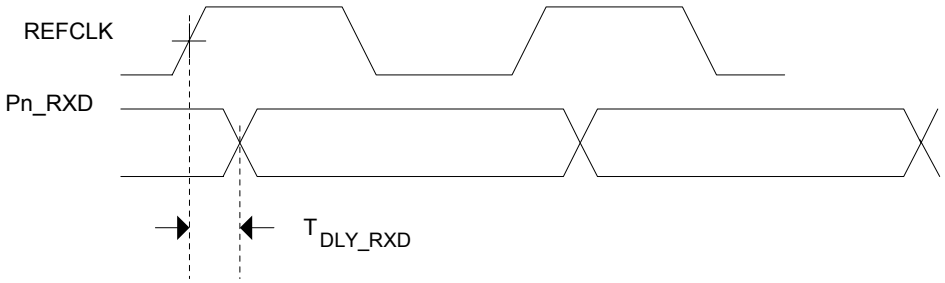


Figure 39: SMII Receive Delay



4.7.11 SSSMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{DLY\_RXD\_SSSMII}$	RX_CLK rising edge to RXD and RX_SYNC delay		1.5		5	ns
$T_{R\_RXD\_SSSMII}$	RXD, RX_CLK and RX_SYNC Rise time	VIL(max) to VIH(min)	1.0		2.5	ns
$T_{F\_RXD\_SSSMII}$	RXD, RX_CLK and RX_SYNC Fall time	VIH(min) to VIL(max)	1.0		2.5	ns

Figure 40: SSSMII Rise and Fall Times

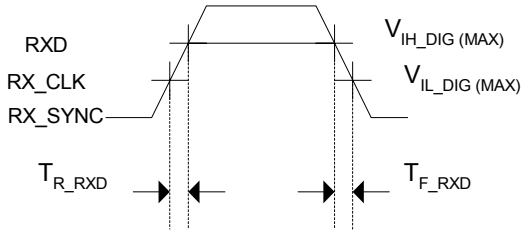
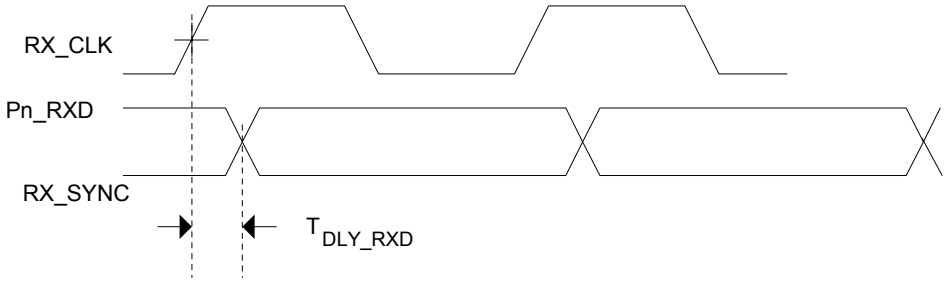


Figure 41: SSSMII Receive Delay



4.7.12 DDR-SSSMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_RXD\_DDR\_SSSMII}$	RXD_O valid to RX_CLK rising edge or RXD_E valid to RX_CLK falling edge			1.4		ns
$T_{HD\_RXD\_DDR\_SSSMII}$	RX_CLK rising edge to RXD_O valid or RX_CLK falling edge to RXD_E valid			1.2		ns

Figure 42: DDR-SSSMII Rise and Fall times

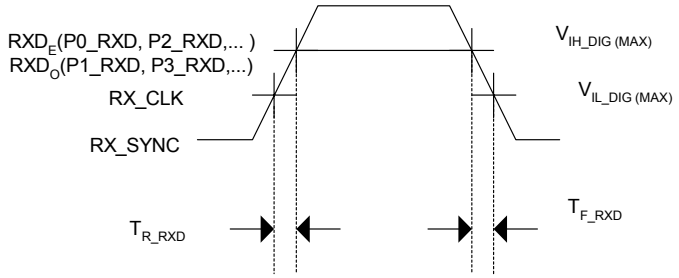
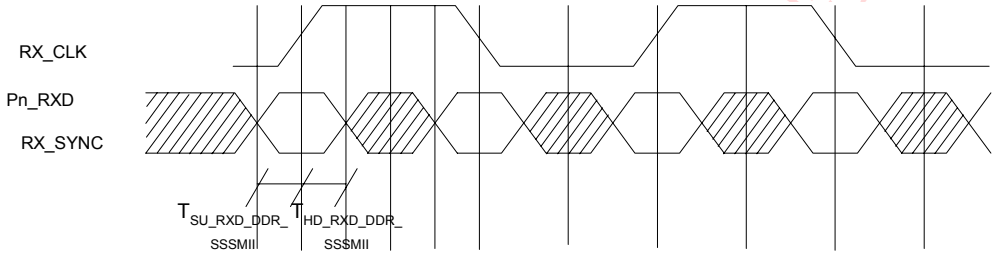


Figure 43: DDR-SSSMII Receive Delay



4.8 Latency Timing

4.8.1 RMII to 100BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_MDI\_100}$	100BASE-TX TX_EN asserted to /J/		231		259	ns
$T_{DA\_TXEN\_MDI\_100}$	100BASE-TX TX_EN de-asserted to /T/		231		259	ns

4.8.2 RMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

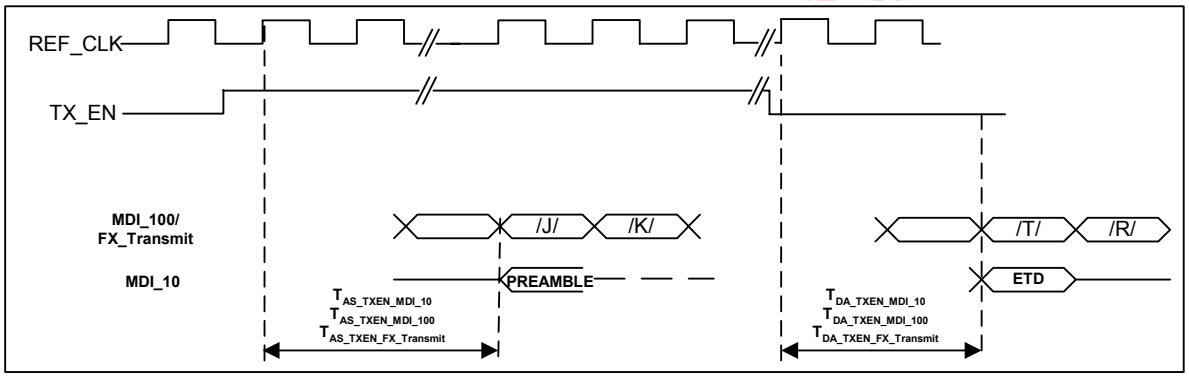
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_MDI\_10}$	100BASE-TX TX_EN asserted to Preamble		1364		1484	ns
$T_{DA\_TXEN\_MDI\_10}$	100BASE-TX TX_EN de-asserted to ETD		1364		1484	ns

4.8.3 RMII to 100BASE-FX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_FX\_Transmit}$	100BASE-FX TX_EN asserted to /J/		223		251	ns
$T_{DA\_TXEN\_FX\_Transmit}$	100BASE-FX TX_EN de-asserted to /T/		223		251	ns

Figure 44: RMII to 10/100BASE-T and 100BASE-FX Transmit Latency Timing



4.8.4 SMII/SSSMII/DDR-SSSMII to 100BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_MDI\_100}$	100BASE-TX TX_EN asserted to /J/		227		235	ns
$T_{DA\_TXEN\_MDI\_100}$	100BASE-TX TX_EN de-asserted to /T/		227		235	ns

4.8.5 SMII/SSSMII/DDR-SSSMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

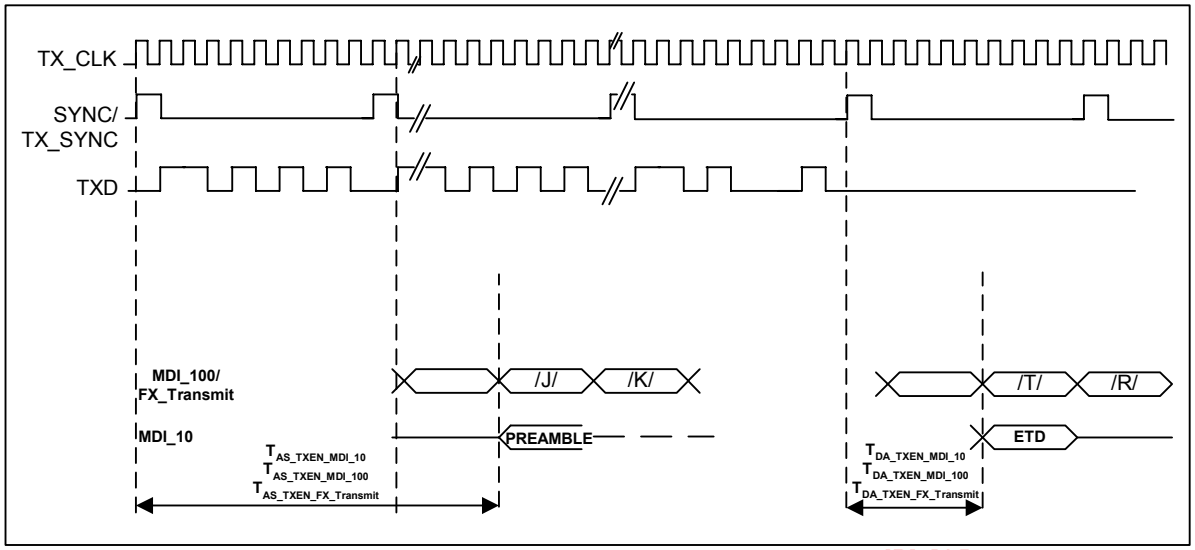
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_MDI\_10}$	100BASE-TX TX_EN asserted to Preamble		1348		1448	ns
$T_{DA\_TXEN\_MDI\_10}$	100BASE-TX TX_EN de-asserted to ETD		1348		1448	ns

4.8.6 SMII/SSSMII/DDR-SSSMII to 100BASE-FX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXEN\_FX\_Transmit}$	100BASE-FX TX_EN asserted to /J/		219		227	ns
$T_{DA\_TXEN\_FX\_Transmit}$	100BASE-FX TX_EN de-asserted to /T/		219		227	ns

Figure 45: SMII/SSSMII/DDR-SSSMII to 10/100BASE-T and 100BASE-FX Transmit Latency Timing



4.8.7 100BASE-T to RMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXD\_100}$	Receive /J/ to RXD assert		283		303	ns
$T_{AS\_MDI\_CRS\_DV\_100}$	Receive /J/ to CRS_DV assert		99		119	ns
$T_{DA\_MDI\_RXD\_100}$	Receive /T/ to RXD de-assert		283		303	ns
$T_{DA\_MDI\_CRS\_DV\_100}$	Receive /T/ to CRS_DV de-assert		99		119	ns

4.8.8 10BASE-T to RMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

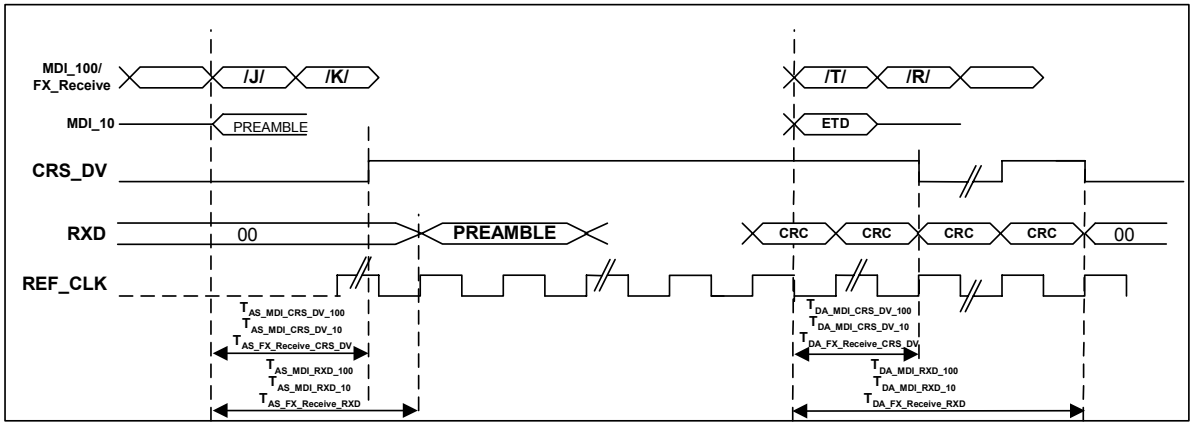
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXD\_10}$	Receive Start of Frame to RXD assert		1980		2100	ns
$T_{AS\_MDI\_CRS\_DV\_10}$	Receive Start of Frame to CRS_DV assert		260		500	ns
$T_{DA\_MDI\_RXD\_10}$	Receive End of Frame to RXD de-assert		1980		2100	ns
$T_{DA\_MDI\_CRS\_DV\_10}$	Receive End of Frame to CRS_DV de-assert		260		500	ns

4.8.9 100BASE-FX to RMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_FX\_Receive\_RXD}$	Receive /J/ to RXD assert		283		303	ns
$T_{AS\_FX\_Receive\_CRS\_DV}$	Receive /J/ to CRS_DV assert		99		119	ns
$T_{DA\_FX\_Receive\_RXD}$	Receive /T/ to RXD de-assert		283		303	ns
$T_{DA\_FX\_Receive\_CRS\_DV}$	Receive /T/ to CRS_DV de-assert		99		119	ns

Figure 46: 10/100BASE-T and 100BASE-FX to RMII Receive Latency Timing



4.8.10 100BASE-T to SMII/SSSMII/DDR-SSSMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXD\_100}$	Receive /J/ to RXD assert		335		435	ns
$T_{AS\_MDI\_CRS\_100}$	Receive /J/ to CRS assert		59		139	ns
$T_{DA\_MDI\_RXD\_100}$	Receive /T/ to RXD de-assert		335		435	ns
$T_{DA\_MDI\_CRS\_100}$	Receive /T/ to CRS de-assert		59		139	ns

4.8.11 10BASE-T to SMII/SSSMII/DDR-SSSMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

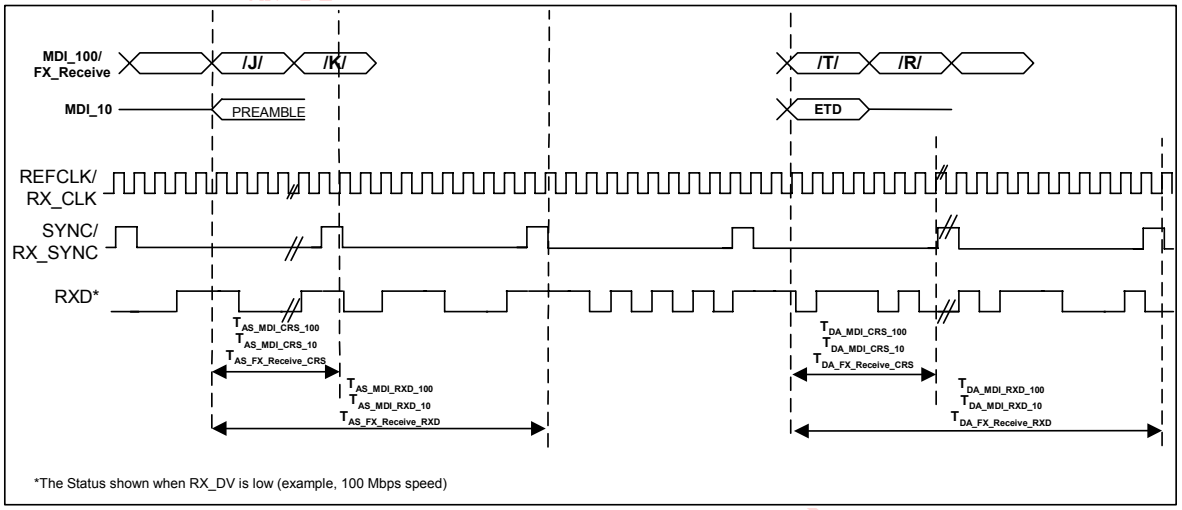
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXD\_10}$	Receive Start of Frame to RXD assert		3132		3240	ns
$T_{AS\_MDI\_CRS\_10}$	Receive Start of Frame to CRS assert		210		490	ns
$T_{DA\_MDI\_RXD\_10}$	Receive End of Frame to RXD de-assert		3132		3240	ns
$T_{DA\_MDI\_CRS\_10}$	Receive End of Frame to CRS de-assert		210		490	ns

4.8.12 100BASE-FX to SMII/SSSMII/DDR-SSSMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_FX\_Receive\_RXD}$	Receive /J/ to RXD assert		355		435	ns
$T_{AS\_FX\_Receive\_CRS}$	Receive /J/ to CRS assert		59		139	ns
$T_{DA\_FX\_Receive\_RXD}$	Receive /T/ to RXD de-assert		355		435	ns
$T_{DA\_FX\_Receive\_CRS}$	Receive /T/ to CRS de-assert		59		139	ns

Figure 47: 10/100BASE-T and 100BASE-FX to SMII/SSSMII/DDR-SSSMII Receive Latency Timing

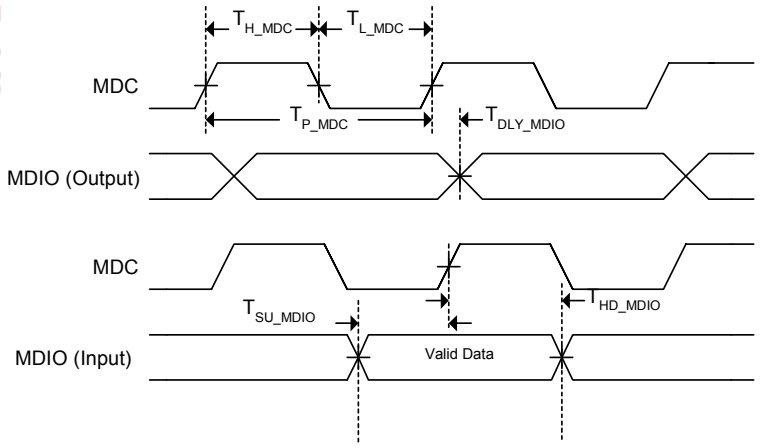


4.9 Serial Management Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		120			ns
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns

Figure 48: MII Serial Management Timing

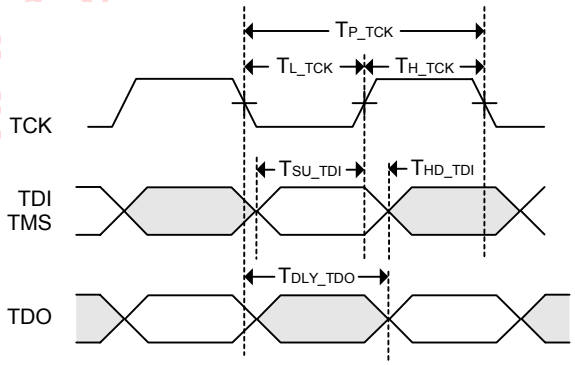


4.10 JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		40			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		20	ns

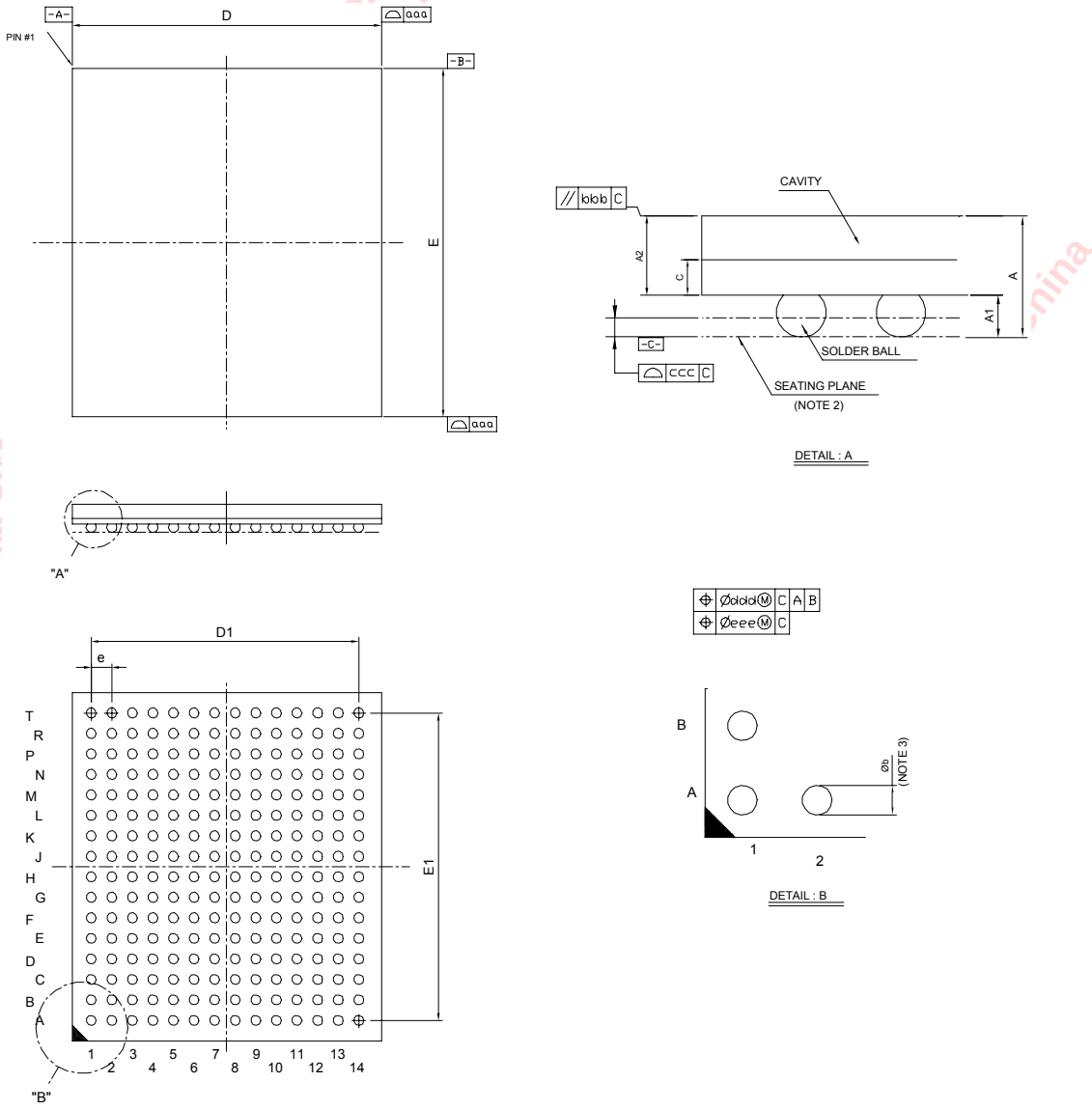
Figure 49: JTAG Timing



Section 5. Package Mechanical Dimensions

5.1 88E3082 Package Mechanical Dimensions

Figure 50: 88E3082 224-pin TFBGA package



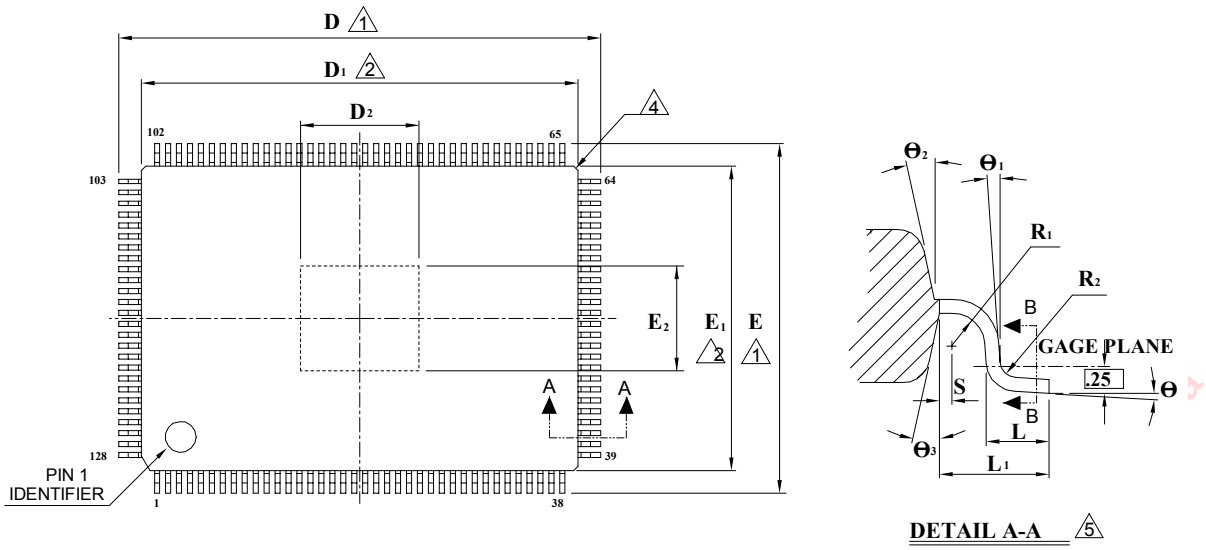
(All dimensions in mm.)

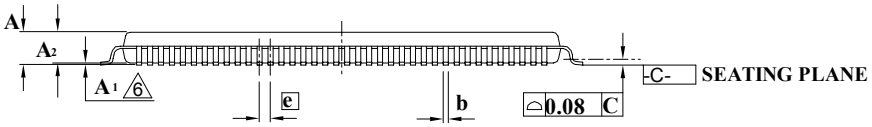
Dimensions in mm			
Symbol	**MIN**	**NOM**	**MAX**
A			1.50
A1	0.30	0.40	0.50
A2	0.84	0.89	0.94
c		0.36	
D	14.90	15.00	15.10
E	16.90	17.00	17.10
D1		13.00 REF	
E1		15.00REF	
e		1.00BSC	
b	0.40	0.50	0.60
aaa		0.10	
bbb		0.20	
ccc		0.15	
ddd		0.15	
eee		0.08	
MD/ME		14/16	

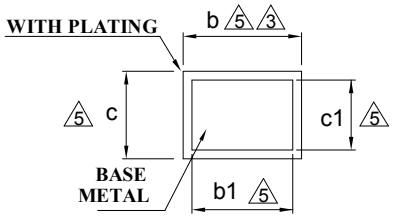
NOTE:
1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY
6. MD/ME: MAXIMUM BALL MATRIX FOR PACKAGE

5.2 88E3083 Package Mechanical Dimensions

Figure 51: 88E3083 128-pin 14x20 LQFP package







NOTE :

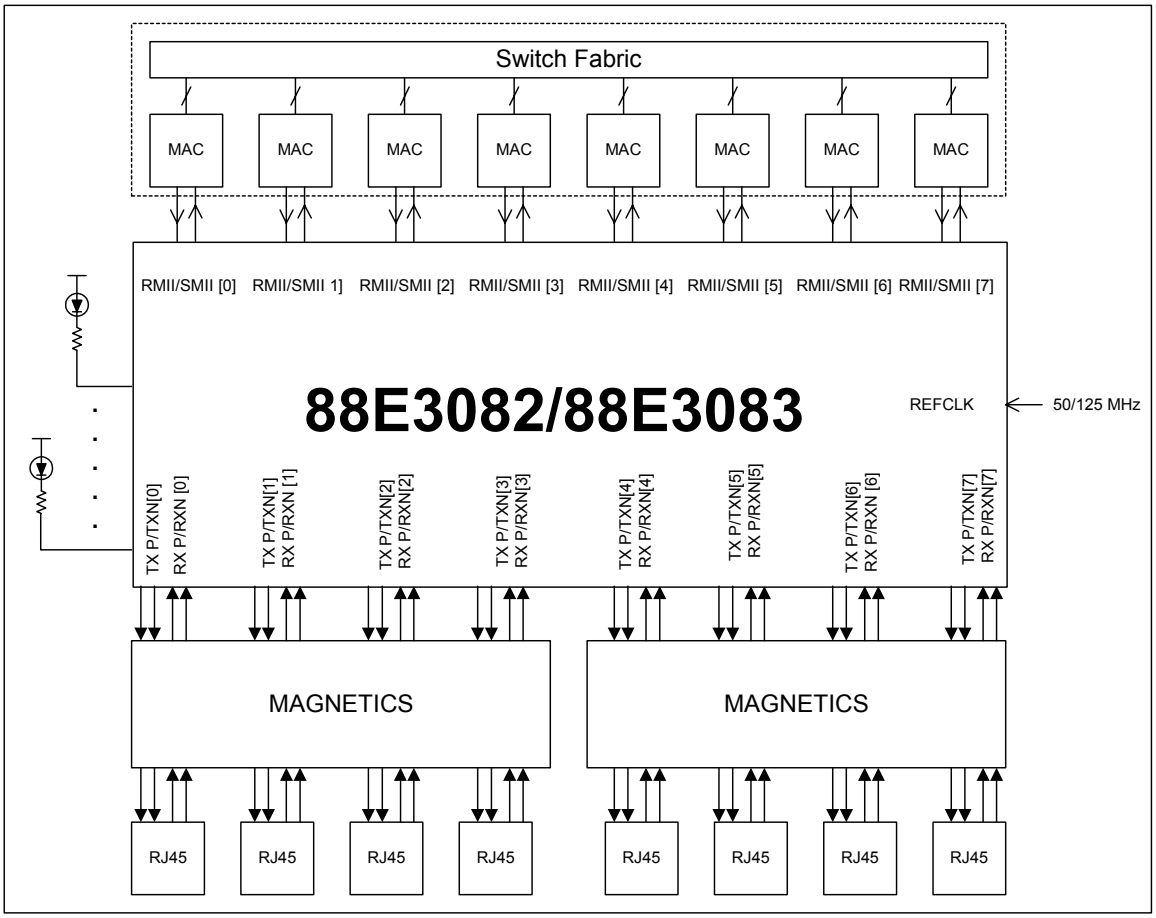
1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

	Dimensions in mm		
Symbol	**MIN**	**NOM**	**MAX**
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	--	0.20
c1	0.09	--	0.16
D	21.90	22.00	22.10
D1	19.90	20.00	20.10
E	15.90	16.00	16.10
D2	6.70 BSC		
E1	13.90	14.00	14.10
E2	5.74 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	--	--
R2	0.08	--	0.20
S	0.20	--	--
θ	0°	3.5°	7°
θ1	4° TYP		
θ2	12° TYP		
θ3	12° TYP		

Section 6. Application Examples

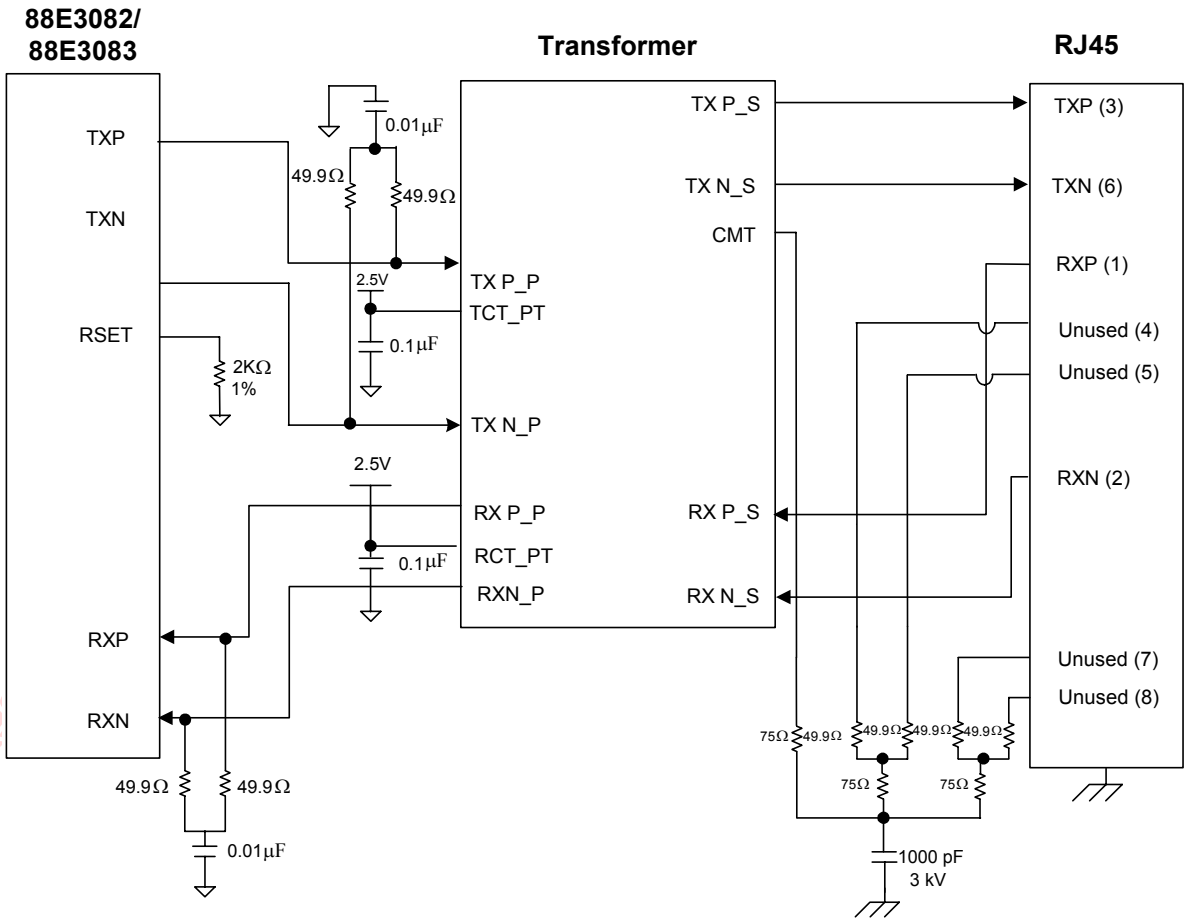
6.1 Switching Application (10/100 TX Mode)

Figure 52: Switching Application (10/100 TX Mode)



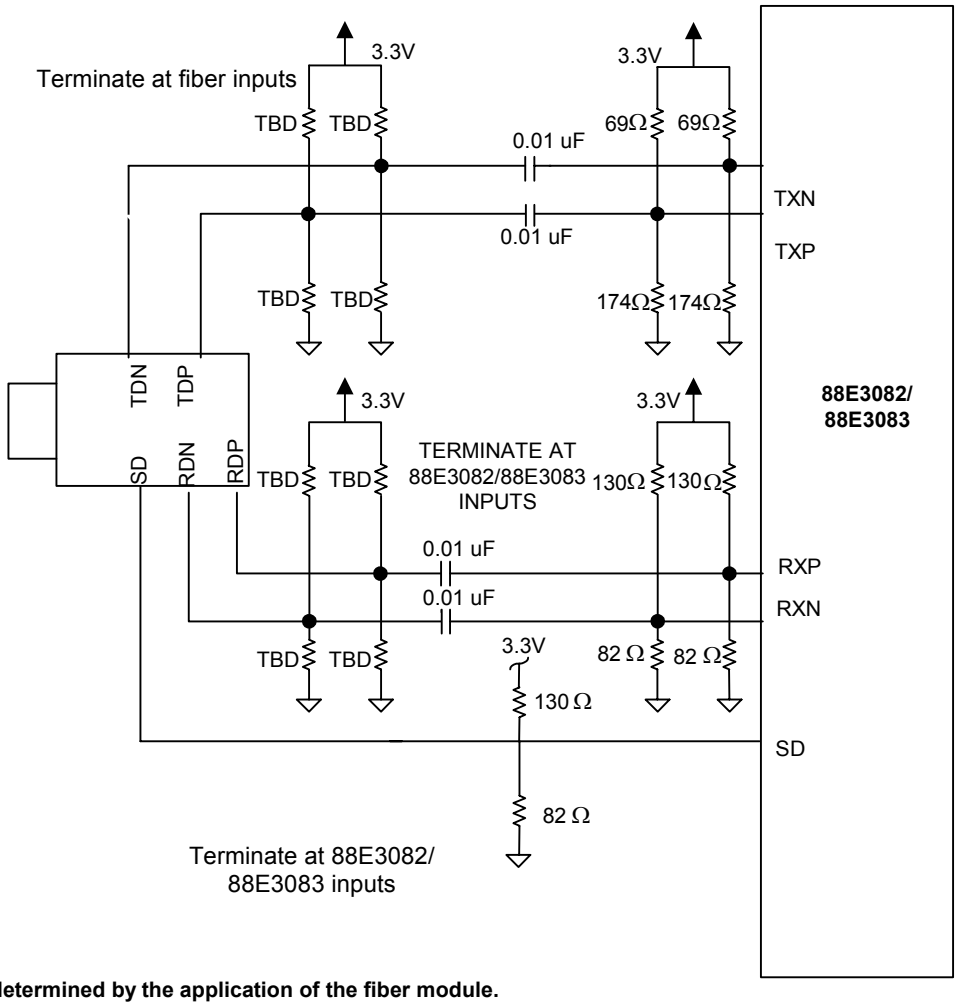
6.2 10/100BASE-T Circuit Application

Figure 53: 10/100BASE-T Circuit Application



6.3 FX Interface to 3.3V Fiber Transceiver

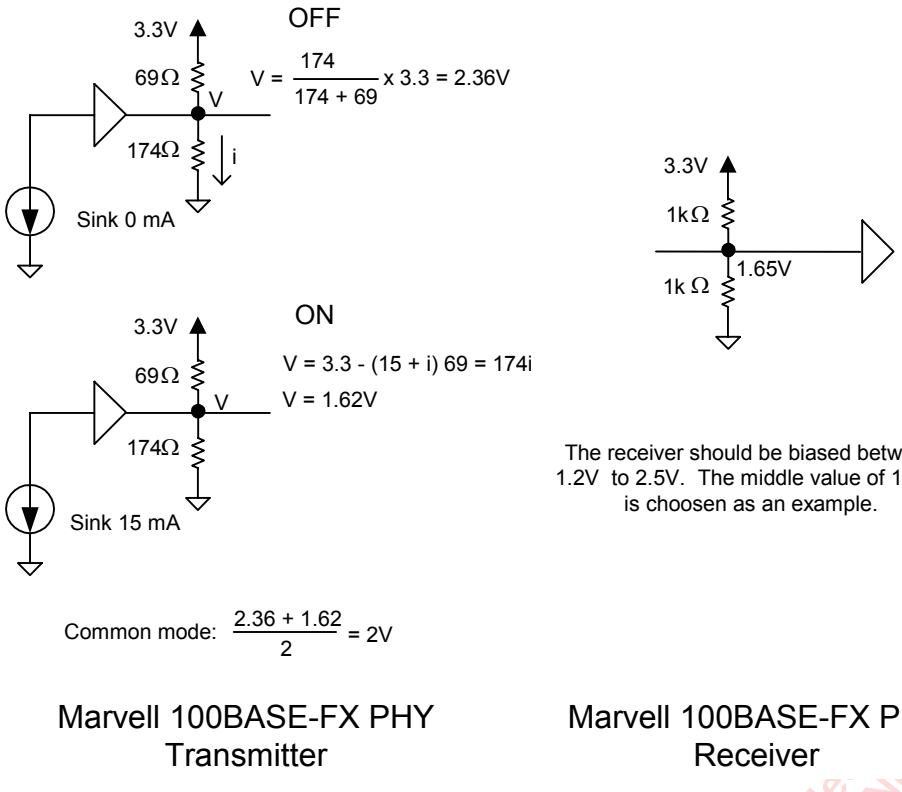
Figure 54: FX Interface to 3.3V Fiber Transceiver



TBD -- To be determined by the application of the fiber module.

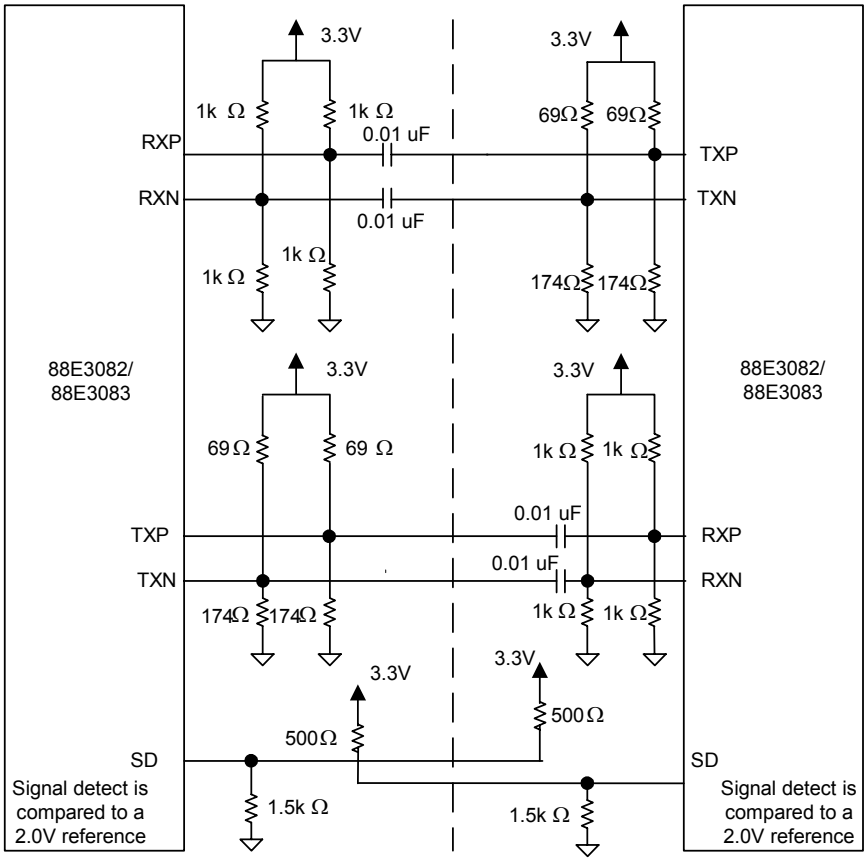
6.4 Transmitter - Receiver Diagram

Figure 55: Transmitter - Receiver Diagram



6.5 88E3082 to 88E3082 Backplane Connection - 100BASE-FX Interface

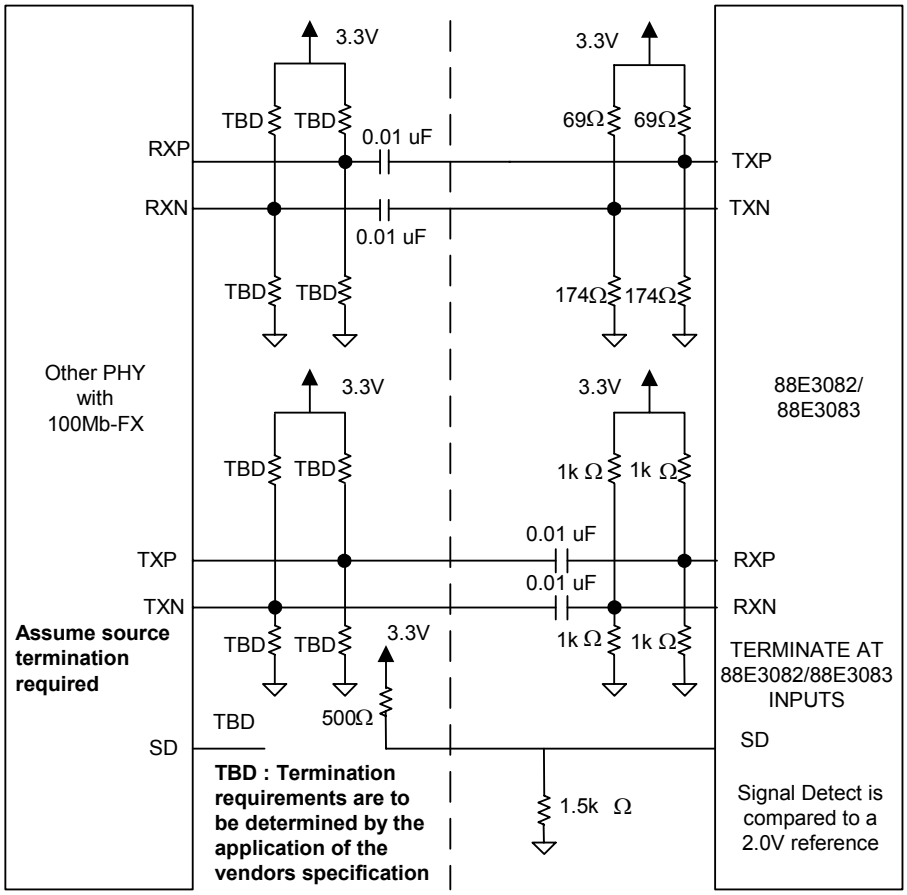
Figure 56: 88E3082 to 88E3082 Backplane Connection - 100BASE-FX Interface



Marvell PHY to Marvell PHY 100Base-FX
Connection Through a Backplane

6.6 88E3082 to Another Vendor's PHY - 100BASE-FX Interface

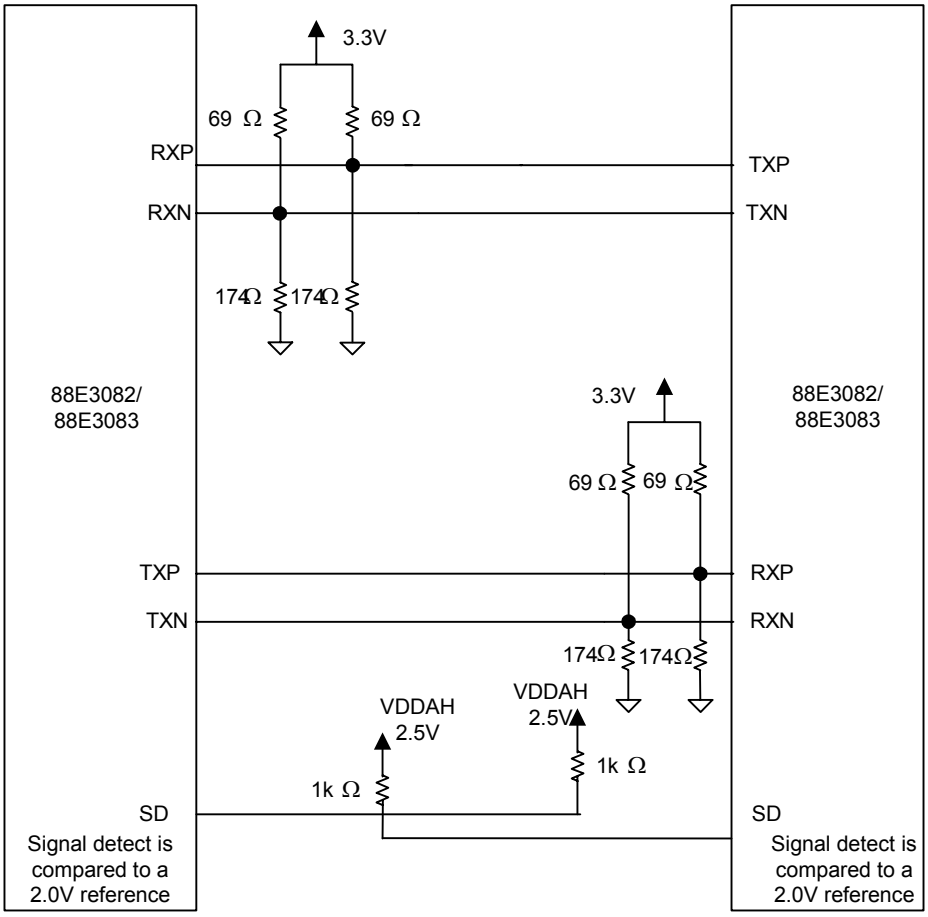
Figure 57: 88E3082 to Another Vendor's PHY - 100BASE-FX Interface



Marvell PHY to Another Vendor's PHY With the 100Base-FX Interface through a backplane

6.7 Marvell® PHY to Marvell PHY Direct Connection

Figure 58: Marvell® PHY to Marvell PHY Direct Connection



Section 7. Order Information

7.1 Ordering Part Numbers and Package Markings

Figure 59 shows the ordering part numbering scheme for the 88E3082/88E3083 devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 59: Sample Part Number

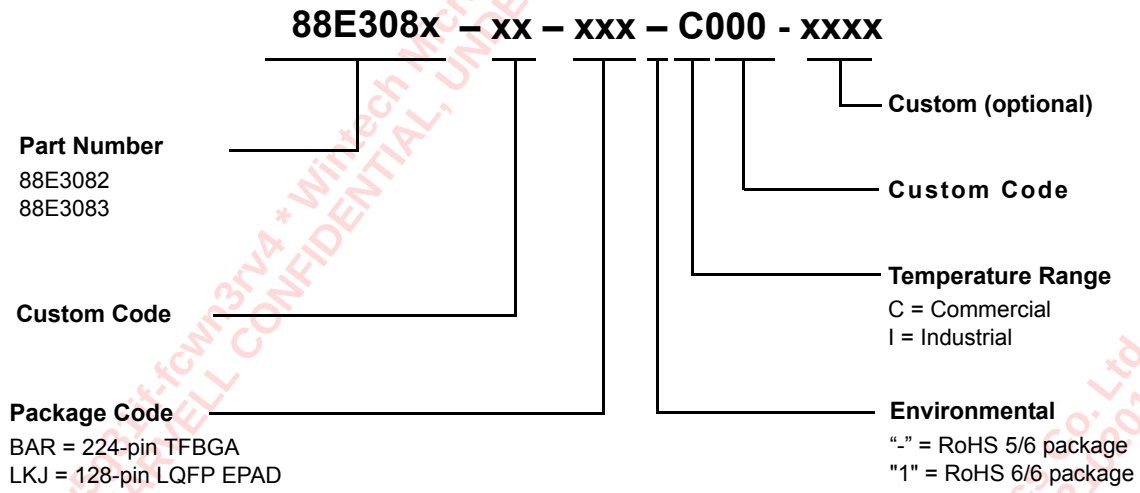


Table 86: 88E3082/88E3083 RoHS 5/6 Part Order Options

Package Type	Part Order Number
88E3082 224-pin TFBGA - Commercial	88E3082-XX-BAR-C000
88E3082 224-pin TFBGA - Industrial	88E3082-XX-BAR-I000
88E3083 128-pin LQFP EPAD - Commercial	88E3083-XX-LKJ-C000

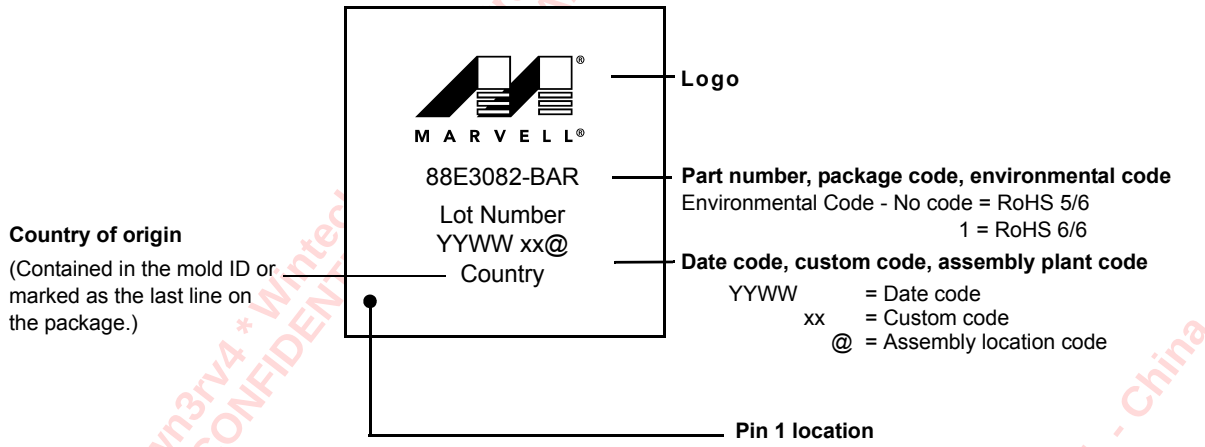
Table 87: 88E3082/88E3083 RoHS 6/6 Part Order Options

Package Type	Part Order Number
88E3082 224-pin TFBGA - Commercial	88E3082-XX-BAR1C000
88E3082 224-pin TFBGA - Industrial	88E3082-XX-BAR1I000
88E3083 128-pin LQFP EPAD - Commercial	88E3083-XX-LKJ1C000

7.1.1 RoHS 5/6 Compliant Marking Examples

Figure 60 is an example of the package marking and pin 1 location for the 88E3082 224-pin TFBGA Commercial RoHS 5/6 compliant package.

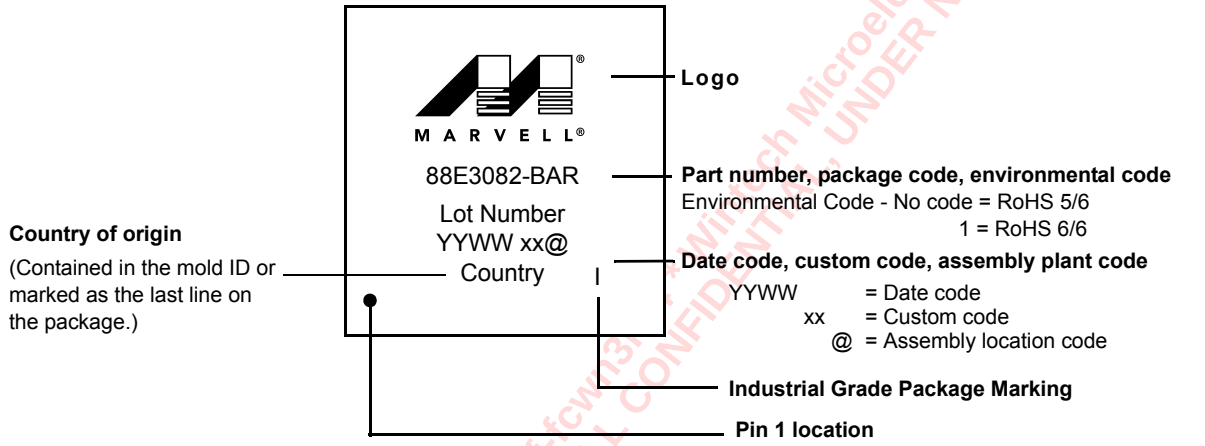
Figure 60: 88E3082 224-pin TFBGA Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 61 is an example of the package marking and pin 1 location for the 88E3082 224-pin TFBGA Industrial RoHS 5/6 compliant package.

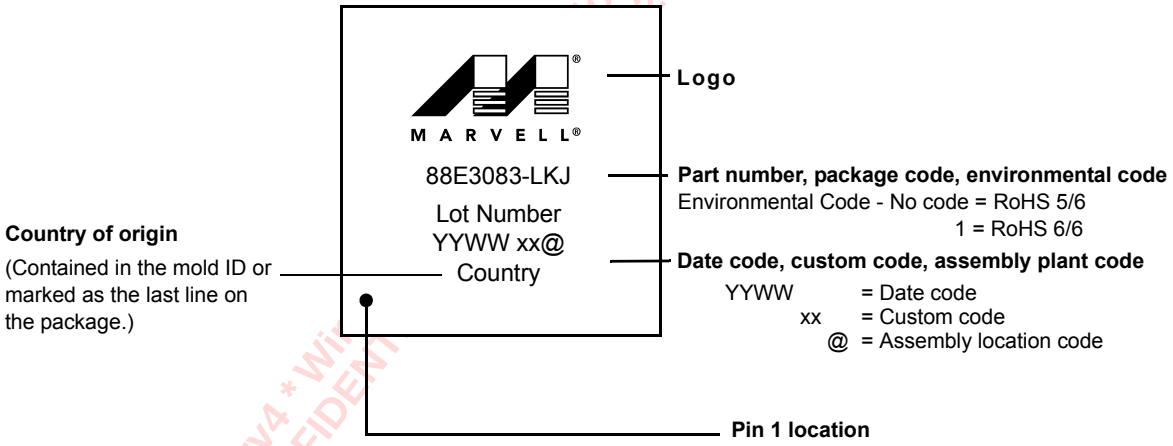
Figure 61: 88E3082 224-pin TFBGA Industrial RoHS 5/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 62 is an example of the package marking and pin 1 location for the 88E3083 128-pin LQFP Commercial RoHS 5/6 compliant package.

Figure 62: 88E3083 128-pin LQFP Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location

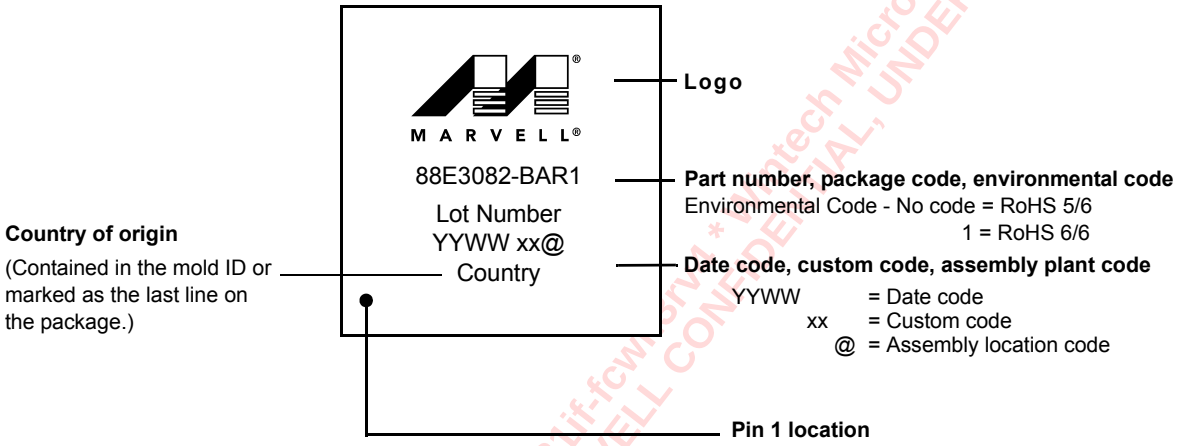


Note: The above example is not drawn to scale. Location of markings is approximate.

7.1.2 RoHS 6/6 Compliant Marking Examples

Figure 63 is an example of the package marking and pin 1 location for the 88E3082 224-pin TFBGA Commercial RoHS 6/6 compliant package.

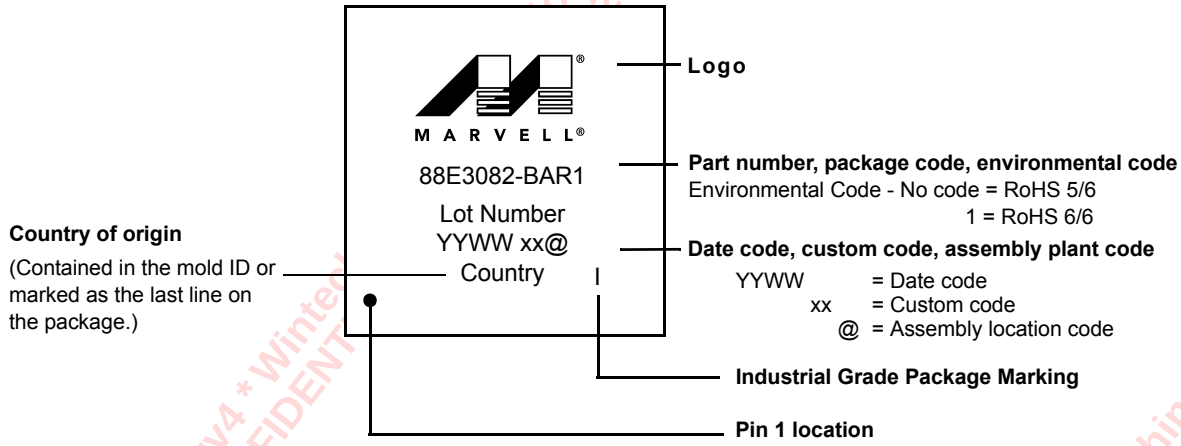
Figure 63: 88E3082 224-pin TFBGA Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 64 is an example of the package marking and pin 1 location for the 88E3082 224-pin TFBGA Industrial RoHS 6/6 compliant package.

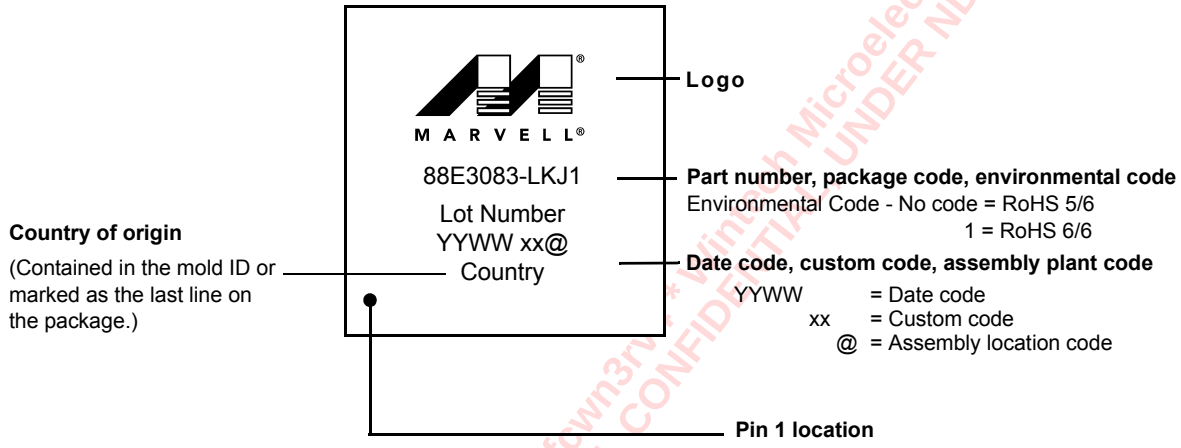
Figure 64: 88E3082 224-pin TFBGA Industrial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 65 is an example of the package marking and pin 1 location for the 88E3083 128-pin LQFP Commercial RoHS 6/6 compliant package.

Figure 65: 88E3083 128-pin LQFP Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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