

M.F.A Munsif,
EG/2021/4684,
Faculty of Engineering,
University of Ruhuna.

Through:
Mr.W.N.B.A.G.Priyankara,
Academic Advisor,
Department of Electrical and Information Engineering,
Faculty of Engineering,
University of Ruhuna.

To:
Dr. Thilina Weerasinghe
Module Coordinator,
Department of Electrical and Information Engineering,
Faculty of Engineering,
University of Ruhuna.

Dear Sir,

Excuse for the late coming for the laboratory session (EE 2.2)

I am M.F.A Munsif (EG/2021/4684) from the 23rd batch of the Faculty of Engineering, University of Ruhuna. I could not attend the laboratory session on the topic of “Sequential logic circuits” (Lab 2.2) conducted on 5th December 2022. What happened was we came to the corridor of the laboratory by 1.20 pm. We have seen the instructors informing other groups to come into the lab. Due to our misunderstanding, we thought that the instructor of the EE 2.2 lab would inform us to come to the lab. But that wasn't the case, then we went to the lab at 1.40 pm and asked. By then we were late. For that reason, we could not do the laboratory Session. I apologize for not attending on time to the laboratory session. I promise to act responsibly to avoid such mistakes in coming labs.

I am grateful if you kindly consider this matter and grant permission to reschedule the above laboratory session.

Name : Munsif M.F.A
Reg No : EG/2021/4684
Group No : GB 29

Thank you.
Yours truly,
M.F.A Munsif
EG/2021/4684
08/12/2022