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Lab 1 Report
ECE 2031 L07
24 January 2022

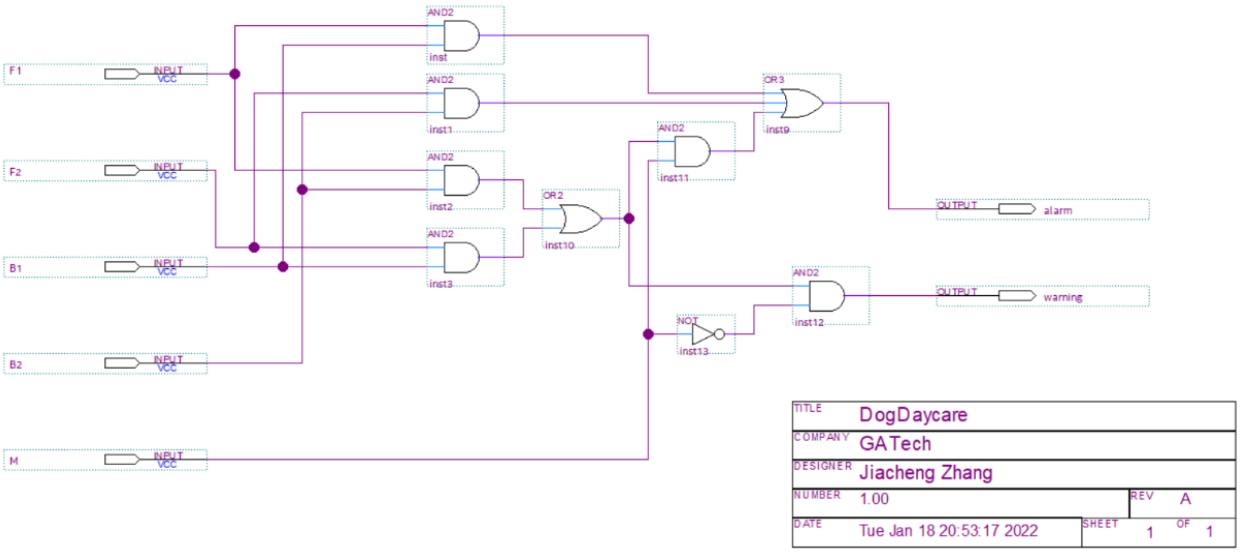

Figure 1. Schematic of circuit implementing alarm = $F_1 \cdot B_1 + F_2 \cdot B_2 + (F_1 \cdot B_2 + F_2 \cdot B_1) \cdot M$ and warning = $(F_1 \cdot B_2 + F_2 \cdot B_1) \cdot /M$.

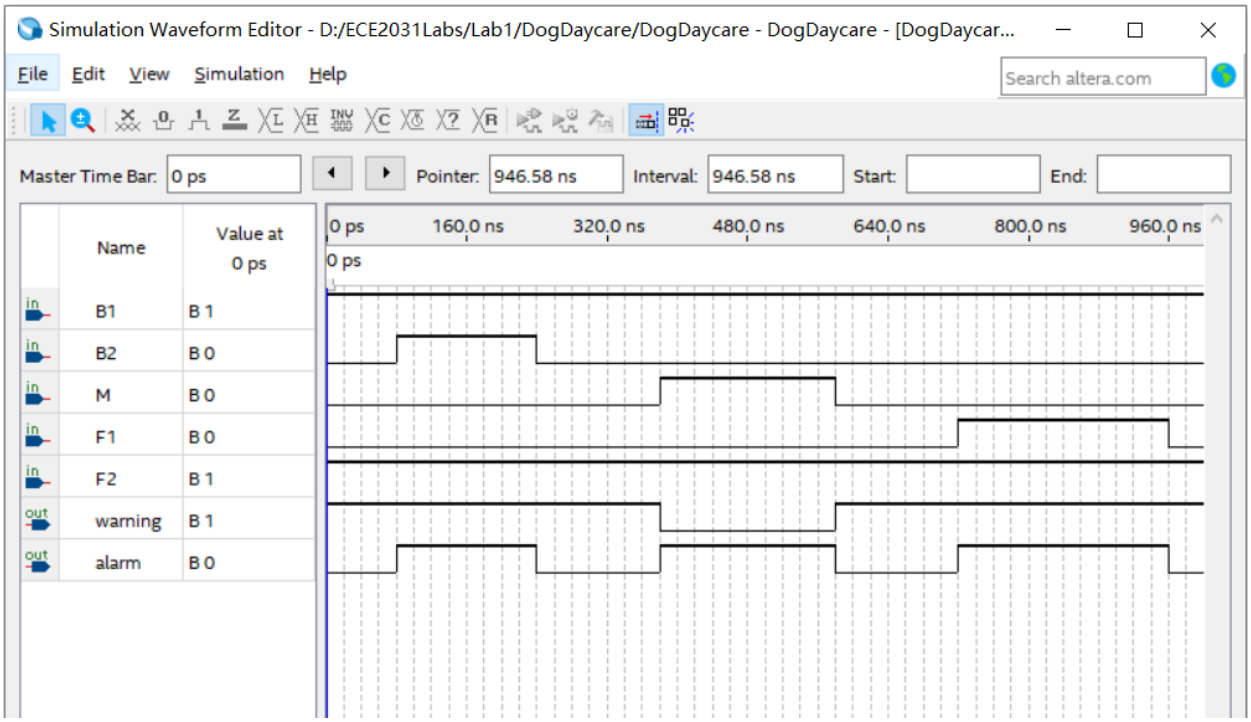

Figure 2. A simulation waveform to testify some specific cases the circuit implements.

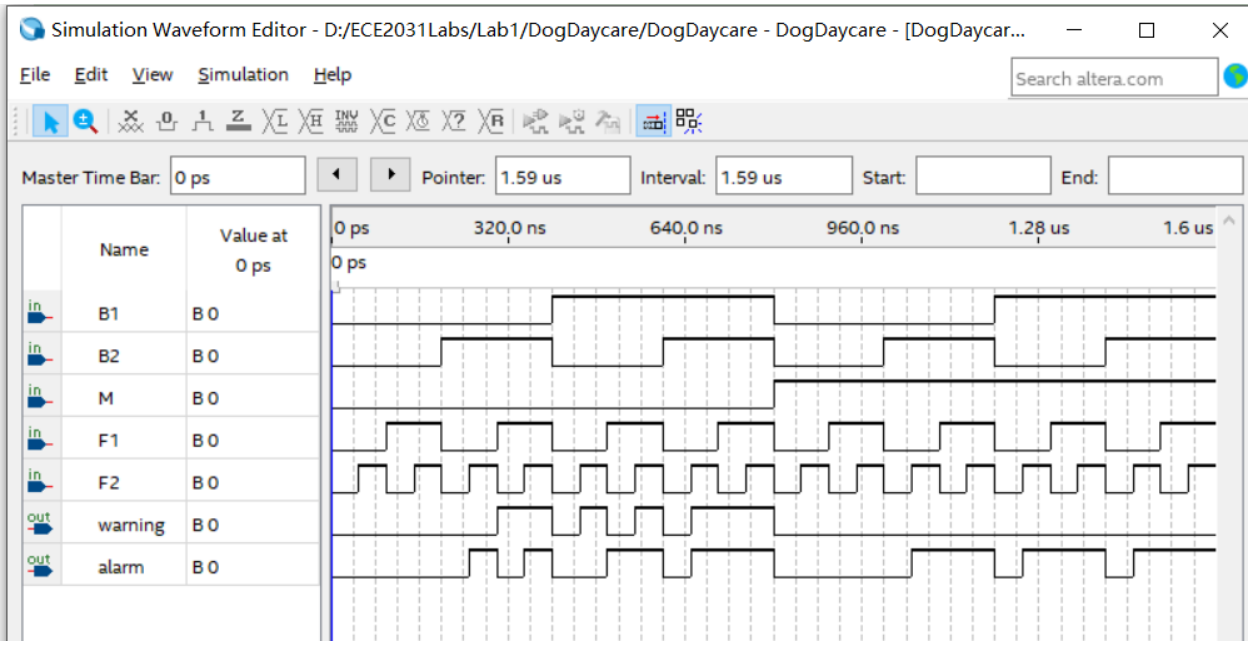

Figure 3. A simulation waveform for all possible input and output combinations of the circuit.

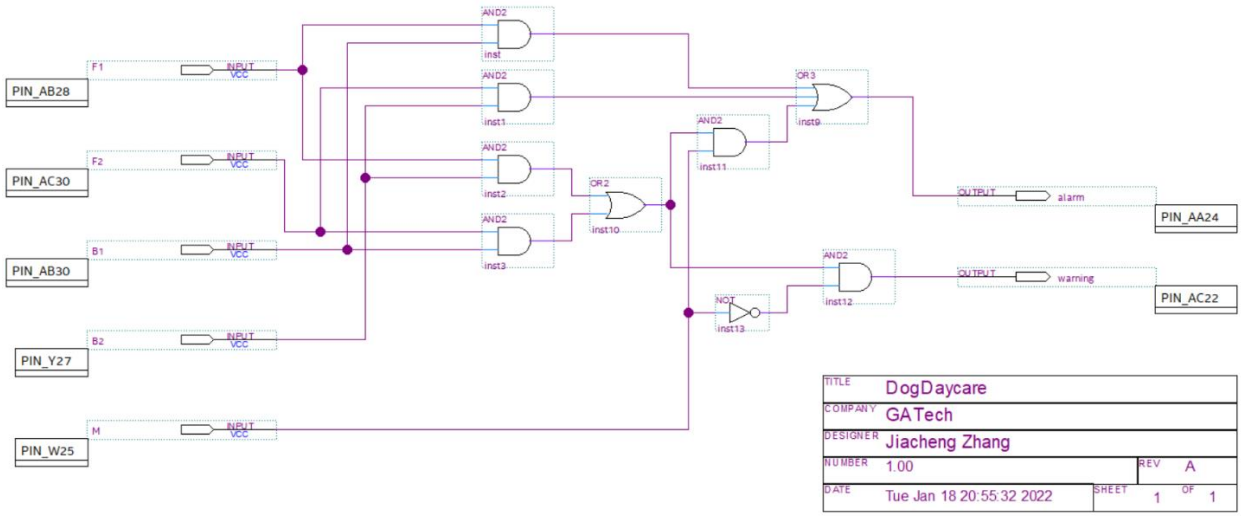

Figure 4. Schematic with FPGA pin assignments of circuit implementing alarm = $F_1 \cdot B_1 + F_2 \cdot B_2 + (F_1 \cdot B_2 + F_2 \cdot B_1) \cdot M$ and warning = $(F_1 \cdot B_2 + F_2 \cdot B_1) \cdot /M$.