Recitation Class for Final Exam
Chapter 10-12

Zexi Li

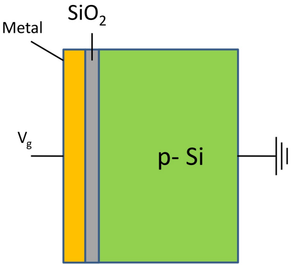
lzx12138@sjtu.edu.cn

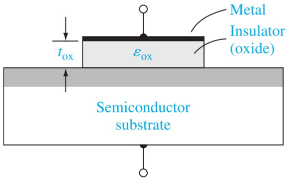
2021.08.03

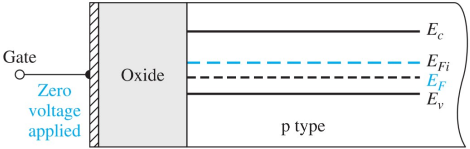
Outline

Table of Contents

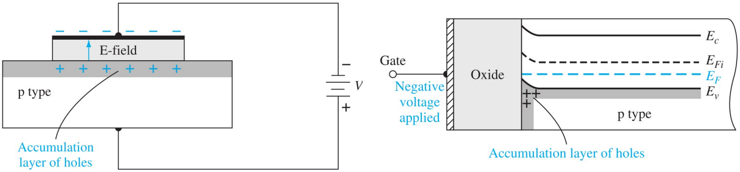
Metal–Oxide–Semiconductor



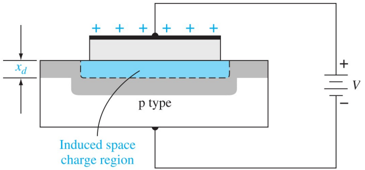


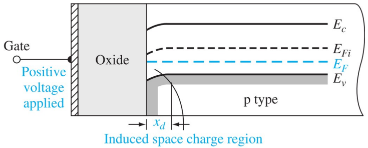


Negative Gate Voltage

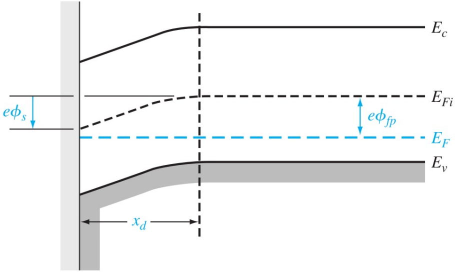


Positive Gate Voltage





Depletion Layer Thickness

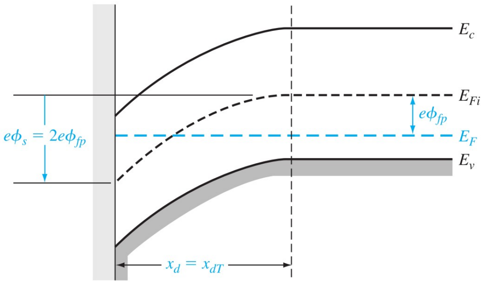


$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_a}\right)^{1/2}$$

ϕ_s: the surface potential, is the difference (in V) between E_{Fi} measured in the bulk semiconductor and E_{Fi} measured at the surface.

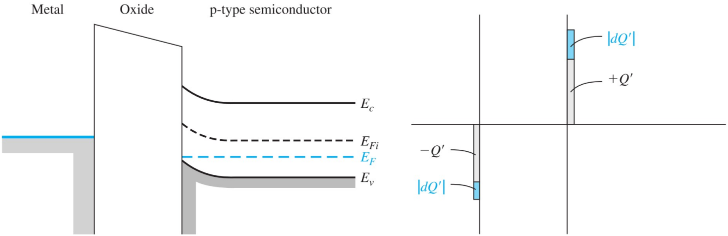
Threshold Inversion Point



$$\phi_s = 2\phi_{fp}$$

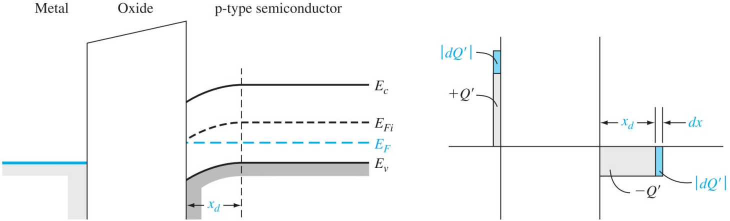
$$\boxed{x_{dT} = \left(\frac{4\varepsilon_s \phi_{fp}}{eN_a}\right)^{1/2}}$$

Accumulation



$$C'(\mathrm{acc}) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

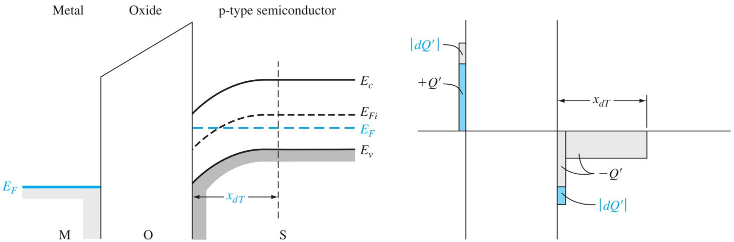
Depletion



$$C'(\text{depl}) = \frac{C_{ox}C'_{SD}}{C_{ox} + C'_{SD}}$$
$$= \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)x_d}$$

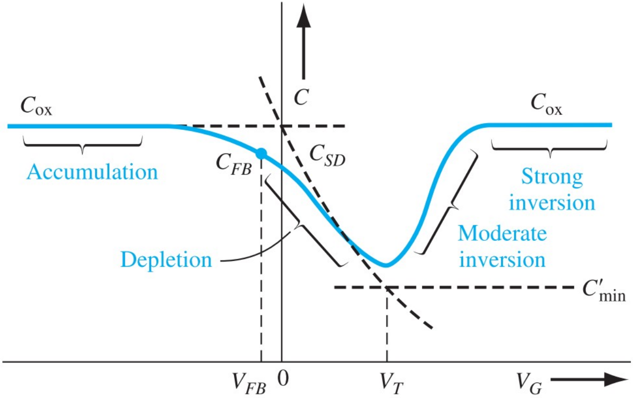
$$C'_{min} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)x_{dT}}$$

Inversion



$$C'(\text{inv}) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Ideal Low-Frequency C-V Curve

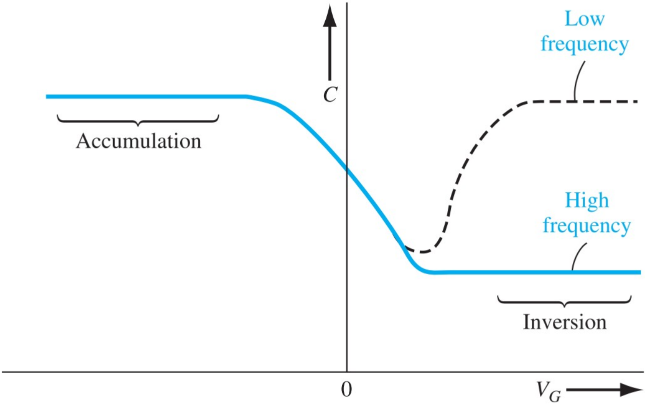


$$C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\varepsilon_s}{eN_a}\right)}}$$

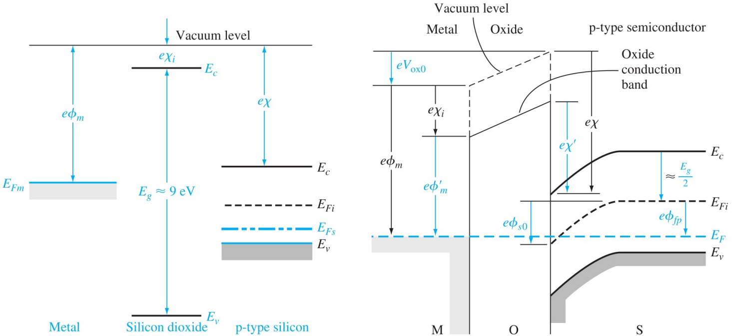
Frequency Effects

Two sources of electrons

1. Diffusion of minority carrier electrons.
2. Thermal generation of electron-hole pairs within the space charge region.



Work Function Difference

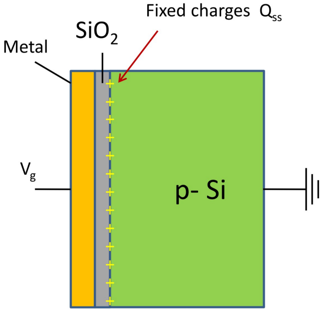


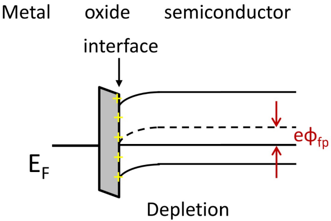
$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$$

Not required.

Fixed Charge

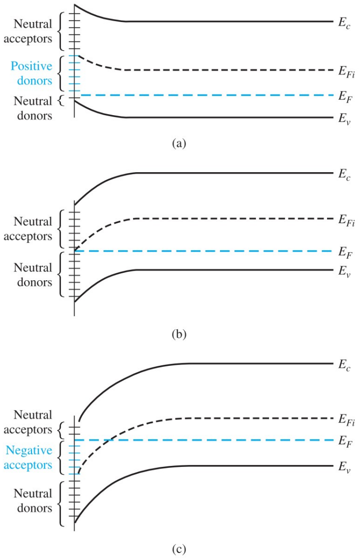


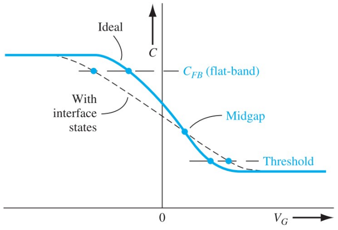


Adjustment on V_T

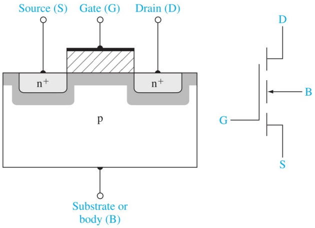
$$\boxed{\begin{aligned} \left|Q'_{SD}(\max)\right| &= eN_a x_{dT} = 2\sqrt{e\varepsilon_s N_a \phi_{fp}} \\ V_{TN} &= \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp} \\ V_{TP} &= -\frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} - 2\phi_{fn} \\ V_{FB} &= \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \cdot \frac{x}{d} \end{aligned}}$$

Surface States

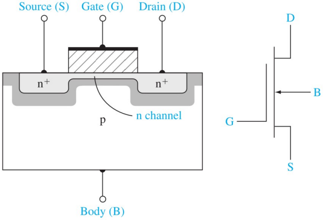




MOSFET



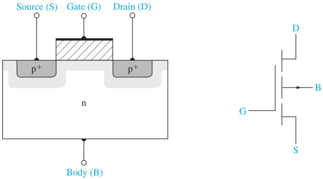
(a) n-channel enhancement MOSFET



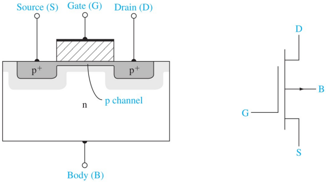
(b) n-channel depletion MOSFET

Enhancement mode: the semiconductor substrate is not inverted directly under the oxide with zero gate voltage.
Depletion mode: a p-channel region exists under the oxide with $0\,V$ applied to the gate.

MOSFET



(a) p-channel enhancement MOSFET



(b) p-channel depletion MOSFET

V_{GS} - V_T

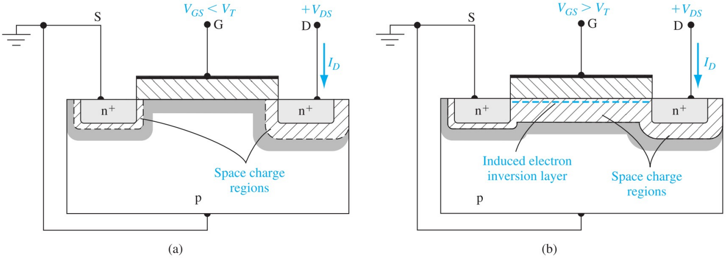


Figure: (a) $V_{GS} < V_T$, (b) $V_{GS} > V_T$

- $V_{GS} < V_T$: no inversion layer, no current.
- $V_{GS} > V_T$: inversion layer created, current flow from drain to source.

V_{DS} when $V_{GS} > V_T$

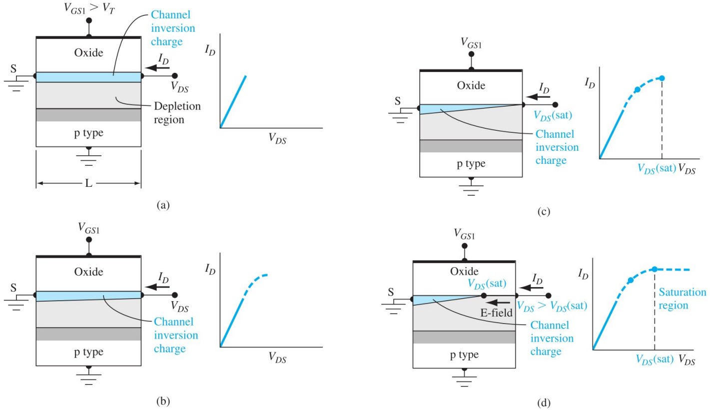
- V_{DS} low ($V_{DS} < V_{GS} - V_T$): act as a controllable resistor.

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}}$$

- V_{DS} high ($V_{DS} \geq V_{GS} - V_T$): saturation

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{2L} \left(V_{GS} - V_T \right)^2 \quad \text{(saturation)}}$$

V_{GS} - V_T

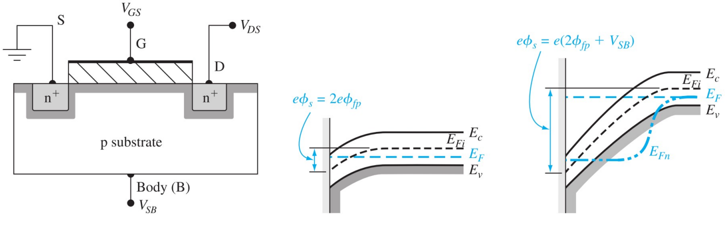


After pinch off: the electrons are injected into the space charge region where they are swept by the E-field to the drain contact.

Transconductance

$$
\begin{aligned}
g_m &= \frac{\partial I_D}{\partial V_{GS}} \\
&= \begin{cases} \mu_n C_{ox} \dfrac{W}{L} V_{DS}, & 0 < V_{DS} < V_{GS} - V_T \\ \mu_n C_{ox} \dfrac{W}{L} \left(V_{GS} - V_T \right), & V_{DS} > V_{GS} - V_T \end{cases}
\end{aligned}
$$

Substrate Bias Effects



(a) (b) (c)

$$V_{SB} = 0: \quad Q'_{SD}(\max) = -\sqrt{2e\varepsilon_s N_a(2\phi_{fp})}$$

$$V_{SB} > 0: \quad Q'_{SD} = -\sqrt{2e\varepsilon_s N_a(2\phi_{fp} + V_{SB})}$$

$$\boxed{\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]}$$

where $\Delta V_T = V_T(V_{SB} > 0) - V_T(V_{SB} = 0)$ for NMOS.

Substrate Bias Effects

$$\boxed{\begin{aligned}\Delta V_T &= -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}}\left[\sqrt{2\phi_{fp}+V_{SB}}-\sqrt{2\phi_{fp}}\right] \\ &= \gamma\left[\sqrt{2\phi_{fp}+V_{SB}}-\sqrt{2\phi_{fp}}\right], \qquad \gamma = \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}}\end{aligned}}$$

Table of Contents

I - Subthreshold Conduction (Leakage Current)

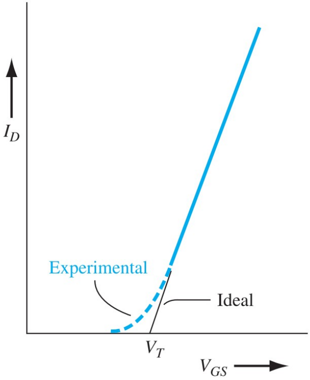
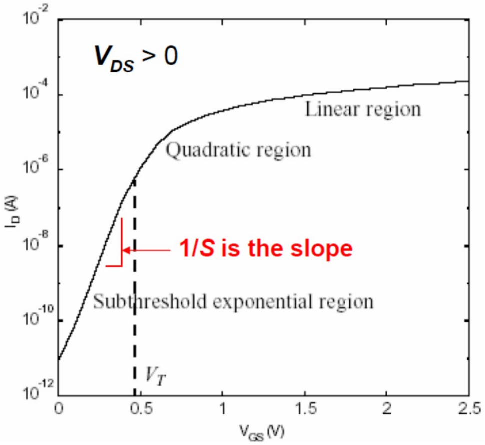


Figure: Comparison of ideal and experimental plots of $\sqrt{I_D}$ versus V_{GS}.

When $V_{GS} < V_T$, $I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$

I - Subthreshold Conduction (Leakage Current)

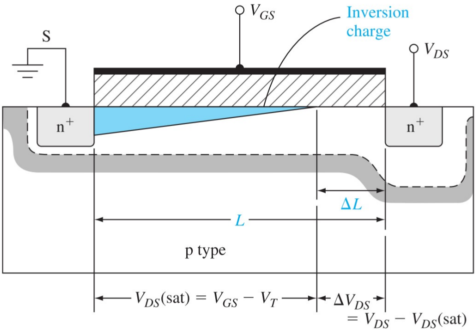
Slope Factor: defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region.



$$S = n\left(\frac{kT}{q}\ln(10)\right) \text{ (Volts per decade)}$$

$S \geq 60mV/dec$ at room temperature.

II - Channel Length Modulation



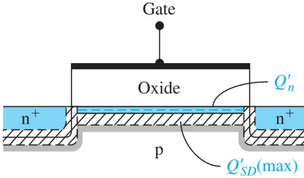
$$I'_D = \mu_n C_{ox} \frac{W}{2L} \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$$

III - Velocity Saturation

$$I_{DSAT} = WC_{ox} \left[V_{GS} - V_T - \frac{V_{DSAT}}{2} \right] v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n} v_{sat}$.

IV - Short Channel Effect



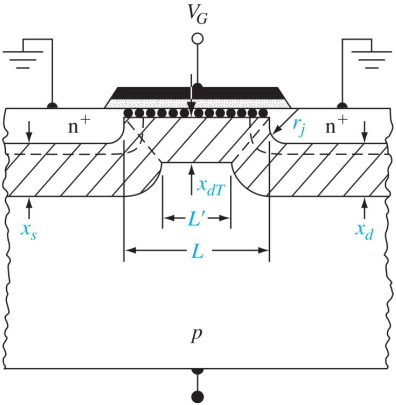
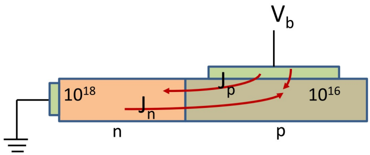
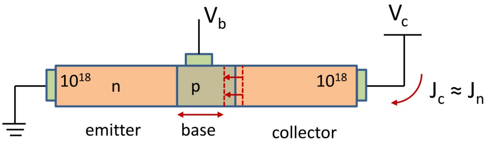


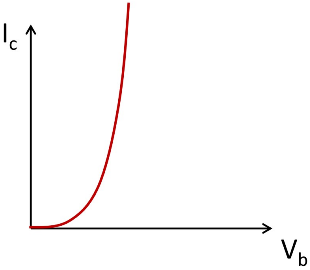
Table of Contents

Bipolar Junction Transistor





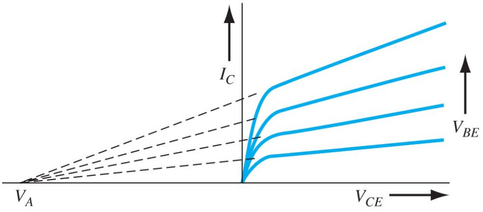
Current Volatege Relationship

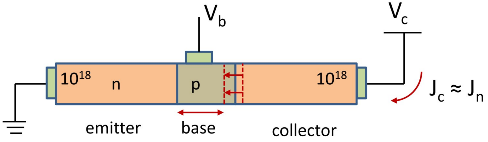


$$I_c = \beta I_s \left(\mathrm{e}^{\frac{eV_b}{nkT}} - 1 \right)$$

1. Narrower base $\rightarrow$ larger gain
2. $\beta \approx N_D / N_A$, higher emitter-to-base ratio $\rightarrow$ higher gain

Early Effect





Trade off:

Gain and Early effect.

Good luck to your final exam!