

Recitation Class 8

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Outline

Chapter 10 - Fundamentals of the Metal–Oxide–Semiconductor Field-Effect Transistor

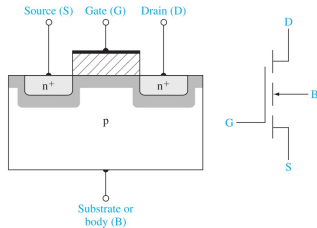
Chapter 11 - Metal–Oxide–Semiconductor Field-Effect Transistor: Additional Concepts

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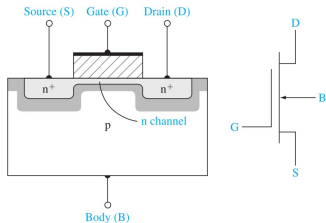
Chapter 10 - Fundamentals of the Metal–Oxide–Semiconductor
Field-Effect Transistor

Chapter 11 - Metal–Oxide–Semiconductor Field-Effect Transistor:
Additional Concepts

MOSFET



(a) n-channel enhancement MOSFET

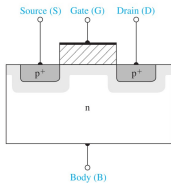


(b) n-channel depletion MOSFET

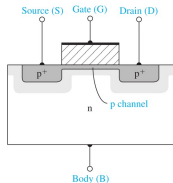
Enhancement mode: the semiconductor substrate is not inverted directly under the oxide with zero gate voltage.

Depletion mode: a p-channel region exists under the oxide with 0V applied to the gate.

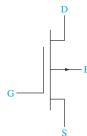
MOSFET



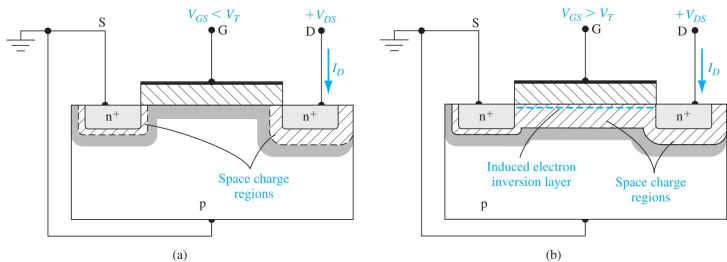
(a) p-channel enhancement MOSFET



(b) p-channel depletion MOSFET



$$V_{GS} - V_T$$



- ▶ $V_{GS} < V_T$: no inversion layer, no current.
- ▶ $V_{GS} > V_T$: inversion layer created, current flow from drain to source.

V_{DS} when $V_{GS} > V_T$

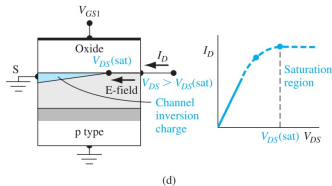
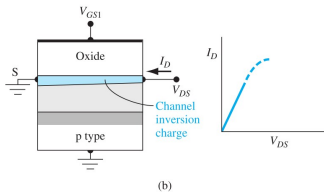
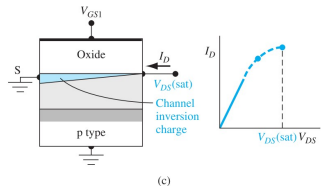
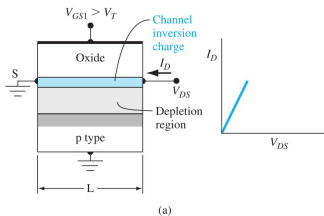
- ▶ V_{DS} low ($V_{GS} < V_{GS} - V_T$): act as a controllable resistor.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

- ▶ V_{DS} high ($V_{DS} \geq V_{GS} - V_T$): saturation

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \quad (\text{saturation})$$

$$V_{GS} - V_T$$

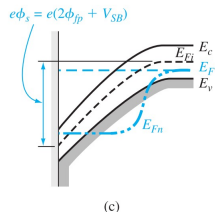
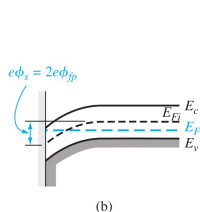
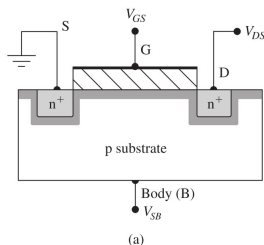


After pinch off: the electrons are injected into the space charge region where they are swept by the E-field to the drain contact.

Transconductance

$$\begin{aligned} g_m &= \frac{\partial I_D}{\partial V_{GS}} \\ &= \begin{cases} \mu_n C_{ox} \frac{W}{L} V_{DS}, & 0 < V_{DS} < V_{GS} - V_T \\ \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T), & V_{DS} > V_{GS} - V_T \end{cases} \end{aligned}$$

Substrate Bias Effects



$$V_{SB} = 0 : Q'_{SD}(\text{max}) = -\sqrt{2e\epsilon_s N_a (2\phi_{fp})}$$

$$V_{SB} > 0 : Q'_{SD} = -\sqrt{2e\epsilon_s N_a (2\phi_{fp} + V_{SB})}$$

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right]$$

where $\Delta V_T = V_T(V_{SB} > 0) - V_T(V_{SB} = 0)$ for NMOS.

Substrate Bias Effects

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right]$$
$$= \gamma \left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}} \right], \quad \gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$$

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Additional Concepts

I - Subthreshold Conduction (Leakage Current)

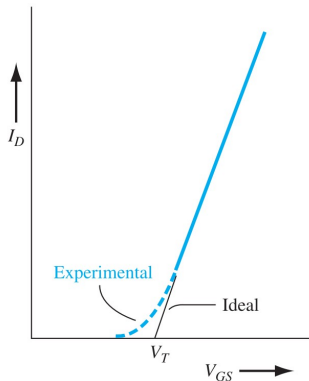
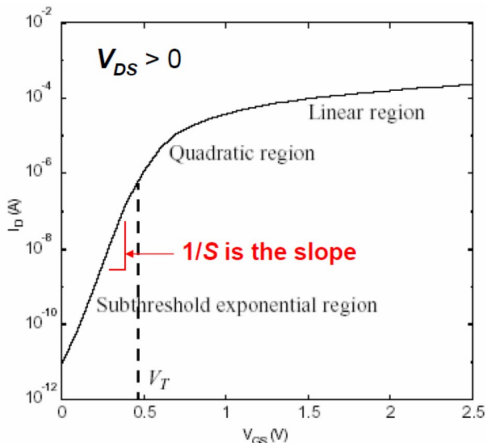


Figure: Comparison of ideal and experimental plots of $\sqrt{I_D}$ versus V_{GS} .

When $V_{GS} < V_T$, $I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$

I - Subthreshold Conduction (Leakage Current)

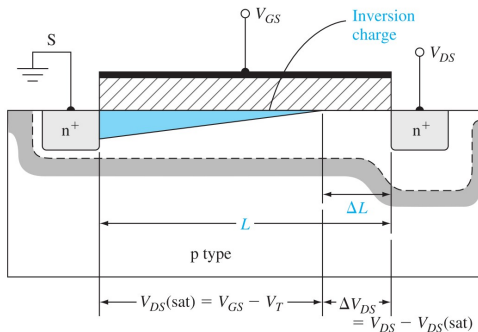
Slope Factor: defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region.



$$S = n \left(\frac{kT}{q} \ln(10) \right) \text{ (Volts per decade)}$$

$S \geq 60 \text{ mV/dec}$ at room temperature.

II - Channel Length Modulation



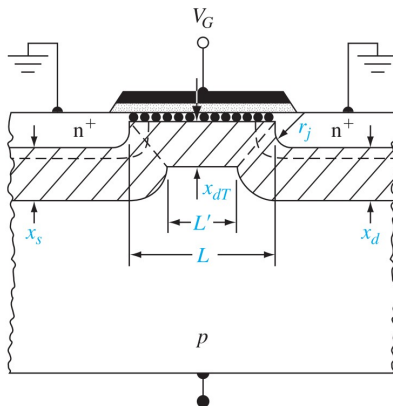
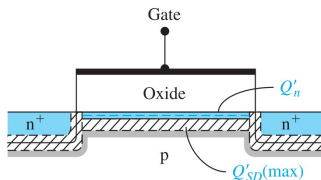
$$I'_D = \mu_n C_{ox} \frac{W}{2L} \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right]$$

III - Velocity Saturation

$$I_{DSAT} = WC_{ox} \left[V_{GS} - V_T - \frac{V_{DSAT}}{2} \right] v_{sat}$$

where $V_{DSAT} = \frac{L}{\mu_n} v_{sat}$.

IV - Short Channel Effect



End