VE373 Recitation Class

Week 5

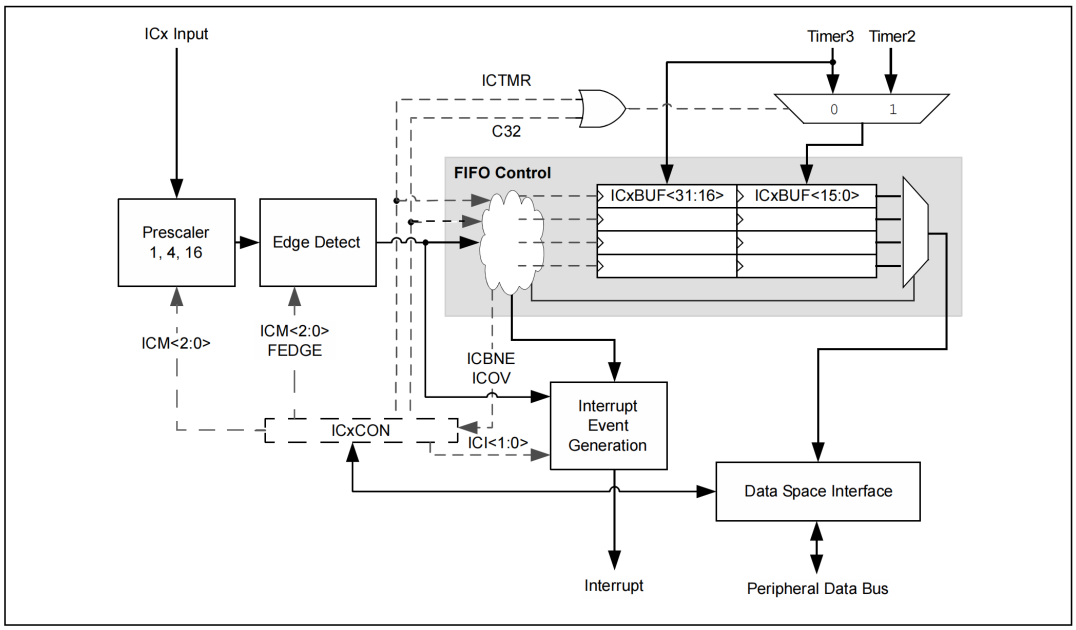
2022.06.11

L8 — Input Capture

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

1. **Advantage (comparing to naive solution)**
    1. Accurate
    2. No preemption issue
    3. Don't bother CPU too much
2. **Block diagram**

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



3. **Operation modes**
    - Simple capture event modes
        - Capture timer value on every falling edge
        - Capture timer value on every rising edge
        - Capture timer value on every edge, with specified starting edge (rising or falling)
    - Prescaled capture event modes
        - Capture timer value on every 4th rising edge
        - Capture timer value on every 16th rising edge
    - Edge detect mode
    - Interrupt-only mode
4. **Persistent interrupt**

    Interrupt is not cleared unless the interrupt condition is cleared.

Table 15-4: Interrupt Persistence Conditions

ICxCON Value	Set Condition	Persistence
ICI<1:0> = 11	Interrupt on every fourth capture event.	Interrupt is active if the number of FIFO entries is equal to 4.
ICI<1:0> = 10	Interrupt on every third capture event.	Interrupt is active if the number of FIFO entries is greater than or equal to 3.
ICI<1:0> = 01	Interrupt on every second capture event.	Interrupt is active if the number of FIFO entries is greater than or equal to 2.
ICI<1:0> = 00 or Edge Detect modes (see the ICM<2:0> bits in the ICxCON register (Register 15-1))	Interrupt on every capture event.	Interrupt is active if the number of FIFO entries is greater than or equal to 1.
ICOV = 1	Interrupt on fifth capture event if FIFO is full.	Interrupt is active until the error condition flag (ICxCON.ICOV) is cleared.

5. **Simple capture event modes**
   - 2–3 T_{PB} delay after the event due to synchronization
   - Capture input is sampled by `PBCLK`, therefore input signal high and low width $> T_{PB}$.
6. **Edge Detect Mode**
   - Prescaler and interrupt count not used.
   - Buffer overflow never signals.
   - Interrupt request on every capture.
7. **Interrupt-only mode**
   - Rising edge on ICx triggers an interrupt
     - Not functioning during normal operation
     - No timer capture
     - No buffer update
   - Used only as a wake-up mechanism for SLEEP or IDLE modes
8. **Capture buffer flags**
   - `ICBNE` (`ICxCON<3>`): IC buffer not empty
     - Read-only
     - Signals when 1 or more entries
   - `ICOV` (`ICxCON<4>`): IC buffer overflow
     - Signals on the 5th capture
     - All extra capture values are lost, until flag cleared
     - Flag cleared when
       * IC Module disabled
       * Module reset
       * `ICBNE` becomes 0 — IC buffer empty
9. **Capture event and interrupt event**
   - Capture event: capture change of `ICx` and store timer value in the FIFO.
   - Interrupt event: interrupt after certain amount of capture events.
10. **Examples**

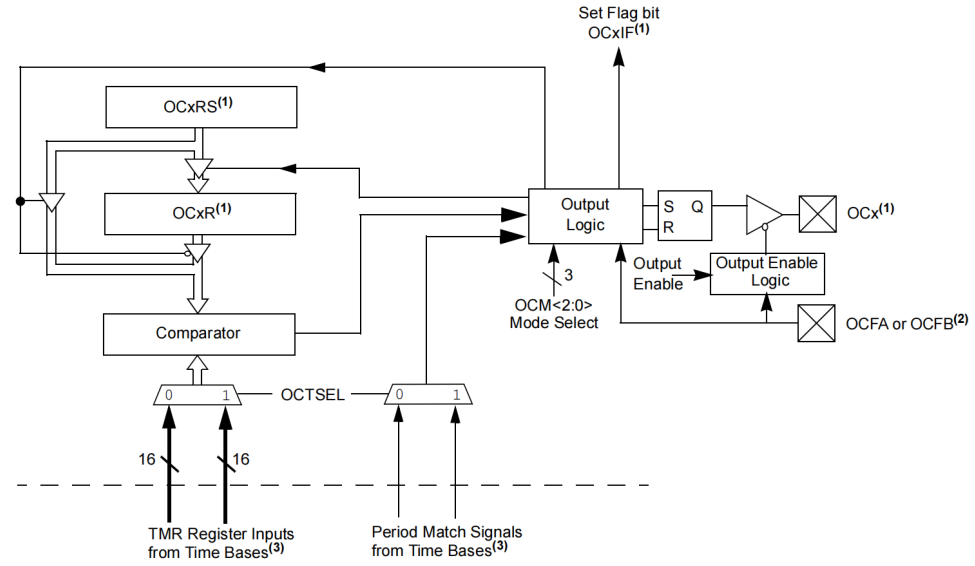
    See reference manual or slides.

L9 — Output Compare and PWM

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events.

1. **Block diagram**

FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.
2: The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.
3: Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

2. **Operation mode**

   - Single Compare Match mode
     Drive high, drive low, toggle
   - Dual Compare Match mode
     Single output pulse, continuous output pulses
   - Simple Pulse Width Modulation (PWM) mode
     With or without fault protection input

3. **Single Compare Match mode**

   - Compare forces `OCx` pin high; initial state of pin is low. Interrupt is generated on the single compare match event.
   - Compare forces `OCx` pin low; initial state of pin is high. Interrupt is generated on the single compare match event.
   - Compare toggles `OCx` pin. Toggle event is continuous and an interrupt is generated for each toggle event.

4. **Dual Compare Match mode**

   Single or continues pulse.

5. **Single pulse special situations**

   - `PRy >= OCxRS > OCxR = TMRy = 0`
     The initial match of `OCxR` and `TMRy` at 0 doesn't drive high, work normally afterwards

- `PRy >= OCxR >= OCxRS`
  Match `OCxR` first, match `OCxRS` in next counting round
- `OCxRS > PRy >= OCxR`
  Only rising edge generated on first match, then signal remains high, no interrupt generated
- `OCxR > PRy`
  Not working, `OCx` remains low

6. **PWM mode**

   Covered in next RC.

7. **Examples**

   See reference manual or slides.