

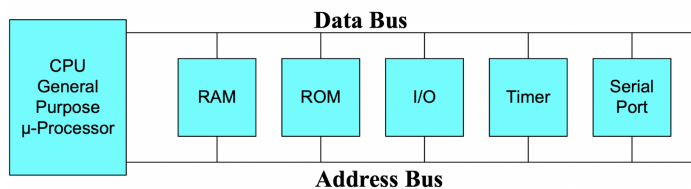
VE373 Recitation Class

Week 2

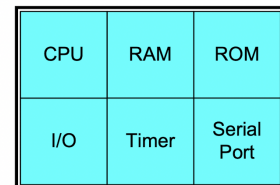
2022.05.21

L1 — Introduction to Embedded Systems

1. Microprocessor (MPU) & Microcontroller (MCU)



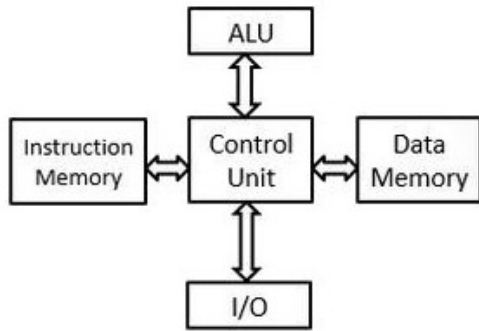
(a) Microprocessor



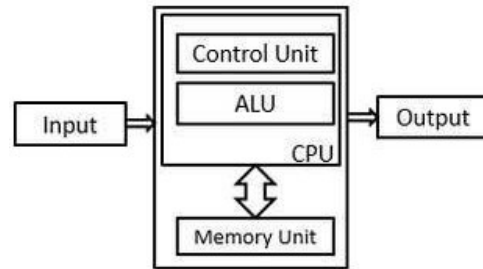
(b) Microcontroller

Microprocessor	Micro Controller
Microprocessor is heart of Computer system.	Micro controller is a hear of embedded system.
It is just a processor. Memory and I/O components have to be connected externally.	Micro controller has external processor along with internal memory and I/O components.
The circuit is large.	The circuit is small.
Cannot be used in compact systems and hence inefficient.	Can be used in compact systems and hence it is an efficient technique.
Cost of the entire system increases.	Cost of the entire system is low.
Due to external components, the entire power consumption is high. Hence it is not suitable to be used with devices running on stored power like batteries.	Since external components are low, total power consumption is less and can be used with devices running on stored power like batteries.
Most of the microprocessors do not have power saving features.	Most of the micro controllers have power saving modes like idle mode and power saving mode. This helps to reduce power consumption even further.
Since memory and I/O components are all external, each instruction will need external operation, hence it is relatively slower.	Since components are internal, most of the operations are internal instruction, hence speed is fast.
Microprocessors have less number of registers, hence more operations are memory based.	Micro controller have more number of registers, hence the programs are easier to write
Microprocessors are based on Von Neumann model/architecture where program and data are stored in same memory module.	Micro controllers are based on Harvard architecture where program memory and Data memory are separate.
Mainly used in personal computers.	Used mainly in washing machines, MP2 players.

2. Von Neumann & Harvard Architecture



(a) Harvard Architecture



(b) Von Neumann Architecture

Harvard architecture	Von Neumann architecture
It required two memories for their instruction and data.	It required only one memory for their instruction and data.
Harvard architecture is required separate bus for instruction and data.	Von Neumann architecture is required only one bus for instruction and data.
Processor can complete an instruction in one cycle	Processor needs two clock cycles to complete an instruction.
Easier to pipeline, so high performance can be achieve.	Low performance as compared to Harvard architecture.
Comparatively high cost.	It is cheaper.

L2 — PIC MCU Architecture

1. PIC32

- MIPS architecture, M4K core, RISC, 5-stage pipelining
- **32-bit address and data bus**
- **200 MHz max frequency**
- 32 32-bit general purpose registers (GPR)
- 64K to 512K on-chip flash memory
- 16K to 128K bytes on-chip SRAM
- **4GB virtual memory space**
- SFRs in CPU and coprocessor0 (CP0)
- Multiple interrupt sources and interrupt vectors
- **A variety of peripherals**
- 7 sets of I/O ports

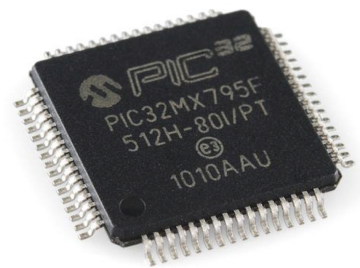


Figure 3: 32-bit PIC32 MCU Example: Architecture

n -bit data address bus = support up to 2^n byte memory.

PIC32 is a combination of Von Neumann and Harvard architecture. See [here](#) for more details if interested.

2. Special Function Register

Used to config, control and monitor various aspects of the microprocessor's function.

For example, T1CON, TMR1 and PR1 when using Timer 1.

L3 — Embedded Programming

1. Compiler

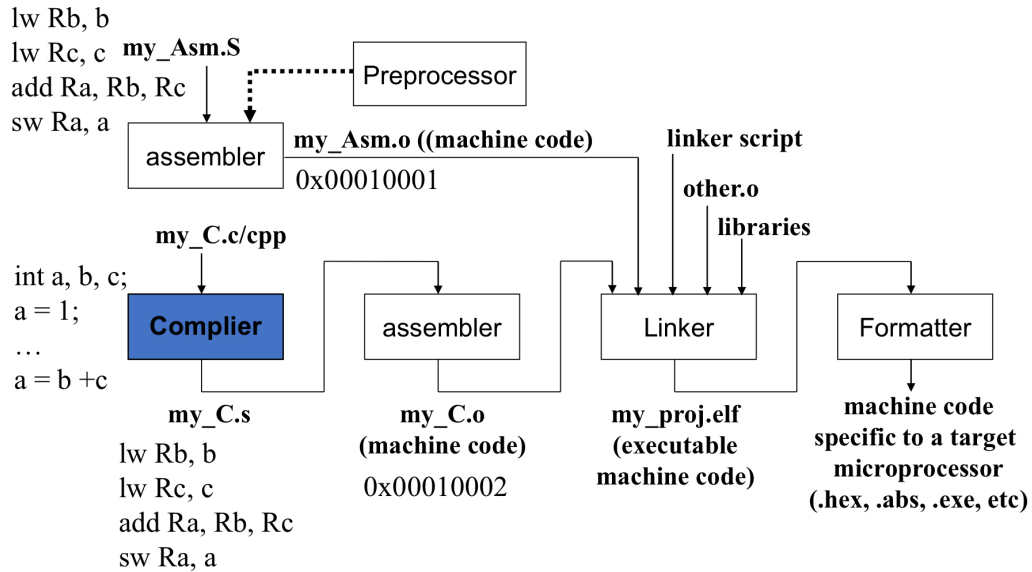


Figure 4: Workflow

2. Const & Volatile

- **const**: the value not supposed to be written by program (read only).
- **volatile**: the value can be changed by something other than program so it should be reexamined frequently.

3. Directives

Directives: compiler dependent commands.

e.g. `#pragma interrupt func_name ipln` (will be used later).

L4 — Timers and IO

1. Oscillator

- **Internal oscillator**:
 - Integrated on-chip within the processor
 - Low frequency accuracy and stability.
 - Most of internal oscillator are RC circuits
- **External oscillator**
 - Located off-chip on the PCB
 - High frequency accuracy and stability
 - Most of external oscillator are crystal oscillator

Peripherals don't have a high clock frequency:

- No need
- Limited by parasitics
- Power consumption

2. Timer

Two types, five timers on PIC32:

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- The diagram illustrates the internal architecture of the TMR1 module. At the top, the **PR1** register provides a value to the **16-bit Comparator**. The **16-bit Comparator** outputs an **Equal** signal to the **Reset** input of the **TMR1** counter. The **TMR1** counter's output is connected to the **TSYNC (T1CON<2>)** input of a 2-to-1 multiplexer. The other input of this multiplexer is the **Sync** signal. The output of the multiplexer is connected to the **D** input of a D flip-flop. The **Q** output of the flip-flop is connected to the **0** input of a 2-to-1 multiplexer, which also receives the **T1IF Event Flag** as input **1**. The output of this multiplexer is the **TGATE (T1CON<7>)** signal. The **Q** output of the flip-flop is also connected to the **TGATE (T1CON<7>)** signal line. The **Q** output of the flip-flop is also connected to the **TCS (T1CON<1>)** input of a 3-to-1 multiplexer. The **Q** output of the flip-flop is also connected to the **ON (T1CON<15>)** input of a 3-to-1 multiplexer. The **Q** output of the flip-flop is also connected to the **Prescaler** input of a 4-to-1 multiplexer. The **Prescaler** has inputs for **1, 8, 64, 256**. The output of the 4-to-1 multiplexer is connected to the **TCKPS<1:0> (T1CON<5:4>)** input of the **Prescaler**. The **Prescaler** output is connected to the **Gate Sync** input of a **Gate Sync** block. The **Gate Sync** block output is connected to the **AND** input of a 3-to-1 multiplexer. The **PBCLK** signal is connected to the **0** input of the 3-to-1 multiplexer. The **Q** output of the flip-flop is connected to the **1** input of the 3-to-1 multiplexer. The output of the 3-to-1 multiplexer is connected to the **Q** input of the D flip-flop. The **SOSCO/T1CK** and **SOSCI** signals are connected to the **SOSCEN(1)** input of a buffer. The output of the buffer is connected to the **Q** input of the D flip-flop. The **Q** output of the flip-flop is connected to the **TGATE (T1CON<7>)** signal line.